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ELECTRONICS SEMINAR

INTRODUCTION TO ASIC DESIGN

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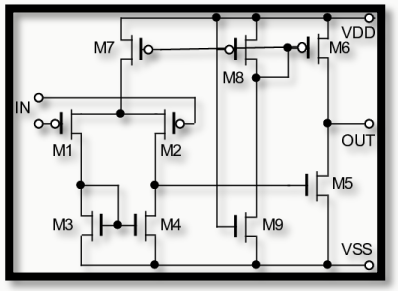
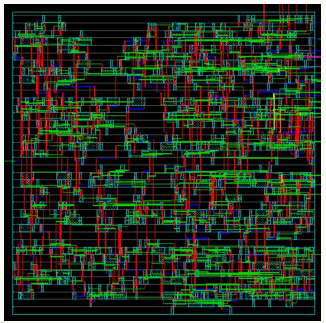
WHY ASICS INSTEAD OF FPGAS OR MCUS?

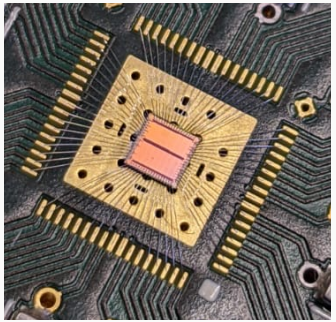
- Application-specific integrated circuit
  - Custom all-in-one solution, specific analog circuits as well as digital logic
  - Integrated solution leads to better signal integrity
- ASICs can be highly optimized
- Smaller resource footprint
  - Space, size, power, material constraints
- Radiation hardness → Commercial solutions often not radiation hard

ASIC DESIGN FLOW

```
15    ff_proc: process (clk)
16    begin
17      if (clk = '1' and clk'event) then
18        q <= d;
19      end if;
20    end process ff_proc;
```







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ASIC DESIGN FLOWS

- Full Custom Design Methodology
  - Standard for custom analog circuits e.g. amplifiers, regulators, I/O cells, etc.
  - Everything create by designer, individual transistor sizes, layout, interconnect

- Cell based Design Methodology
  - Primarily used for digital circuits
  - The designer uses pre-characterized, pre-designed cells
  - Automation: Most of the design process, including placement and routing

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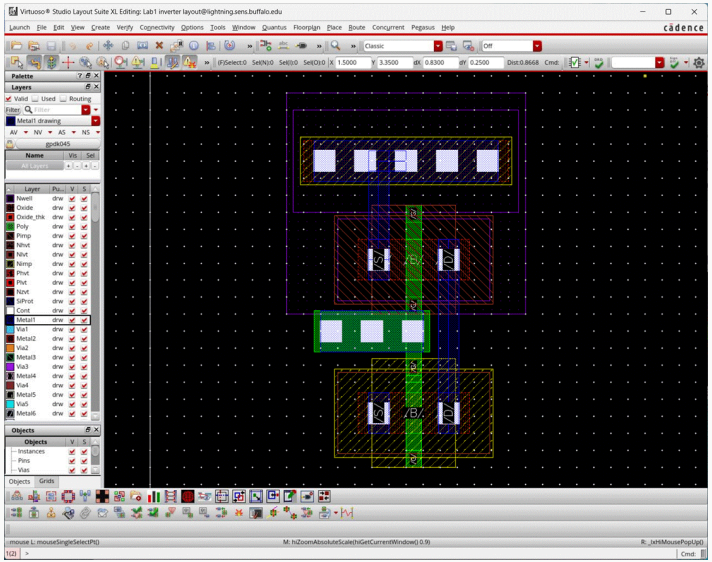
FULL CUSTOM DESIGN METHODOLOGY (ANALOG)

FULL CUSTOM DESIGN METHODOLOGY

- Design specified up to level of individual transistor
  - Allows customization of all design aspects
  - Requires experience in circuit design
  - Large design effort, time consuming
- Design flow used for sensor development
- Used to be default for top-level integration
  - Complex designs tend to favor digital-on-top



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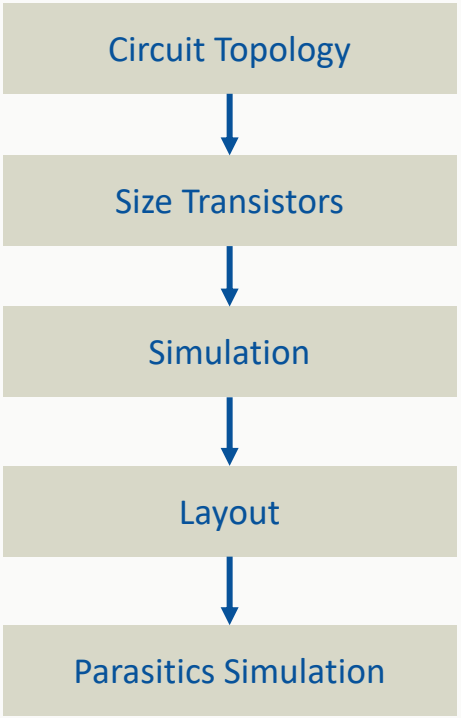
FULL CUSTOM DESIGN METHODOLOGY

- Develop circuit topology in schematic editor
- Size all transistors (width/length) to meet requirements
- Simulate design at various stages
  - AC, DC Biasing, Stability Analysis, etc.
- Manual Placement, Layout
  - Minimize Parasitics, Match Critical Components
  - Power and Ground Routing, Guard Elements



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CELL BASED DESIGN METHODOLOGY (DIGITAL)

RTL DESIGN / VERIFICATION

- RTL Design
  - Design Abstraction written in Verilog or VHDL
  - Focuses on data transfer and data is processing
  - Combinational and sequential logic
- Verification
  - Testbenches / UVM / Cocotb verification framework
  - Takes more effort than the RTL Design
    - Especially for radhard designs

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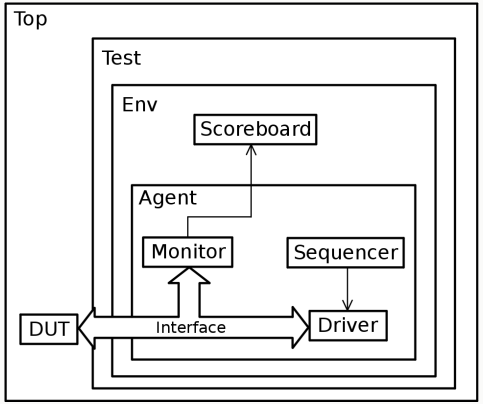

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SYNTHESIS

- Translation from high-level description to netlist
- Netlist consists of standard cells and interconnections
- Optimization according to constraints
- Hierarchy Flattening

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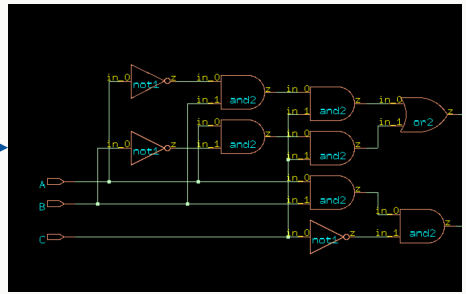

Elaboration

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Generic Synthesis

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Technology Mapping

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Optimization

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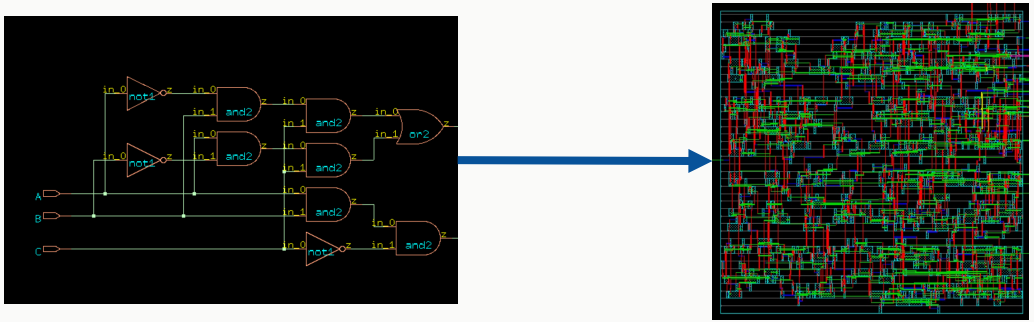
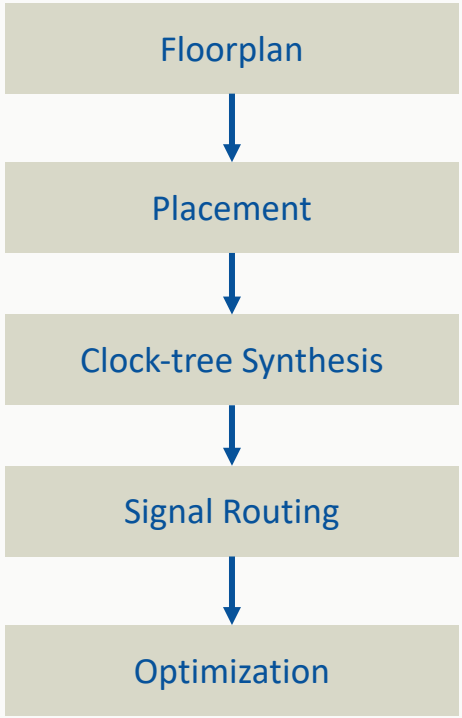
PHYSICAL DESIGN

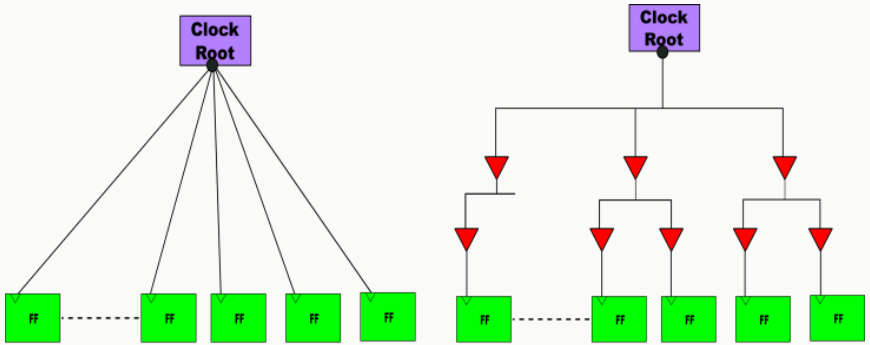
- Conversion from synthesized netlist into layout of ASIC
- Floorplan defines general layout e.g., position of pins
- Placement of cells, minimizing the total wire length
- Routing connects the cells according to the netlist



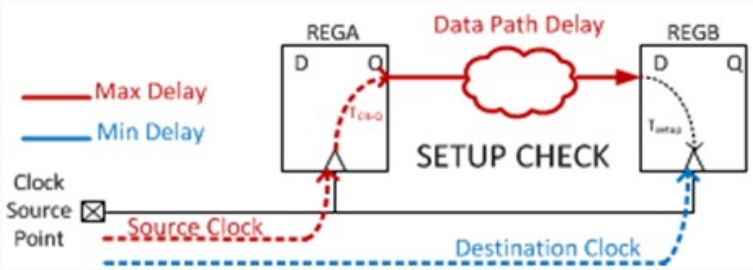


CLOCK TREE SYNTHESIS / TIMING

- Clock-tree distributes clock to all sinks
  - CTS aims to minimize clock skew
  - Introduction of clock buffer cells

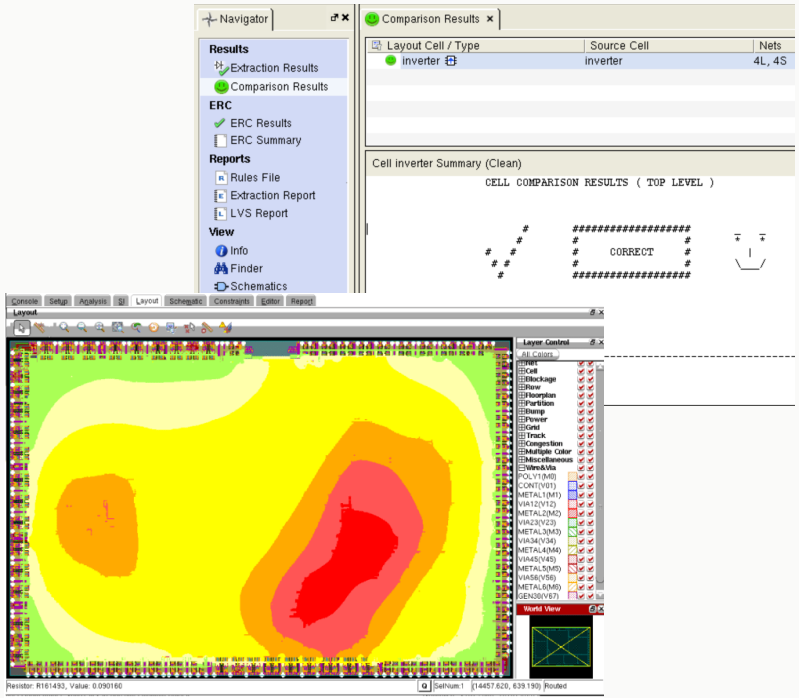


- Timing optimization
  - Ensure timing is met for all paths
  - resize gates, add/delete buffers
  - restructure netlist, move instances



SIGNOFF / MANUFACTURABILITY VERIFICATION

- Static Timing Analysis (STA)
- Design Rule Checking (DRC)
  - Design for Manufacturability (DFM)
- Layout vs. Schematic (LVS)
- Power Integrity Analysis
  - IR Drop / Electromigration



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REQUIREMENTS FOR ASIC DESIGN

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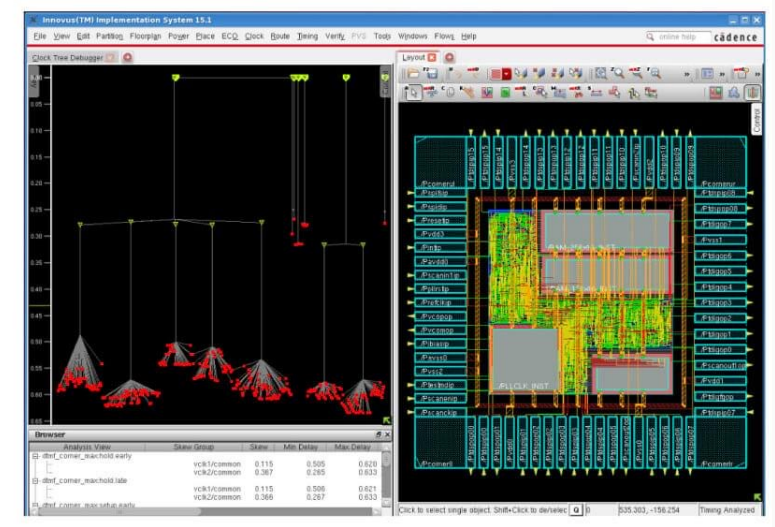
ELECTRONIC DESIGN AUTOMATION (EDA) TOOLS

- Schematic Design Editor / Layout Tool
- Synthesis / Place and Route Tool
- Parasitic Extraction
- Timing and Power Analysis
- Physical Verification
- Simulators



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PROCESS DESIGN KIT (PDK)

- Describe the specifics of a semiconductor process
- Fundamental building block for integrated circuit (IC) design
- Input to EDA tools during chip design:
  - Technology data (Layers / Process constraints / Electrical Properties)
  - Primitive device library / parameterized Cells
  - Simulation Models (Spice)
  - Verification checks / Rules (DRC / LVS / Parasitics)

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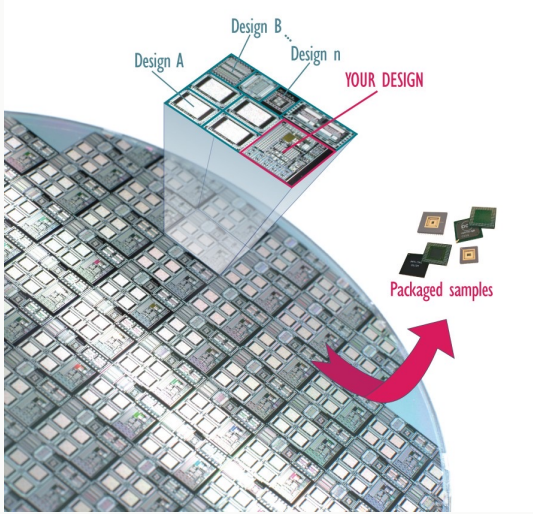
STANDARD CELLS / IP BLOCKS

- Standard Cells
  - Used in cell-based design flow (Logic synthesis)
  - Set of pre-designed digital cells (AND, Flip-flops, Multiplexer)
  - Physical Layout
  - Logic, timing and power characterization data and simulation models
- IP-Blocks
  - pre-designed, larger functional units (made from standard cells)
  - Custom designed blocks like PLLs or SRAM

PRODUCTION / MANUFACTURING COST

- General Multi-Project-Wafer
- Reduce cost by sharing wafer with different projects
- Available through EUROPRACTICE / IMEC / CERN



TSMC mini@sic Pricelist	Standard prices	
	EUR / min area	EUR / extra area
TSMC 130 BCD+ (min area = 6 mm^2)	13,982	231 / 0.1 mm^2
TSMC 65 LP/GP MS RF (min area = 1 mm^2)	4,462	418 / 0.1 mm^2
TSMC 40 LP MS RF (min area = 3 mm^2) [1]	21,249	662 / 0.1 mm^2
TSMC 28 HPC+ RF (min area = 1 mm^2) [1]	10,541	915 / 0.1 mm^2
TSMC 16 FFC RF (min area = 1mm^2) [2, 3]	30,364	2,814 / 0.1 mm^2

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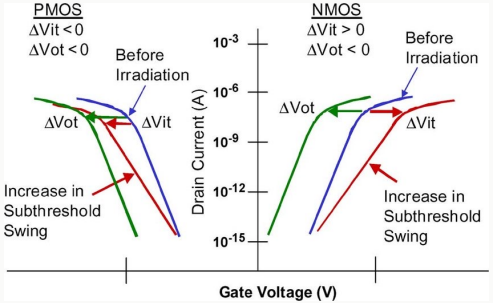
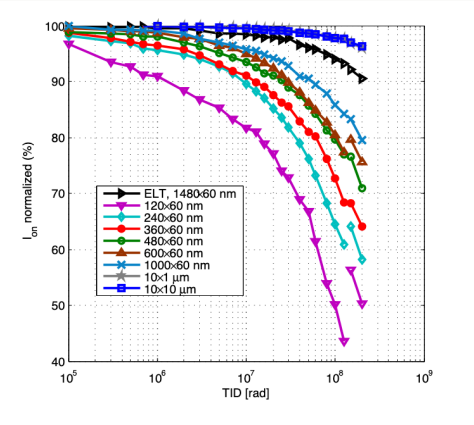
RADIATION EFFECTS

CUMULATIVE RADIATION EFFECTS

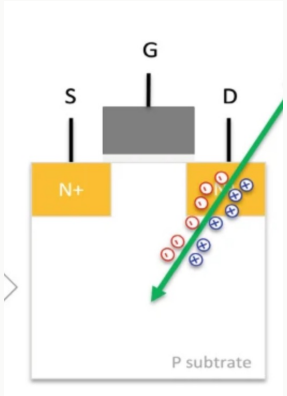
- Cumulative radiation effects (TID):
  - Affect transistors parameter over time
  - Shift in threshold
  - Reduction in drive current
  - Depending on technology, size, bias conditions, etc.
- Impact on digital circuits:
  - Changes in leakage currents
  - Reduced timing margin



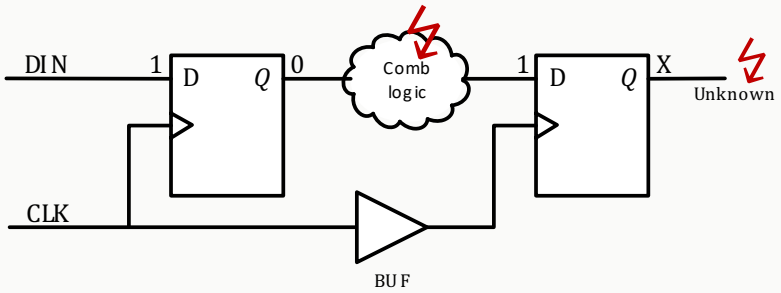


SINGLE EVENT EFFECTS

- Can be triggered at any time by a single particle trace
- Permanent effects, non recoverable, may damage device
  - E.g., Single event latch-up



- Temporary effects, recoverable
  - Single Event Upsets and Transients
  - Can lead to functional interrupt



SET in comb. logic (setup / hold violation)

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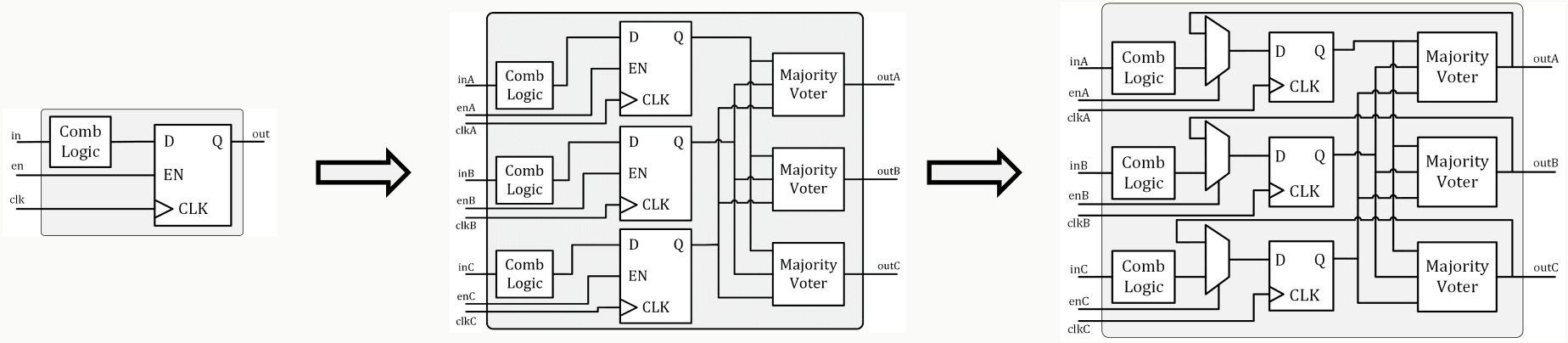
RADIATION HARDENING OF ASICS

- Radiation-Hardening by Process (RHBP)
  - Optimization at technology level e.g., materials, oxide thickness etc.

- Radiation Hardening by Design (RHBD)
  - Optimization at cell level e.g., layout, guard rings etc.
  - Special circuit topology e.g., dual interlocked storage cells
  - Single event mitigation by introducing signal redundancy

TRIPLE MODULAR REDUNDANCY

- Triplication and majority voting of the three identical instances
- Typically used for individual signals and modules, not for large data blocks
- Applicable at different levels, e.g. signal or module level



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