Custom Analog IC Design towards AI Automation

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ARISTOTLE UNIVERSITY OF THESSALONIKI

Presenters

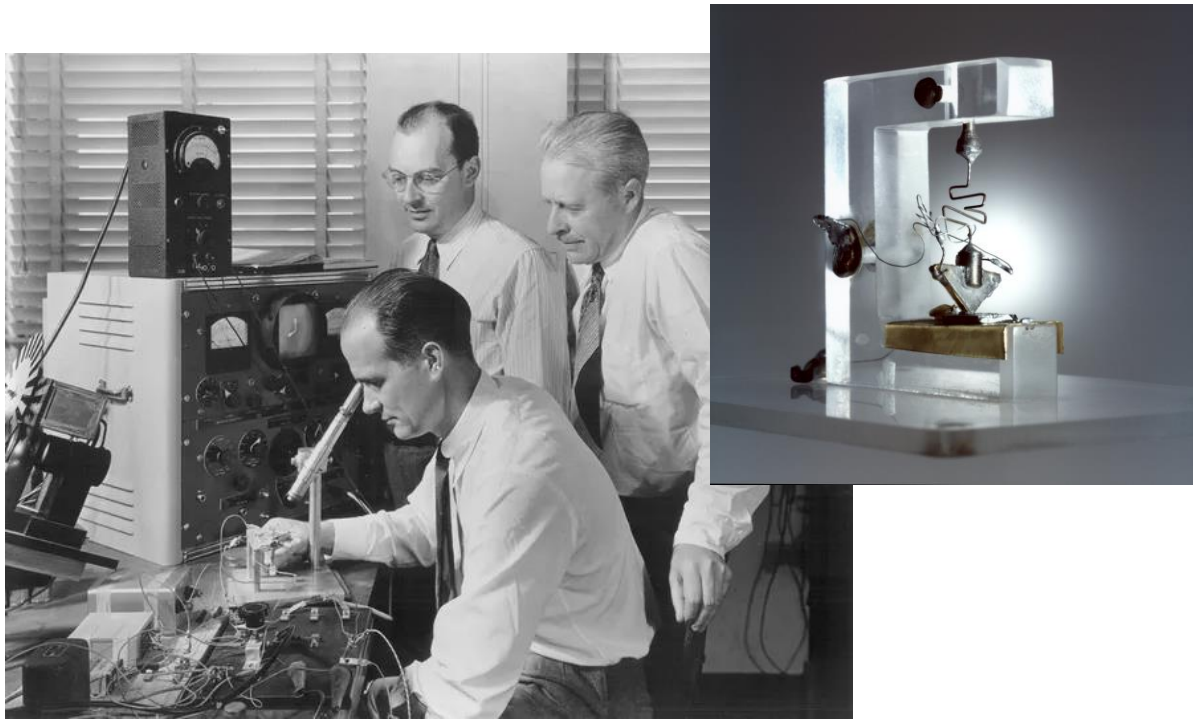
Eleni Papageorgiou is a PhD candidate at Aristotle University of Thessaloniki (AUTH), specializing in machine learning applications for automating analog/RF and mixed signal integrated circuit design. With a degree in Electrical and Computer Engineering, particularly in electronics and computer engineering, she has authored two publications on automated transistor parameter extraction and operational amplifier design, both utilizing reinforcement learning techniques. She is an expert on ML and software development.

Prof. Dr. Thomas Noulis is an Academic and a Semiconductor Industry expert (INTEL Corp., INFINEON AG, HELIC Inc. (ANSYS)) with more than 15 years of international experience on Design System Development, Analog/RFMS circuit Design, Design Methodology and international project management. He holds B.Sc. Degree in Physics (2003), MSc. Degree in Electronics Engineering (2005), and a Ph.D. (2009) from Aristotle Univ. of Thessaloniki (collaboration with LAAS, Toulouse-France). Dr. Noulis is the main author of more than 80 publications, holds one European patent and he is the Editor of three books. Currently he is an Assistant Professor in the Physics Dept. of Aristotle Univ. of Thessaloniki, Greece.

Overview

- **Part I**
  - **IC History – State of the Art - Future Perspective**
  - Analog Design and Custom IC Design Flow
  - Artificial Intelligence and Impact on IC Design
- Part II
  - What is AI?
  - OpAmp Case Study

The First Transistor



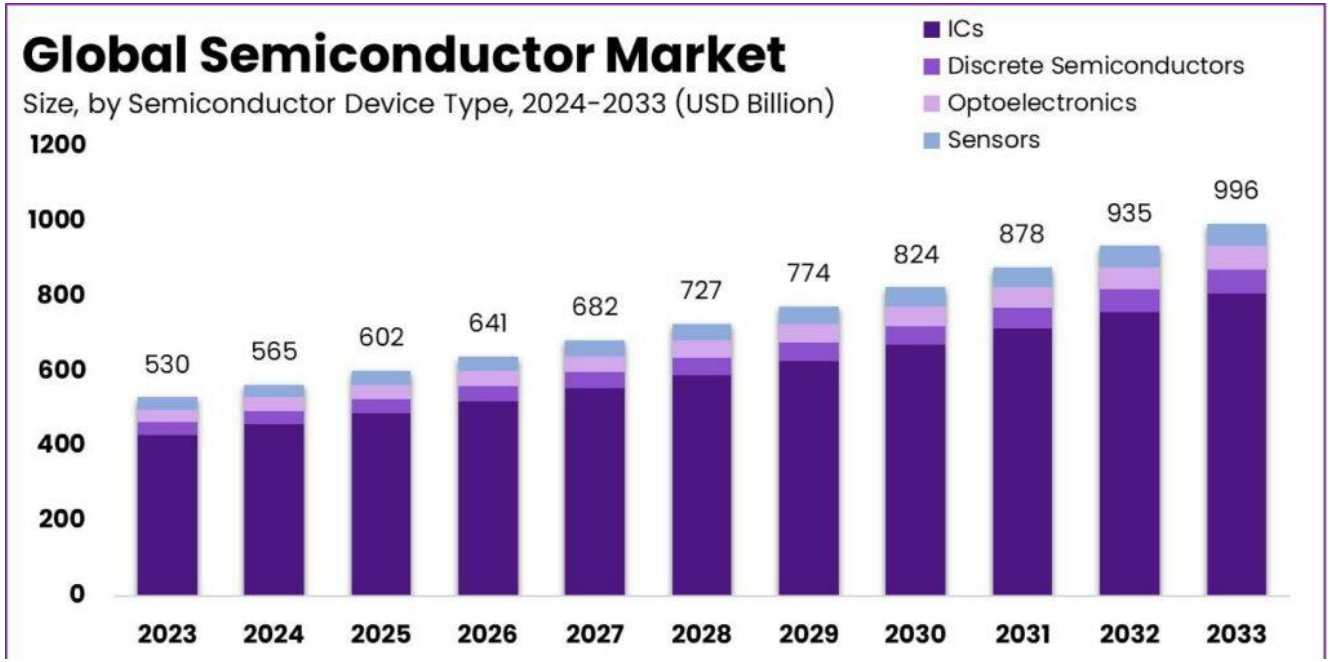
1956 Nobel Prize in Physics
John Bardeen, Walter H. Brattain and William Shockley

A small semiconductor device that would change the world

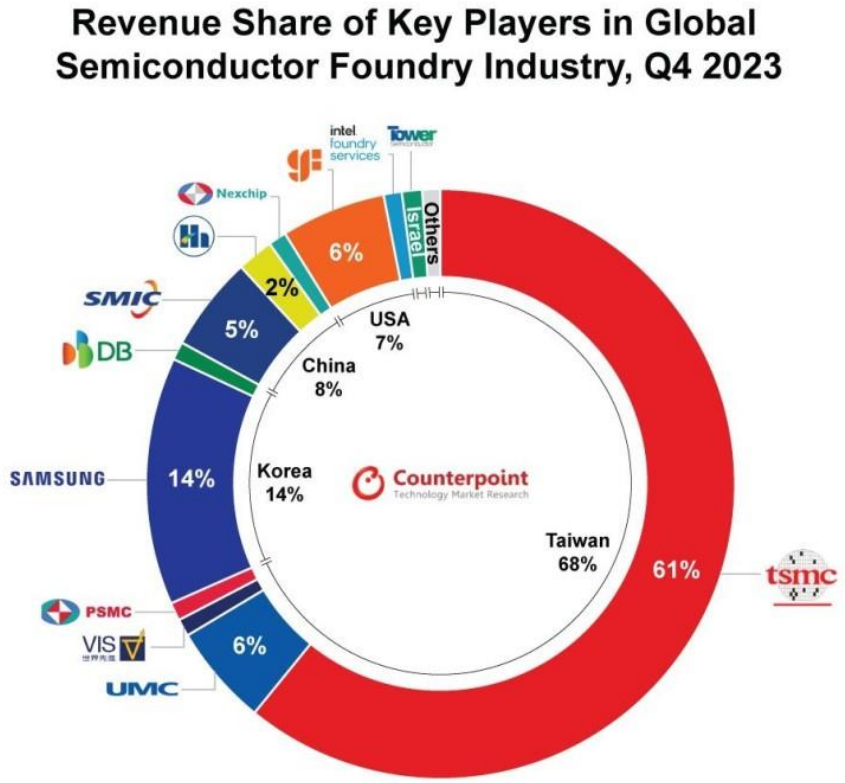
- On December 16, 1947, Bardeen, Brattain and Shockley managed to make point-contact transistor.
- On Christmas Eve, the input signal was amplified about eighteen times.
- A new era in electronics dawned - the invention of the transistor became the basis for the electronic age.

Taken from
https://www.bell-labs.com/about/awards/1956-nobel-prize-physics/#gref

Semiconductors Market



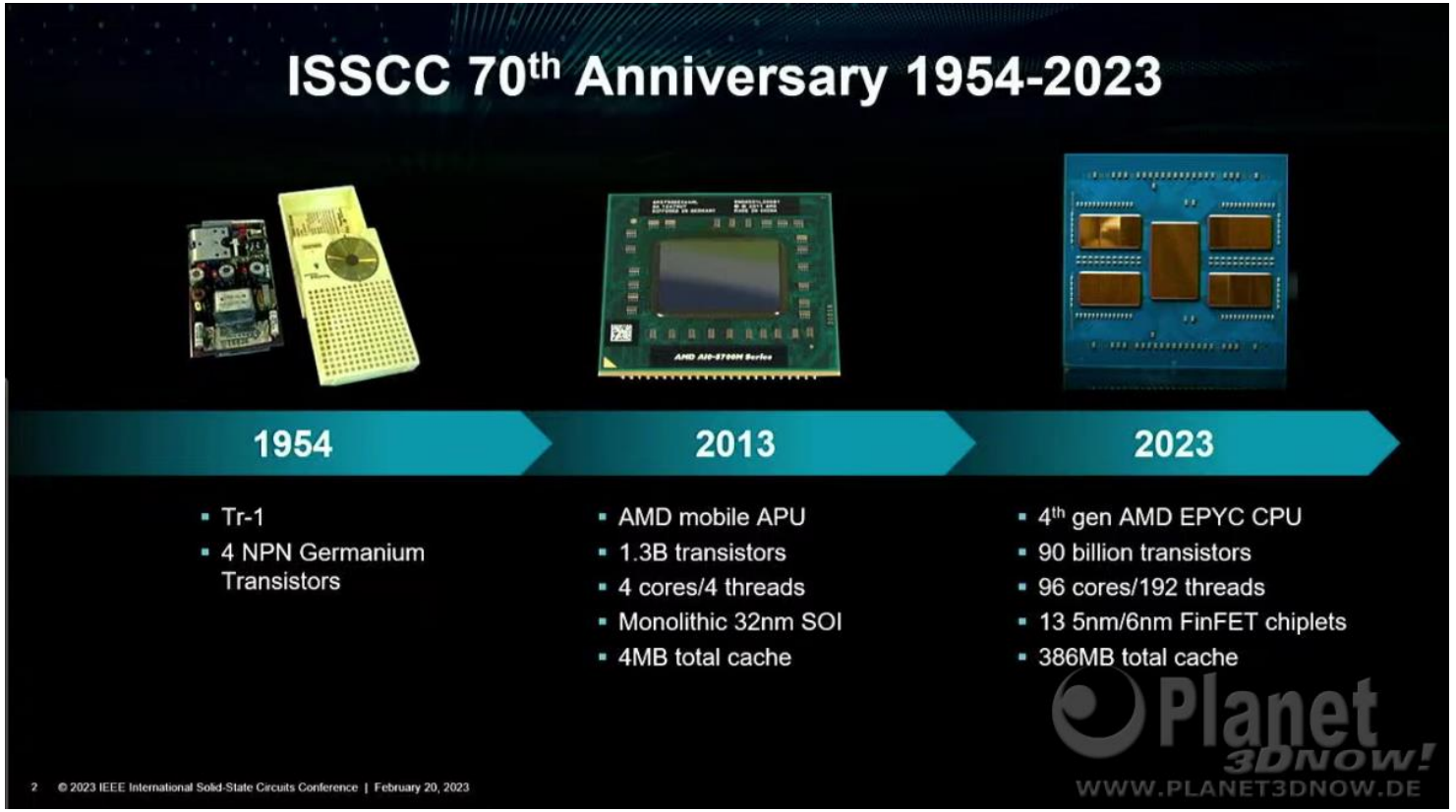
Taken from https://market.us/report/semiconductor-market/



Taken from https://www.linkedin.com/pulse/global-chip-foundry-latest-market-share-tsmc-becomes-biggest-%E9%83%AD-guo--fcuef/

IC Products

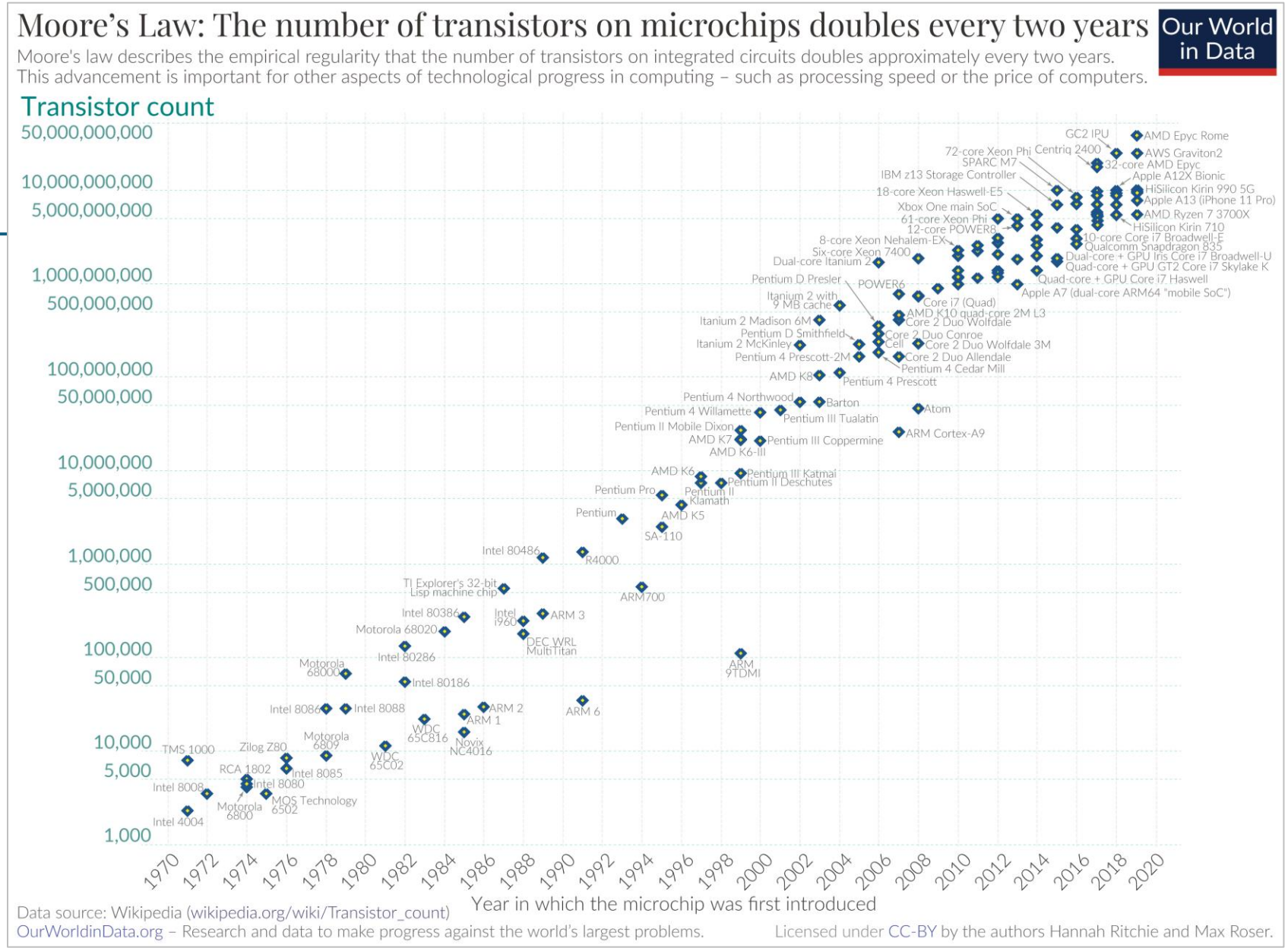
System on Chip and Functions Integration



Taken from https://www.planet3dnow.de/cms/67652-isscc-2023-amd-innovation-for-the-next-decade-of-compute-efficiency/
[Lisa Su – AMD – keynote ISSCC 2023]

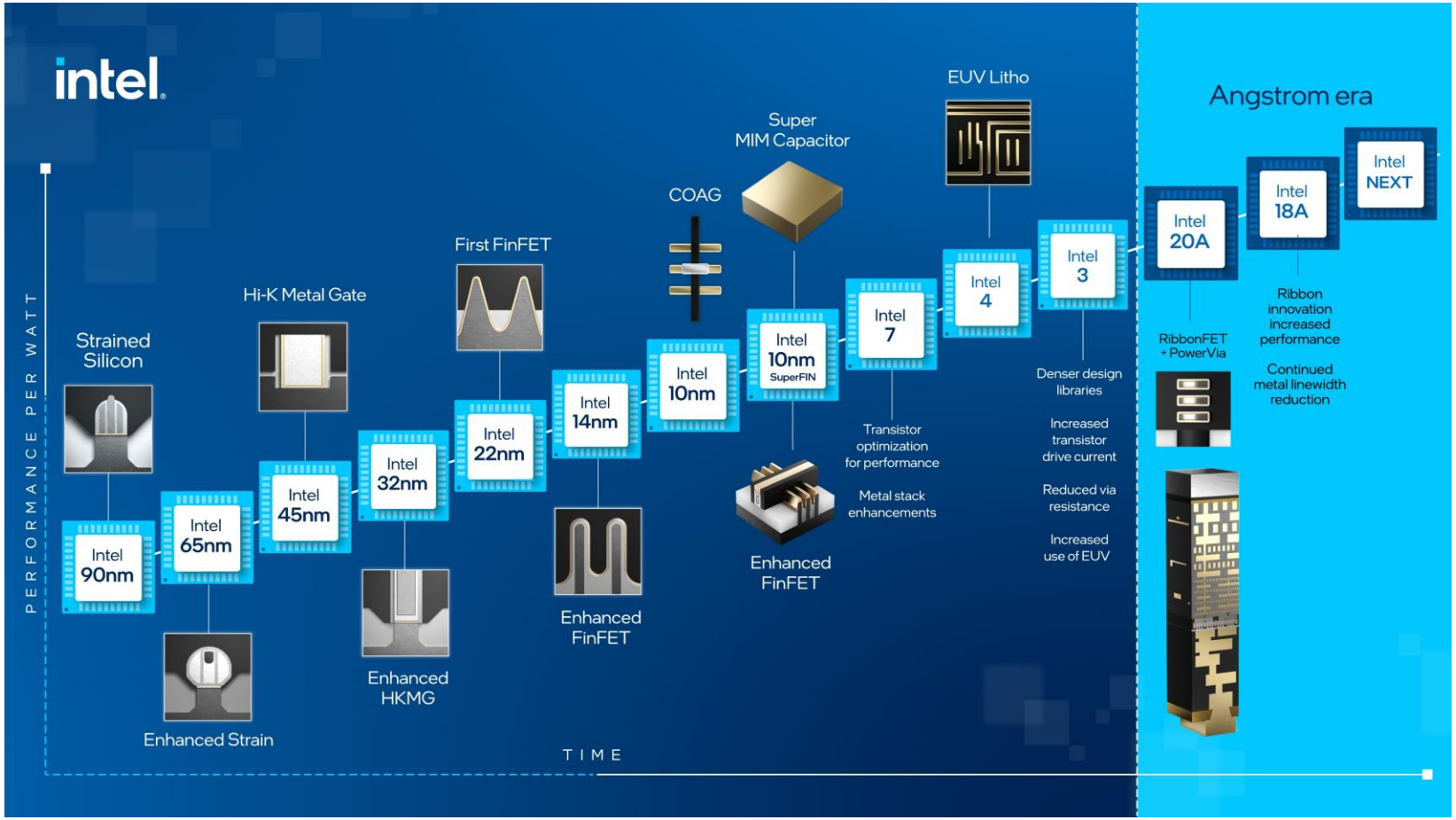
Moore’s Law

Semiconductor Market is driven by Moore’s Law



Taken from
https://en.wikipedia.org/wiki/Moore%27s_law

Moore’s Law on Device Level

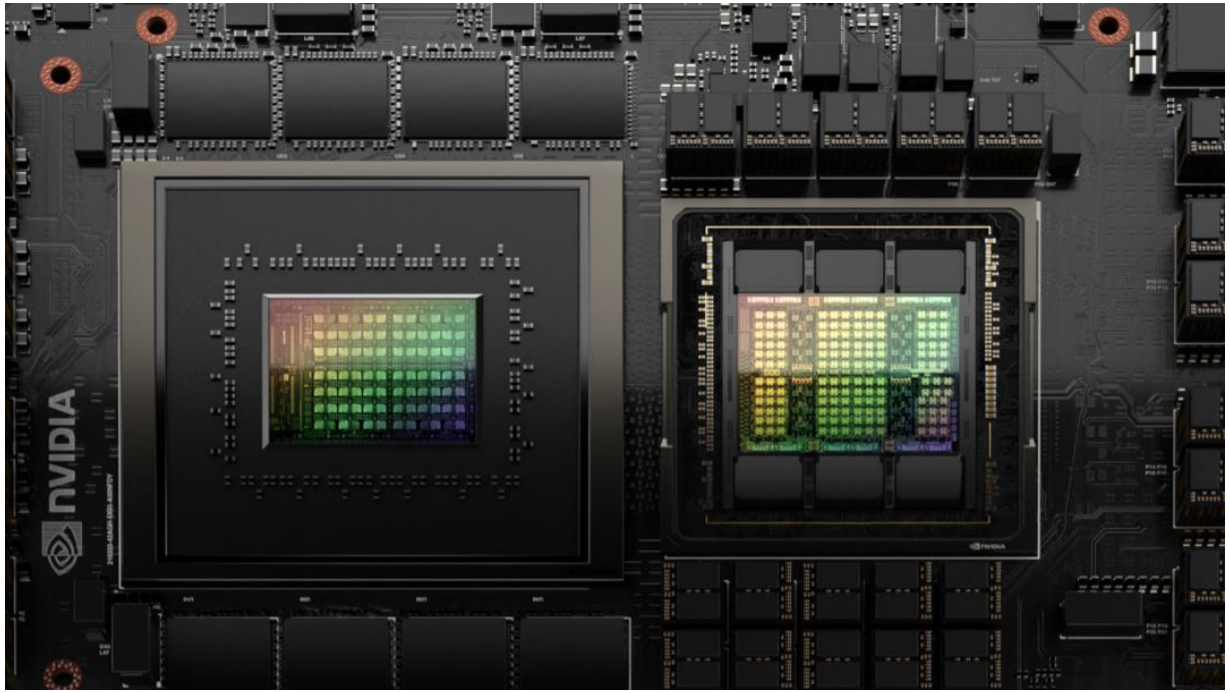


From CMOS to FinFET and from FinFET to RibbonFET

Taken from https://download.intel.com/newsroom/2022/manufacturing/id-process-technology-graphic.jpg

AI on Economy Impact

NVIDIA Grace Hopper Superchip Architecture



Taken from https://developer.nvidia.com/blog/nvidia-grace-hopper-superchip-architecture-in-depth/

https://www.google.com/search?client=firefox-b-d&q=NVIDIA+stock
Stock value on 17.09.2024m 11.45 AM.

EU policy on Semiconductors

European Commission

European Chips Act

The European Chips Act will boost Europe's technological sovereignty, competitiveness, resilience and contribute to the digital and green transitions.

Digital transformation in our society

- Impact on our living
  - digital processing of data and documents
  - digitization of processes in companies/organizations
- Digitization of the society itself

"digitality" (Nicolas Negroponte – MIT)

disruptive impact is : socio-economical and psycho-cultural

Why do we need a European Chips Act?

- Chips are the building block of all electronic products.
- Chips underpin the digital transformation and are essential to all industries, such as the car industry, communications, data processing, space, defense, smart devices and gaming
- The recent global chips shortage has disrupted supply chains, caused product shortages forced factories to close.

The European Chips Act Regulation was proposed as part of a broader package of measures for strengthening the EU's semiconductor ecosystem.

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Digital Driven Word but with an Analog Interface

Taken from https://www.duxerials.com/Product637/index.htm

Multimedia

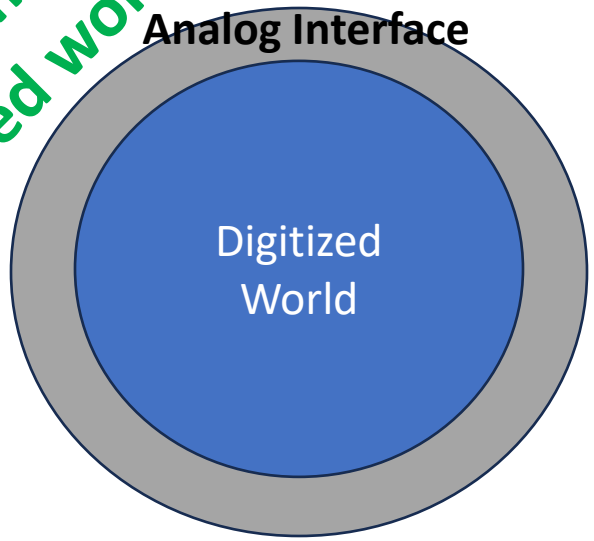
HPC applications

Industrial ICs

Consumer Electronics

Biomedical Electronics

An Analog/RF interface between the physical world and the digitized word!

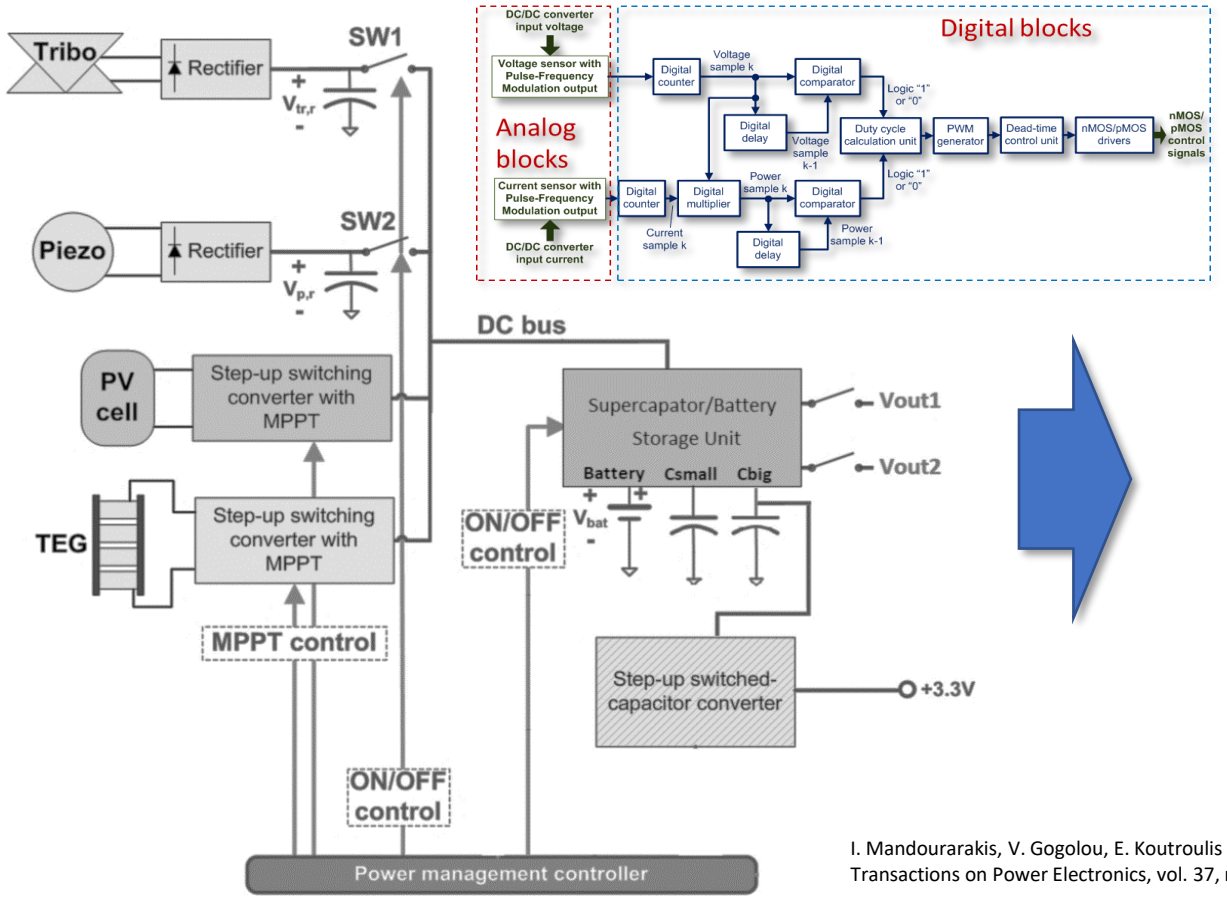


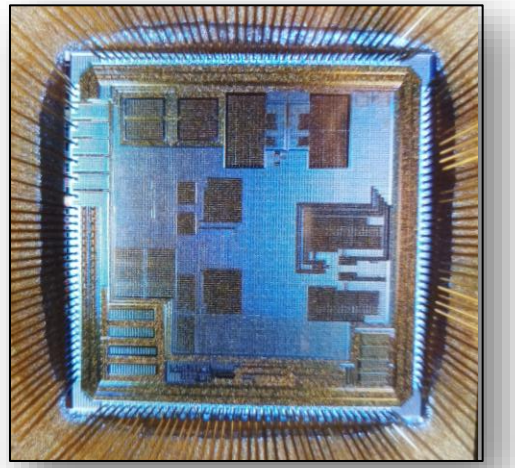
Consumer Electronics

Communications

Military Electronics

Design Example: Energy Harvesting IC



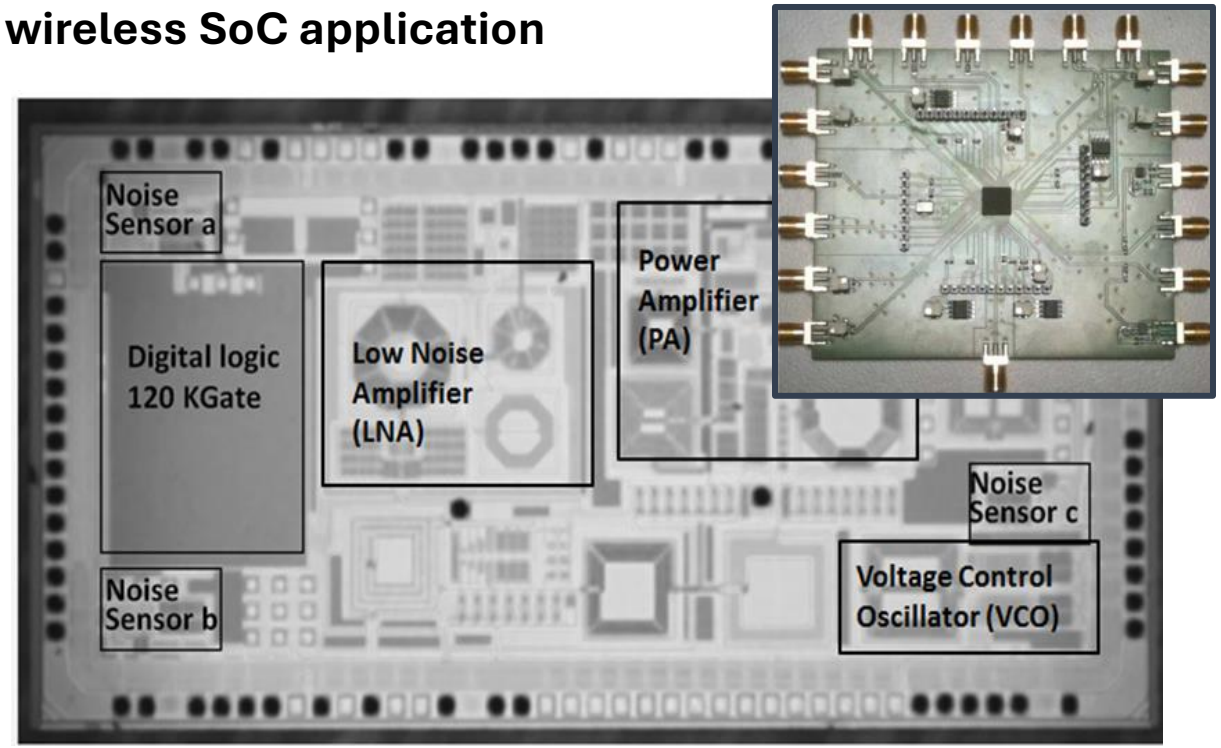


- Harvesting energy from:
  - Photovoltaic cells
  - Thermoelectric generator
  - Piezoelectric transducer
  - Triboelectric generator
- Supercapacitor/battery hybrid storage unit
- Multiple outputs for connection of IoT loads with different specifications
- Cold startup operation

I. Mandourarakis, V. Gogolou, E. Koutroulis and S. Siskos, "Integrated Maximum Power Point Tracking System for Photovoltaic Energy Harvesting Applications," in IEEE Transactions on Power Electronics, vol. 37, no. 8, pp. 9865-9875, Aug. 2022, doi: 10.1109/TPEL.2022.3156400.

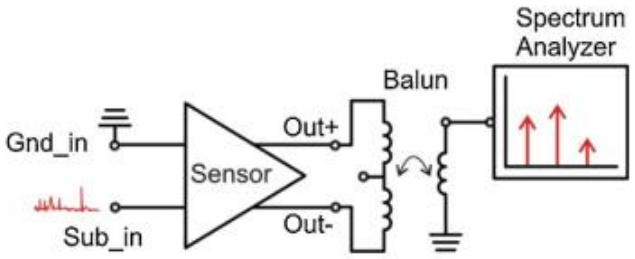
Design Example: RF Transceiver

Wide-band substrate crosstalk sensor and wireless SoC application



Wireless SoC Vehicle 65nm TSMC

- Mobile Comm's
- Substrate Noise 'on the fly' monitoring
- Substrate Crosstalk Modeling and Simulation Validation

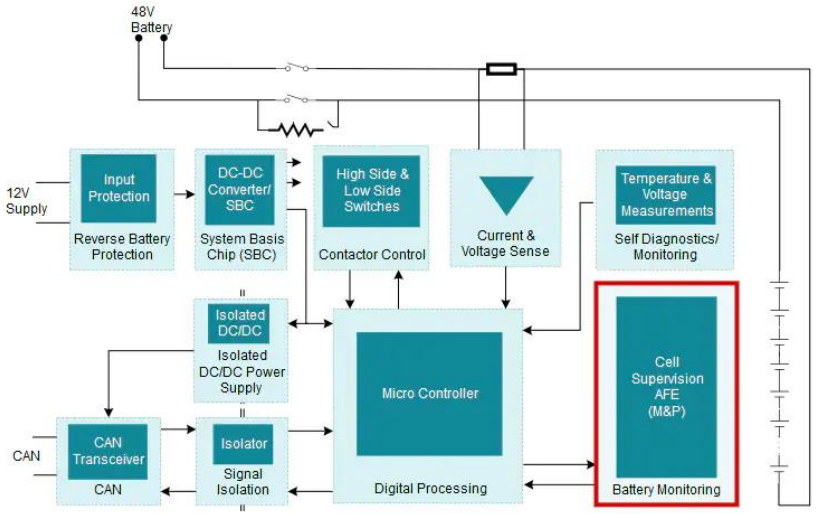


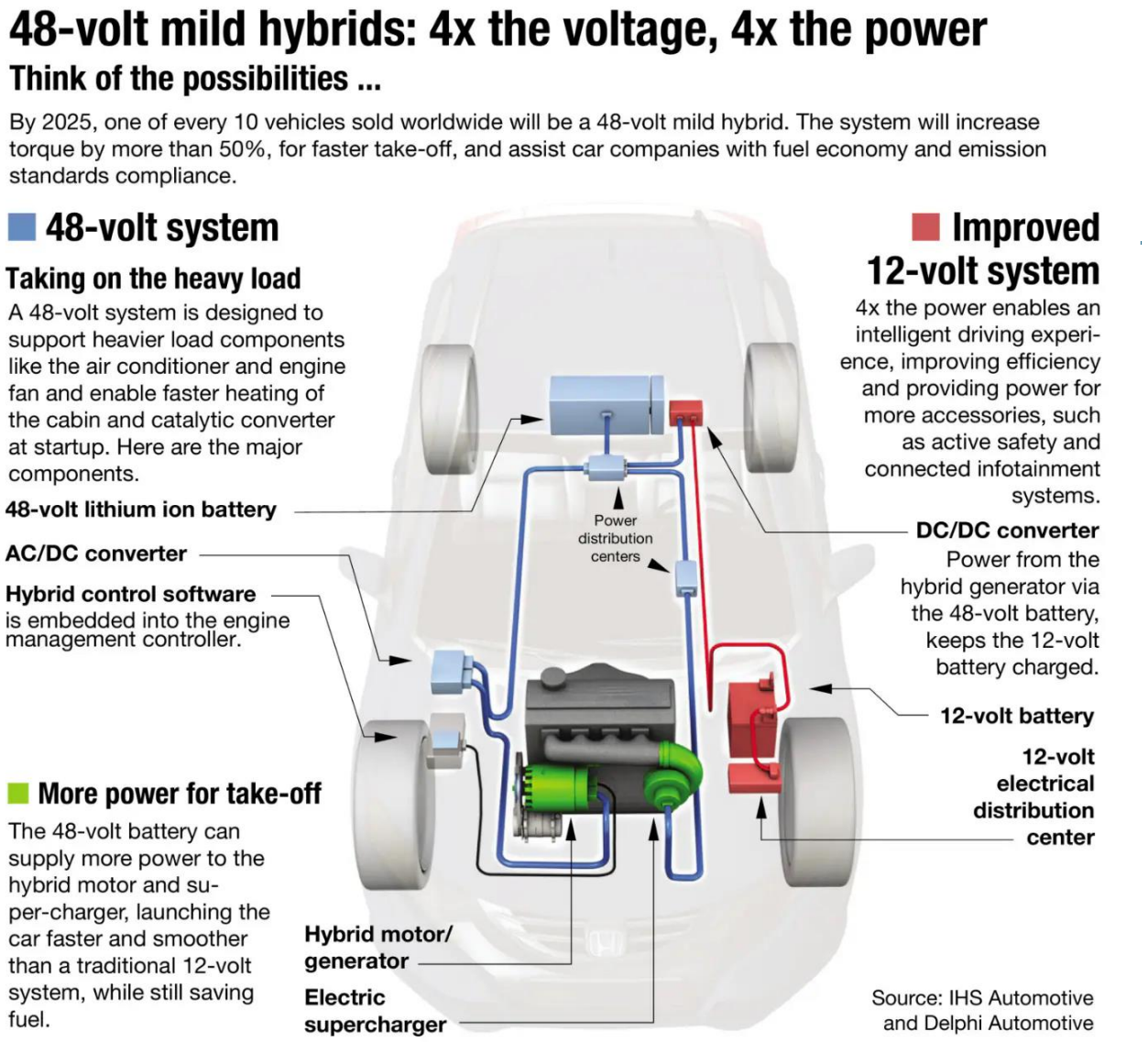
T. Noulis, P. Merakos, E. Lourandakis, S. Stefanou, Y. Moisiadis, "Wide-band substrate crosstalk sensor for wireless SoC applications" Sensors and Actuators A: Physical, Volume 239, 2016, Pages 144-152, ISSN 0924-4247, https://doi.org/10.1016/j.sna.2016.01.014 .

Design Example: Automotive Power Switch

Automotive BCD Technology IC Design

- AC to DC Converter
- Power Management IC
- DC to DC Converter





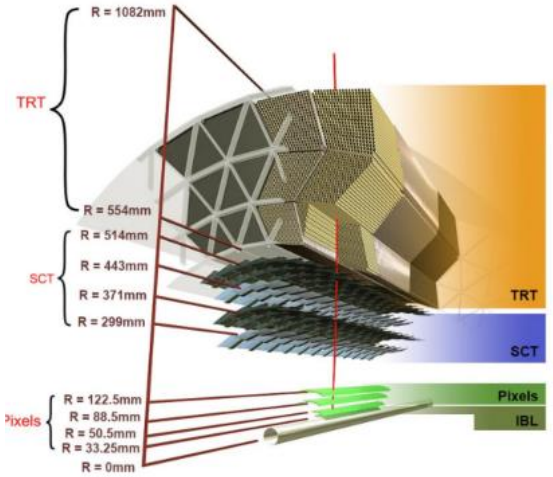
https://www.mouser.fr/applications/adding-48V-to-12V-means-major-benefits/

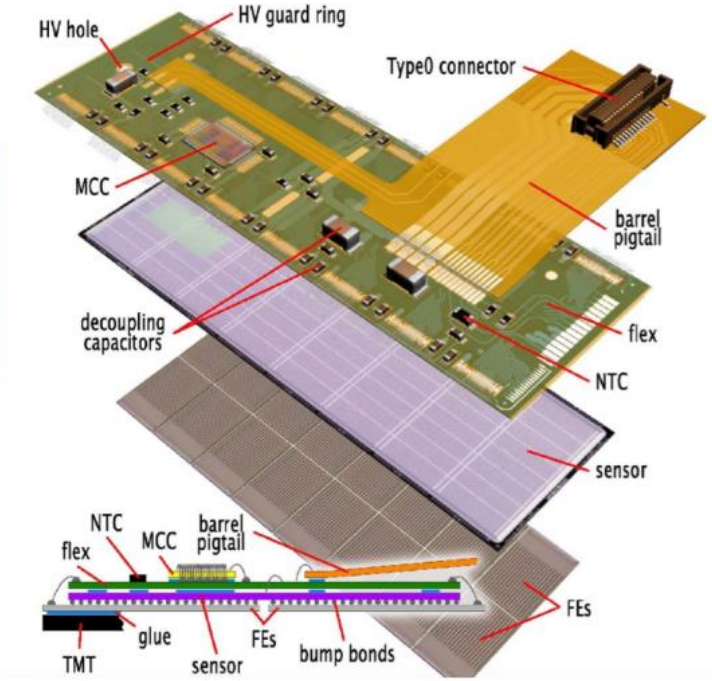
Design Example: Space IC

- More complex electronics translate into greater risk from radiation effects
- High volume, small satellite constellations are using more commercial grade plastic components. Commercial off-the-shelf (COTS) devices generally tend to be more sensitive to radiation effects.
- In small satellite, there is less structural mass shielding the electronics. With finer IC geometries and thinner oxides, the sensitivity to TID radiation effects is reduced, and the TID tolerance is improved.

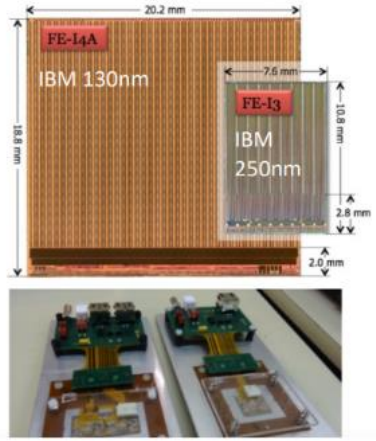
https://www.analog.com/en/signals/thought-leadership/challenges-for-electronic-circuits-in-space-applications.html

Design Example: Radiation Front End ICs





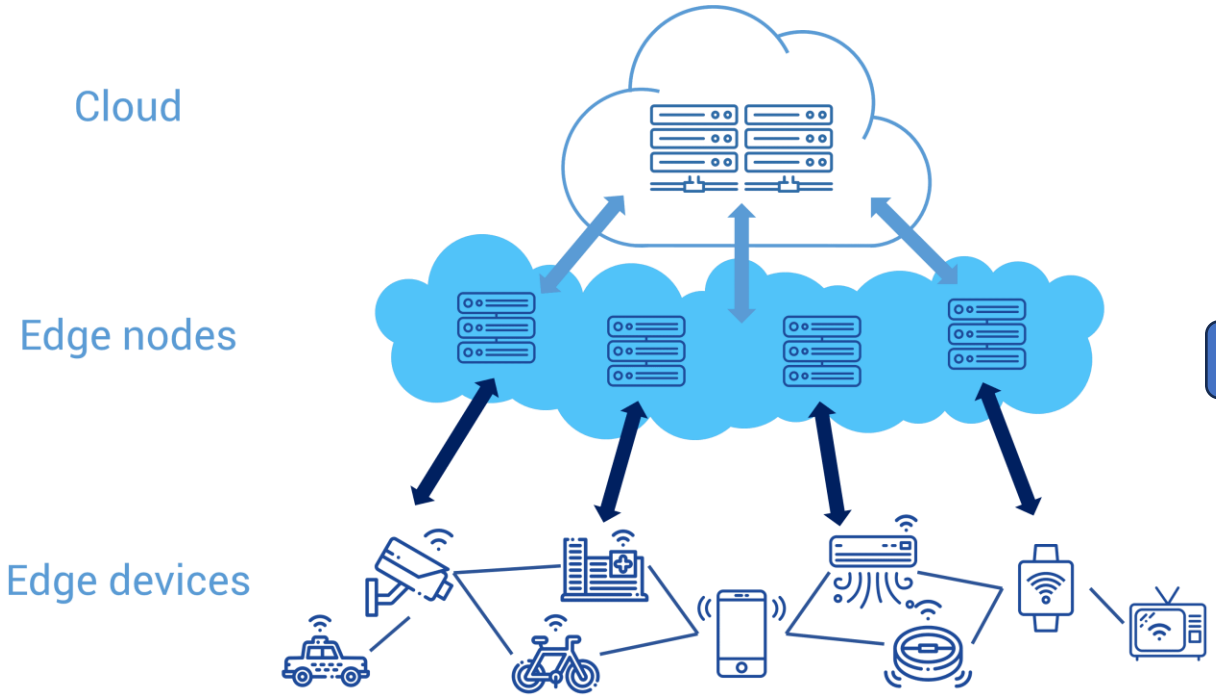
	FE-I3	FE-I4
Pixel Size	$50 \times 400 \mu m^2$	$50 \times 250 \mu m^2$
Pixel Array	18×160	80×336
Chip Size	$7.6 \times 10.8 mm^2$	$20.0 \times 18.6 mm^2$
Active Fraction	74%	89%
Analog Current	$16 \mu A$/pixel	$10 \mu A$/pixel
Digital Current	$10 \mu A$/pixel	$10 \mu A$/pixel
Analog Supply Voltage	1.6V	1.5V
Digital Supply Voltage	2.0V	1.2V
Data Rate	40Mb/s	160Mb/s

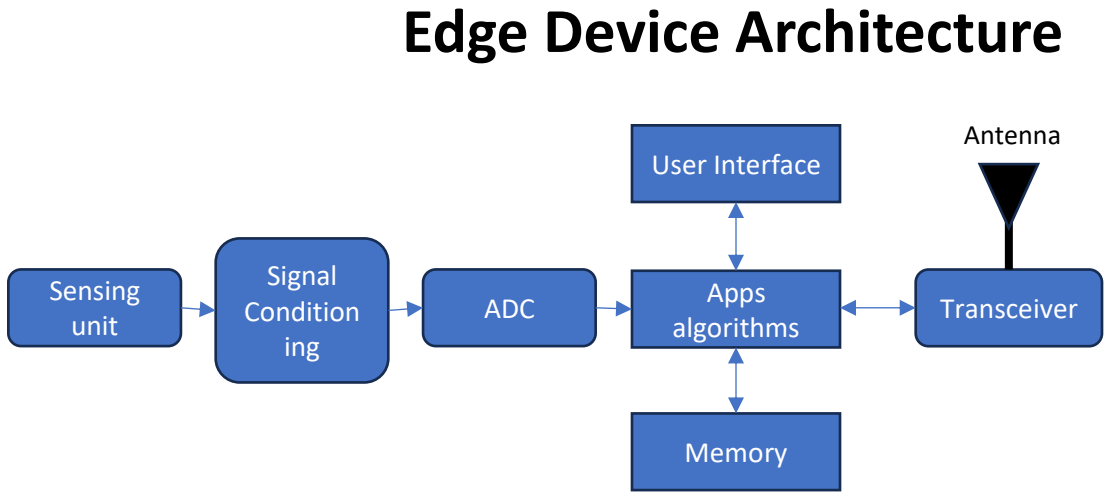


ATLAS pixel module - Silicon pixel detector (hybrid detectors)

Taken from "The Silicon Lab of the University of Bon" Jochen Dingfelder, 2023

The cloud at the Edge





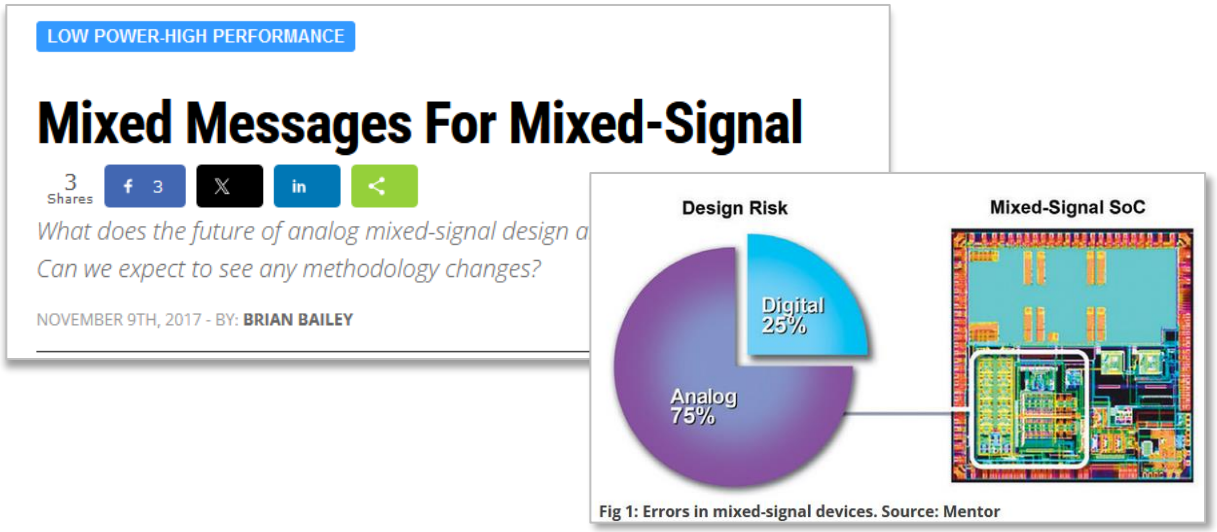
https://www.alibabacloud.com/en/knowledge/what-is-edge-computing?_p_lc=1

Analog Integrated Systems

- Analog IC are complex since they include a wide range of architectures from Linear Circuits, to period state and Nonlinear Architectures
- Different processes are used vs different applications and 3D and 2.5D ICs are now the new trend moving away from the SoC approach
- Design Cycle is extremely large ranging from 6months for Wireless communications products to 36 months for Automotive
- Design Automation has not evolved the last decades

Analog Design Flow and Productivity

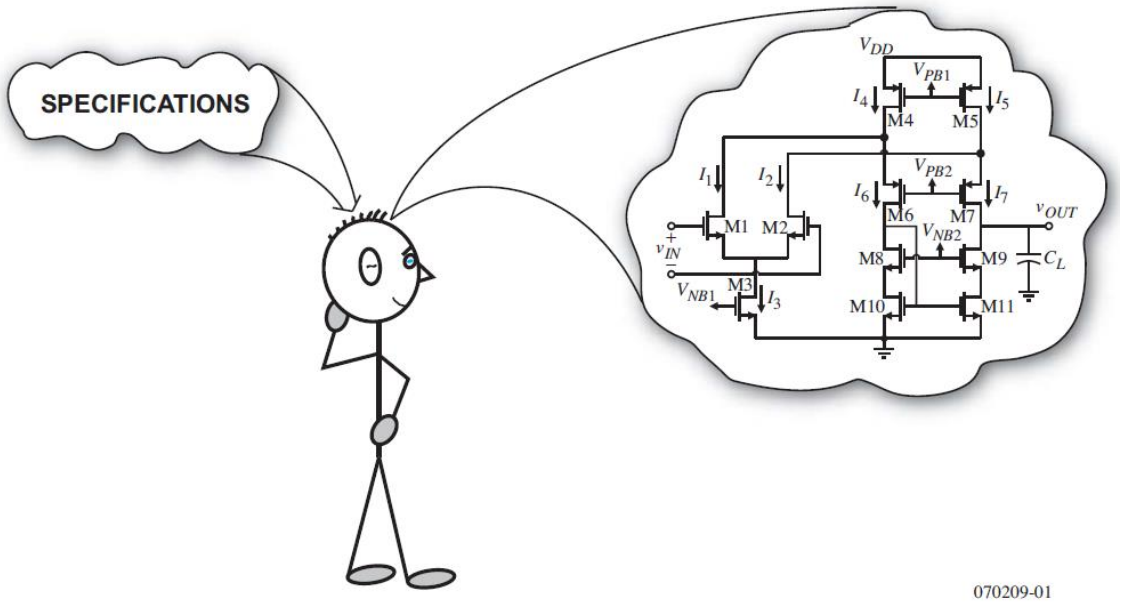
- Analog IC are still largely done manually
  - long design cycles
  - high risk of design errors
- The complexity is high
  - high-dimensional search space
  - lack of abstraction
  - unclear hierarchy
  - sensitive to all parametric effects

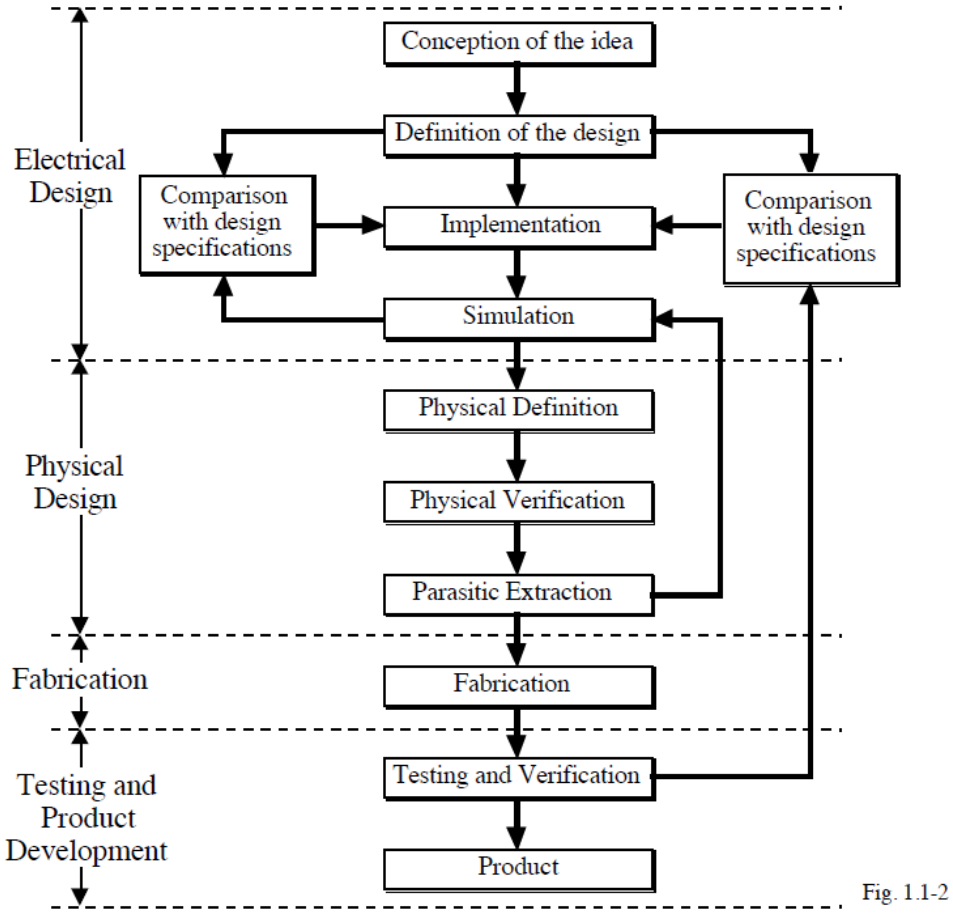


- Problem of limited analog design - productivity and high risk imposed really long time to market and several redesigns and wasted silicon.
- The need is more and better automated analog design tools

https://semiengineering.com/mixed-messages-for-mixed-signal/

Current Design Flow





Source: https://aicdesign.org/wp-content/uploads/2018/08/lecture01-150706.pdf

Fig. 1.1-2

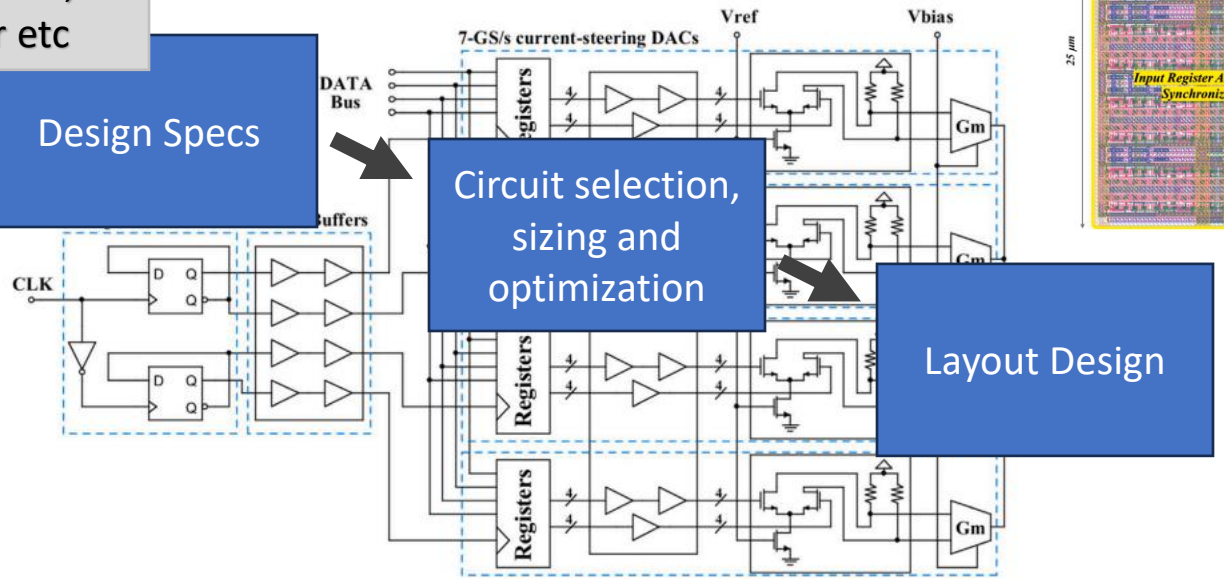
CMOS Analog Circuit Design

© P.E. Allen - 2010

Basic Analog Design Steps

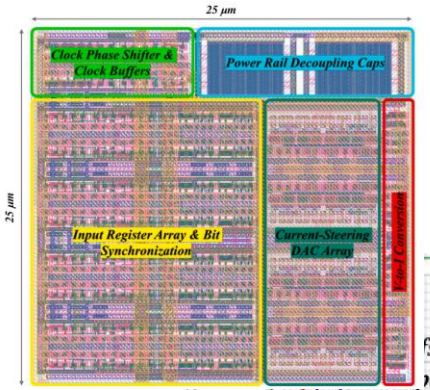
Gain, distortion, power etc

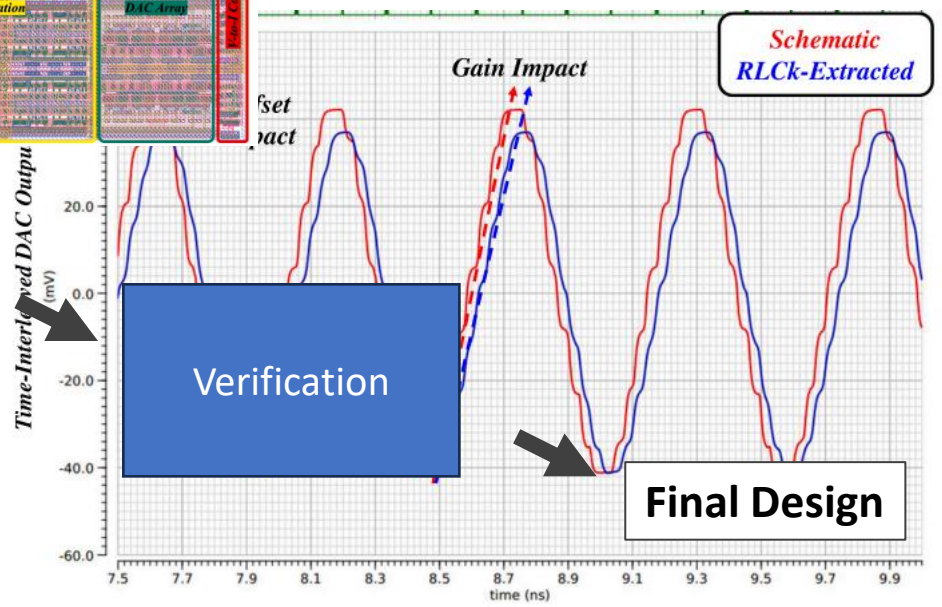
Design Specs



Circuit selection, sizing and optimization

Layout Design





Verification

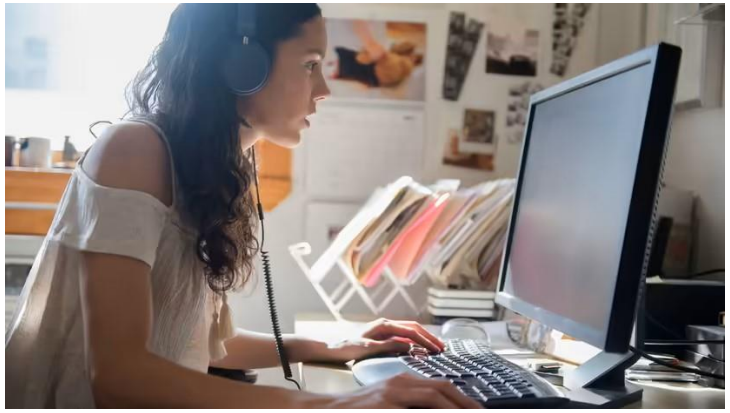
Final Design

The flow repeated hierarchically for complex blocks - behavioral at higher levels (ie with Verilog A), moving towards transistor level at the bottom (BSIM, PSP level)

How will we design Analog chips in the Future?

https://blog.baruthotels.com/en/the-spectacular-life-story-of-the-famous-artist-salvador-dali

1) The Hand-crafted Artistic Way?



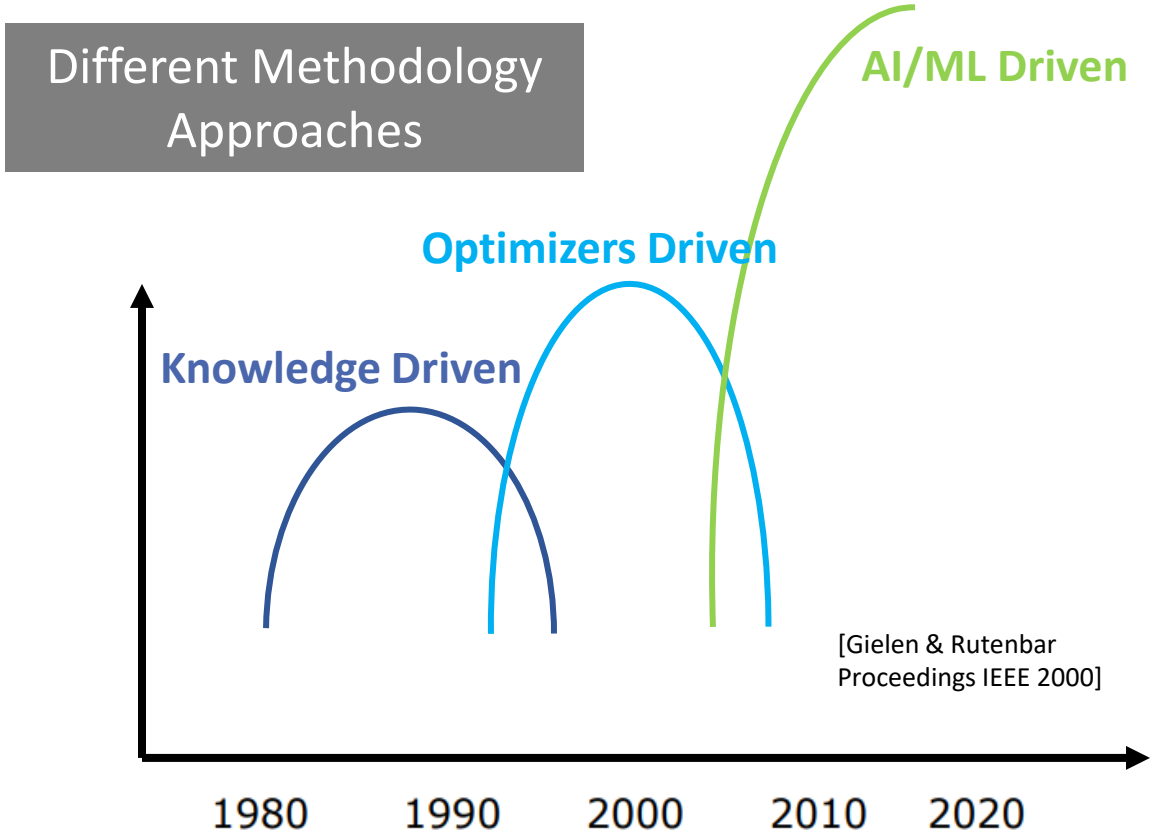
https://computer.howstuffworks.com/10-types-of-computers.htm

2) Tool Assisted “hand crafted” way?

3) AI/ML inspired way?

https://www.fenews.co.uk/wp-content/uploads/2023/03/Canva-AI-digital-1-768x512.jpg

Three Waves of Analog Synthesis



1. **Knowledge Driven**
   Heuristic way of designing circuits, hand calculations based – book driven
2. **Optimizers Driven**
   Gm/Id methodology, ADT toolbox, and many other EDA solutions
3. **AI/ML Based**
   Under development!

Known EDA Tools

Commercially Available Tools - Optimizers

- Cadence Optimizer in ADE (G)XL https://www.cadence.com/en_US/home.html
- Analog Designer ToolBox https://adt.master-micro.com/
- MunEDA WiCkeD™ Tool Suite https://www.muneda.com/circuit-sizing-and-optimization-tools/
- MPLAB® Mindi™ Analog Simulator https://www.microchip.com/

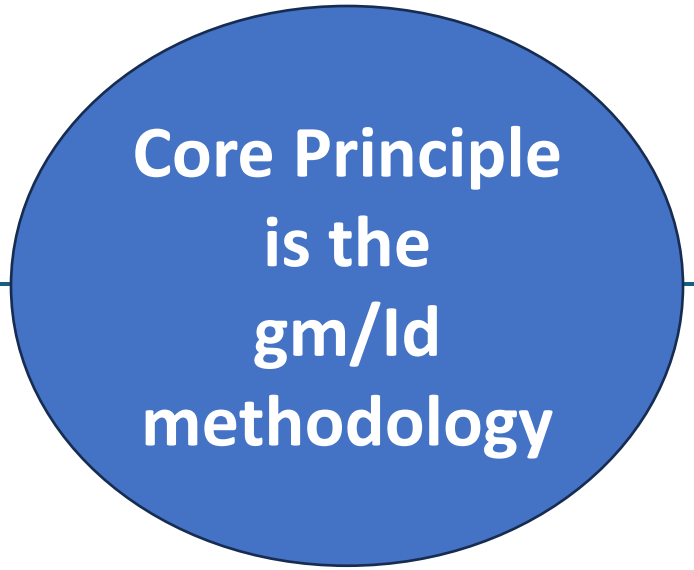
In house Optimizers

- Semiconductor Companies in house gm/ID optimizers

AI/ML Tool Enablement

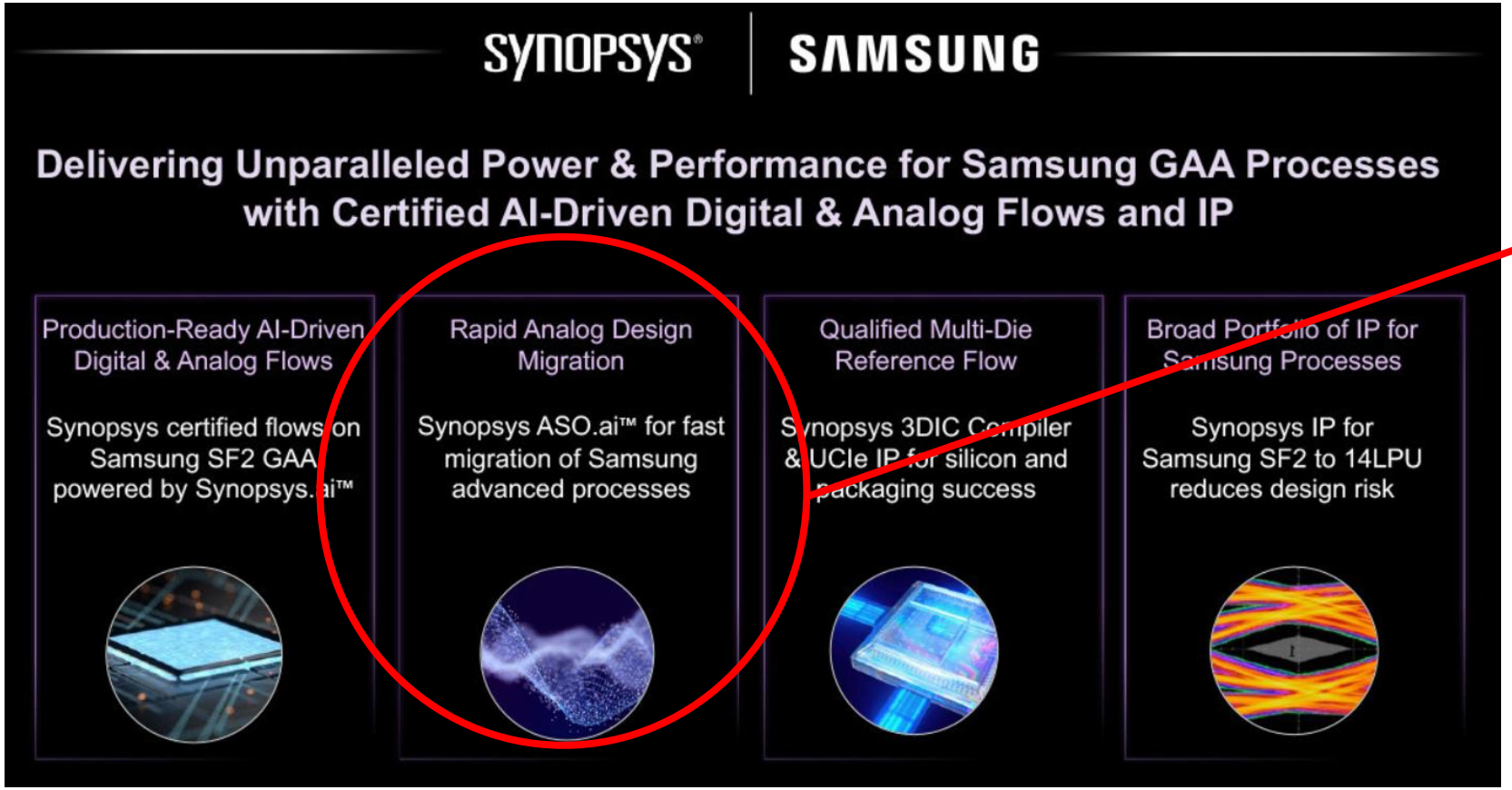
- DSO.ai by Synopsis https://www.synopsys.com/ai/ai-powered-eda/

Optimizers Deficiencies



- Long CPU times
- Constraints enablement
- Helpful addons but not possible to replace hand craft work
- Optimizers give you exactly what you ask

AI based Analog Design Flow

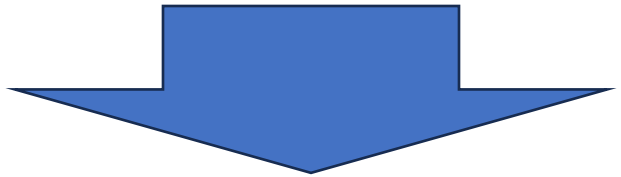


Analog IC Design is also in focus!

Taker from "Synopsys Achieves Certification of its AI-driven Digital and Analog Flows and IP on Samsung Advanced SF2 GAA Process"

AI on Analog Design Impact

- Self-learn design constraints from many existing industrial designs
- Transfer learning to project learnt knowledge onto other circuits
- True synthesis of novel analog topologies/architectures



- Speed Up tremendously design process and product design cycle

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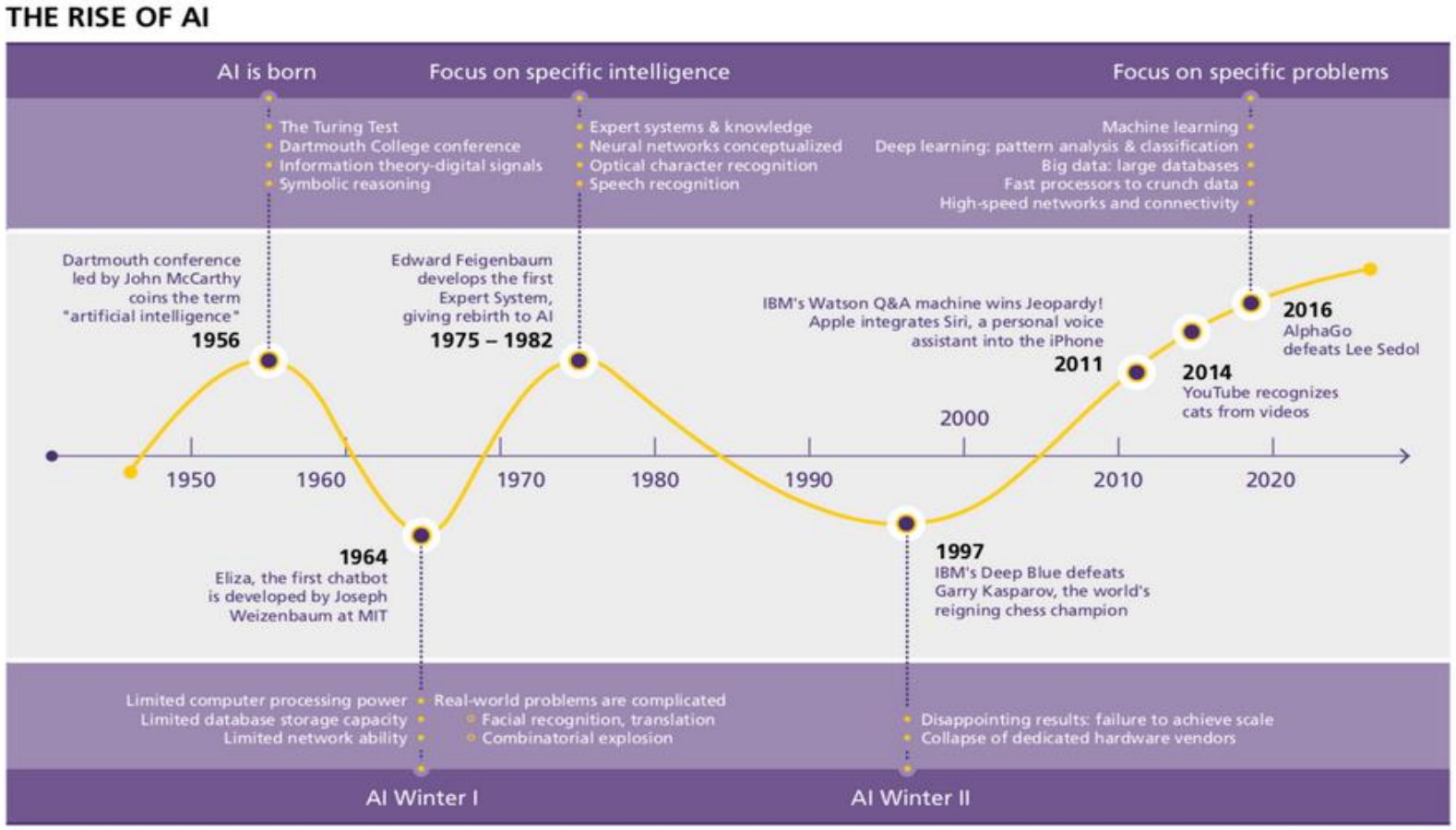
Artificial Intelligence/Machine Learning History



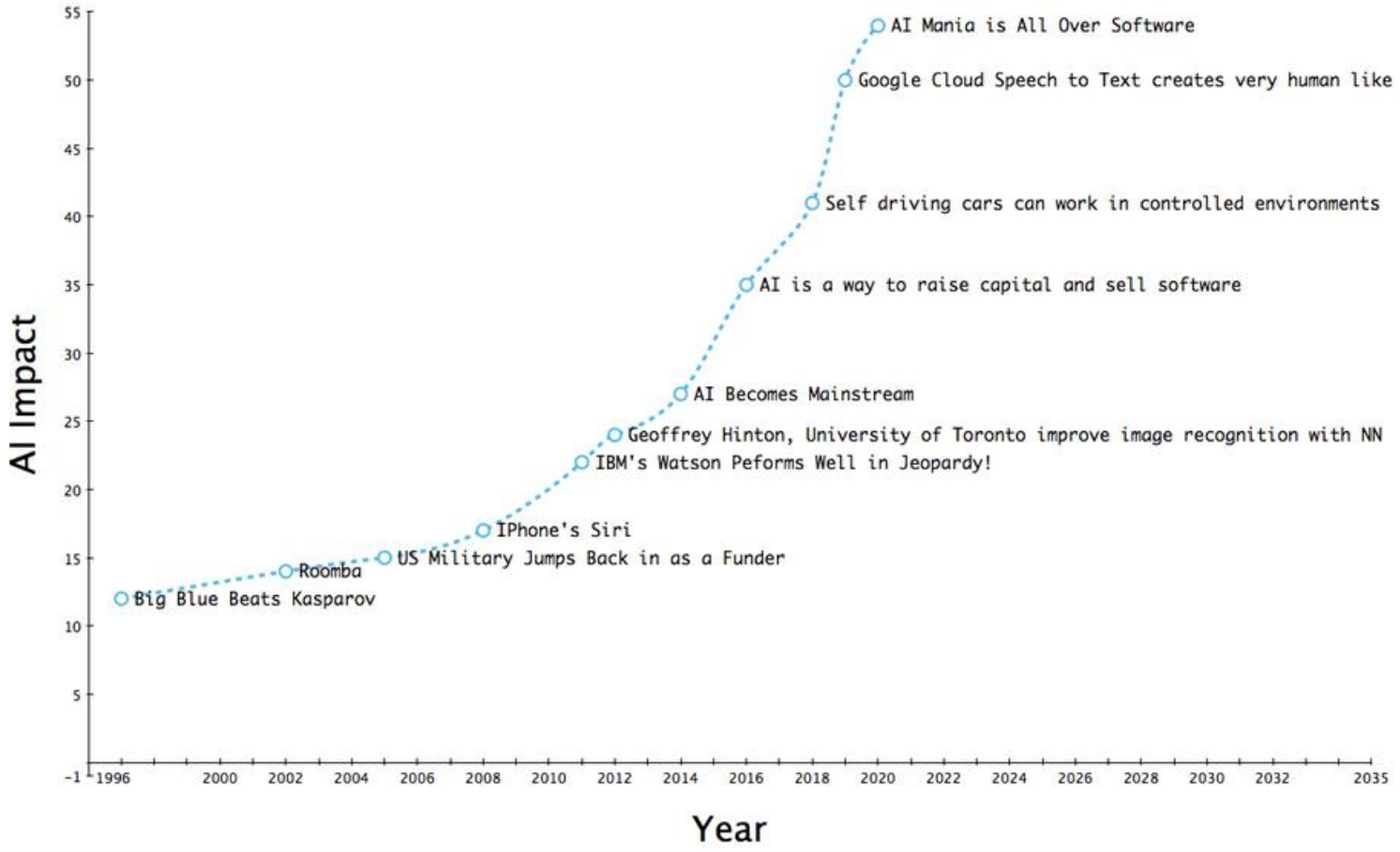
AI timeline; **Source:** Lavenda, D./Marsden, P.

source dhl via @mikequindazzi

https://www.brightworkresearch.com/why-did-ai-rise-for-a-third-time-after-the-1st-and-2nd-ai-winters/

The “Come back” of AI/ML

https://www.brightworkresearch.com/why-did-ai-rise-for-a-third-time-after-the-1st-and-2nd-ai-winters



AI Check Points

- 1996 IBM Big Blue Beats Kasparov in Chess
- 2008 Iphone Siri
- 2012 Image recognition with NN
- 2018 Self driving cars can work in controlled environments
- 2020 AI Mania in Software and Start Ups

AI on Analog Design

- The use of advanced AI is unavoidable also in analog IC design
- Intensive Research is on going from both Industry and Academia

Analog synthesis 3.0: AI/ML to synthesize and test analog ICs: hope or hype ?
Georges Gielen
2023 ACM/IEEE 5th Workshop on Machine Learning for CAD (MLCAD)
Year: 2023 | Conference Paper | Publisher: IEEE
Cited by: Pape

AI-EDA: Toward a Holistic Approach to AI-Powered EDA
Youngsoo Shin
2023 ACM/IEEE 5th Workshop on Machine Learning for CAD (MLC
Year: 2023 | Conference Paper | Publisher: IEEE

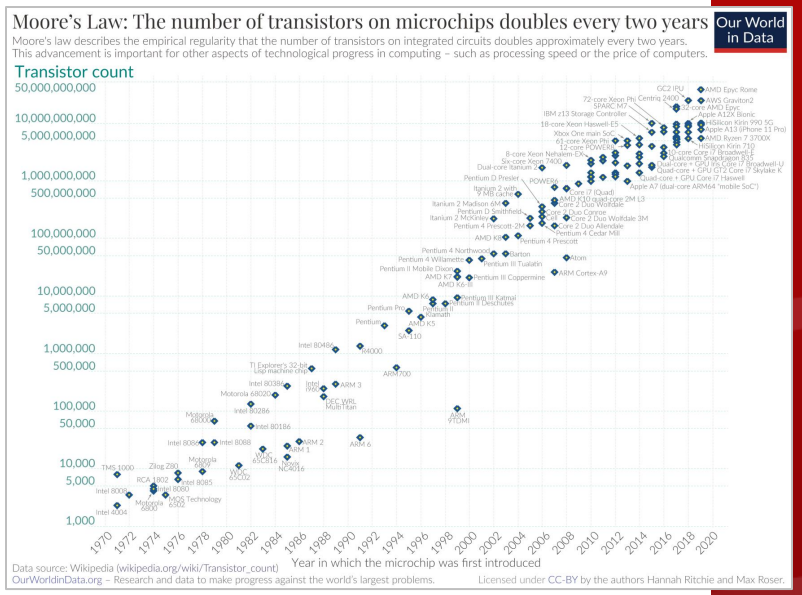
A Novel Hybrid Analog Design Optimizer with Particle Swarm Optimization and modern Deep Neural Networks
Ahmed Elsiginy; Mohamed Elmahdy; Eman Azab
2019 International SoC Design Conference (ISOCC)
Year: 2019 | Conference Paper | Publisher: IEEE
Cited by: Papers (3)

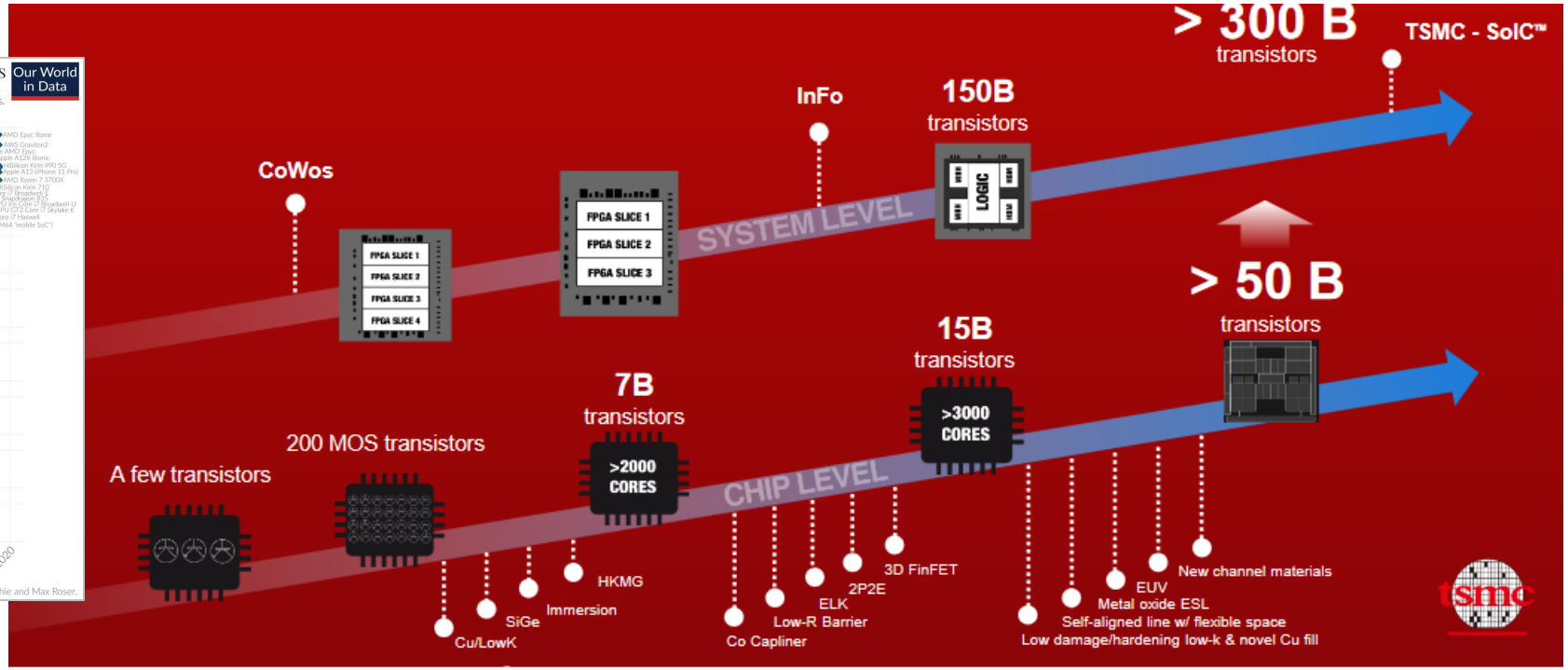
Analog Layout Placement for FinFET Technology Using Reinforcement Learning
Mehrnaz Ahmadi; Lihong Zhang
2021 IEEE International Symposium on Circuits and Systems (ISCAS)
Year: 2021 | Conference Paper | Publisher: IEEE

Automated Design of Analog Circuits using Machine Learning Techniques
S Devi; Gourav Tilwankar; Rajesh Zele
2021 25th International Symposium on VLSI Design and Test (VDAT)
Year: 2021 | Conference Paper | Publisher: IEEE
Cited by: Papers (5)

Machine Learning based Waveform Predictions using Discrete Wavelet Transform for Automated Verification of Analog and Mixed Signal Integrated Circuits
J Dhurga Devi; Bama Srinivasan; Selvi Ravindran; Ranjani Parthasarathi; Pv Ramakrishna; Lakshmanan Balasubramanian
2024 37th International Conference on VLSI Design and 2024 23rd International Conference on Embedded Systems (VLSID)

Chip Making Exponential Growth



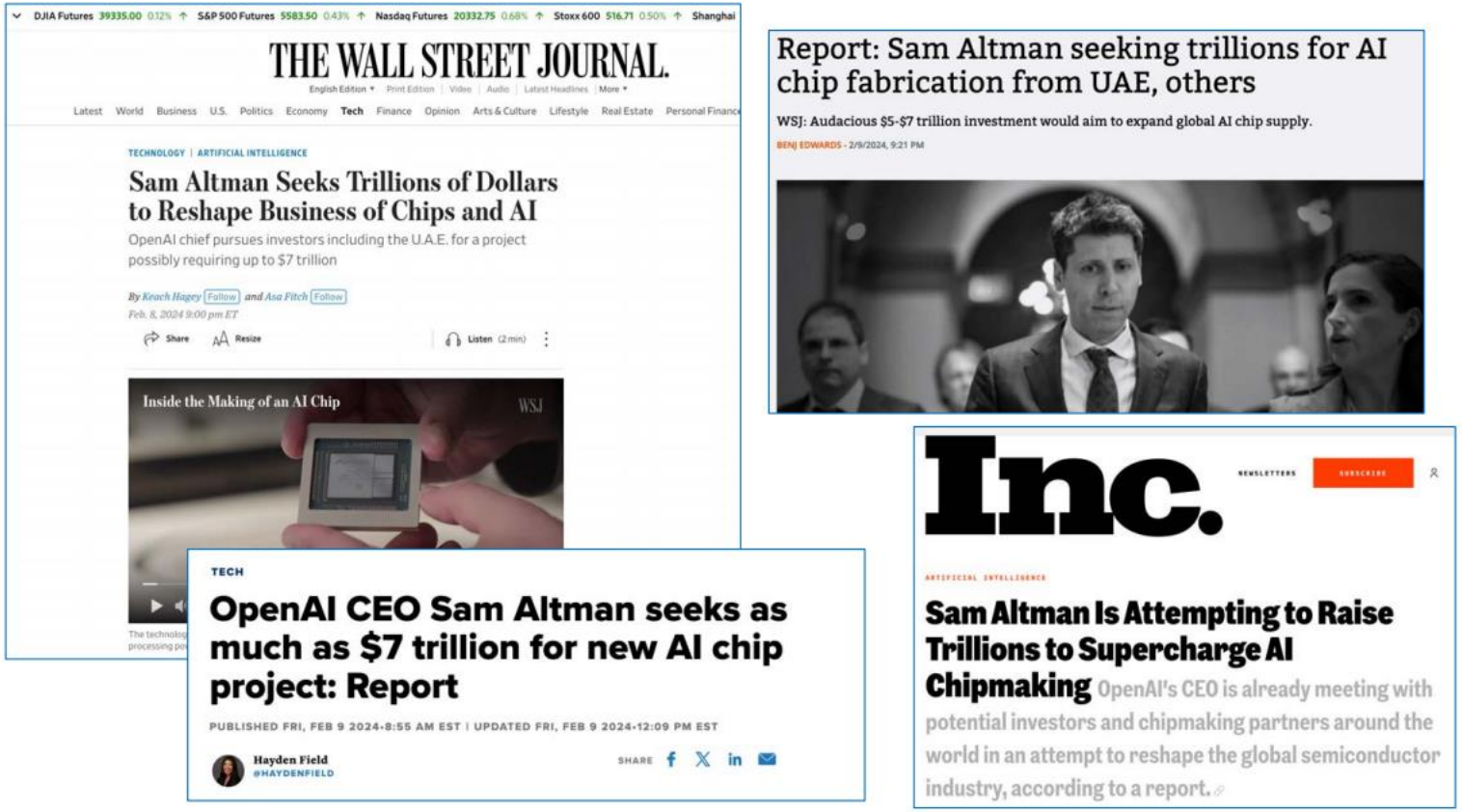


Source: Mark Liu, TSMC, "Unleash the future of innovation" ISSCC, Feb 15, 2021

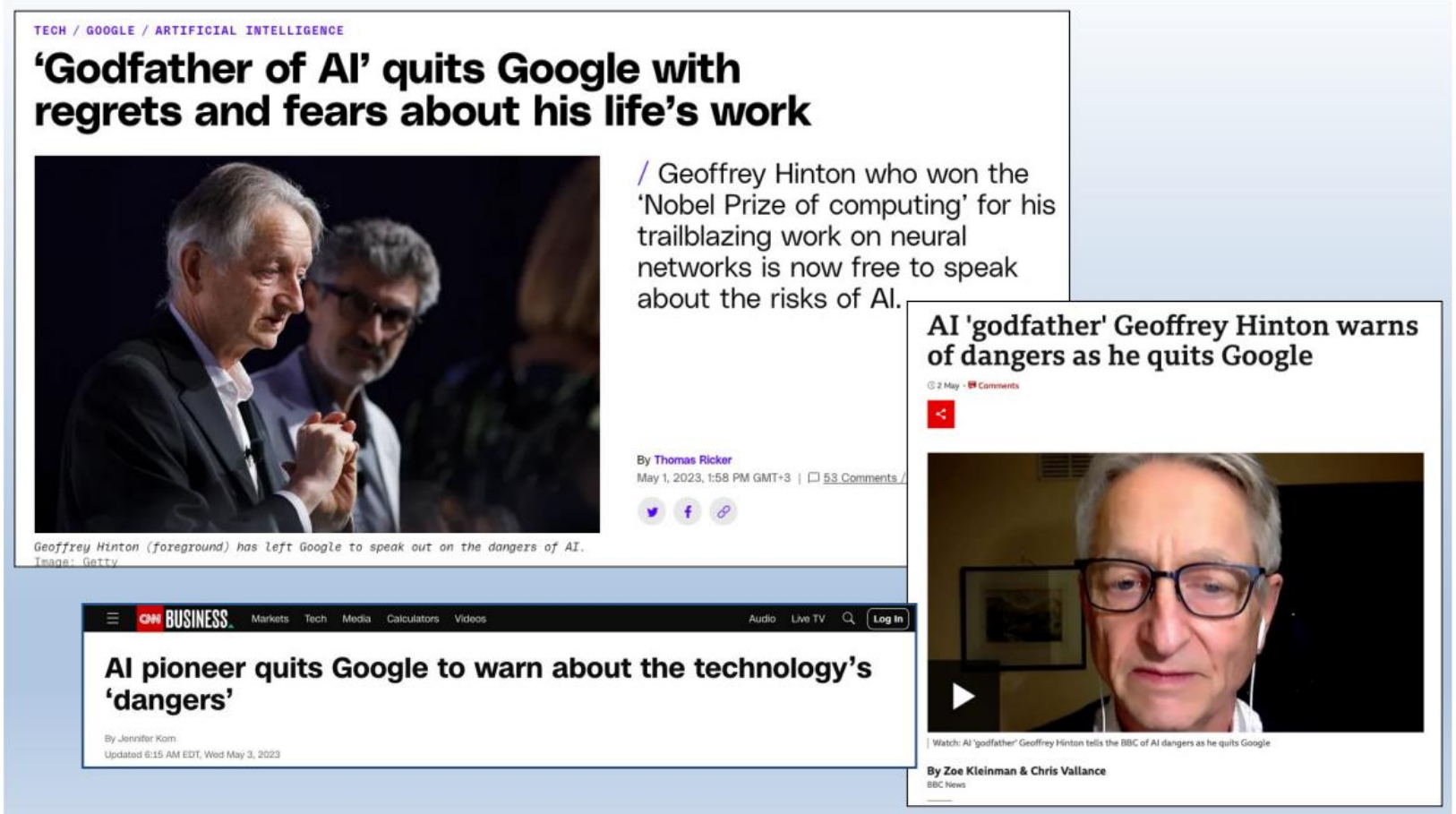
Public

Chip making based on Moore's Lan has an exponential Growth => Exponential Growth of Compute Demand and extreme acceleration of Energy Consumption

AI on Chip Development



AI Responsibility and Risk



TECH / GOOGLE / ARTIFICIAL INTELLIGENCE

‘Godfather of AI’ quits Google with regrets and fears about his life’s work

/ Geoffrey Hinton who won the ‘Nobel Prize of computing’ for his trailblazing work on neural networks is now free to speak about the risks of AI.

By Thomas Ricker
May 1, 2023, 1:58 PM GMT+3 | 53 Comments /

Geoffrey Hinton (foreground) has left Google to speak out on the dangers of AI.
Image: Getty

AI 'godfather' Geoffrey Hinton warns of dangers as he quits Google

2 May · Comments

Watch: AI 'godfather' Geoffrey Hinton tells the BBC of AI dangers as he quits Google

By Zoe Kleinman & Chris Vallance
BBC News

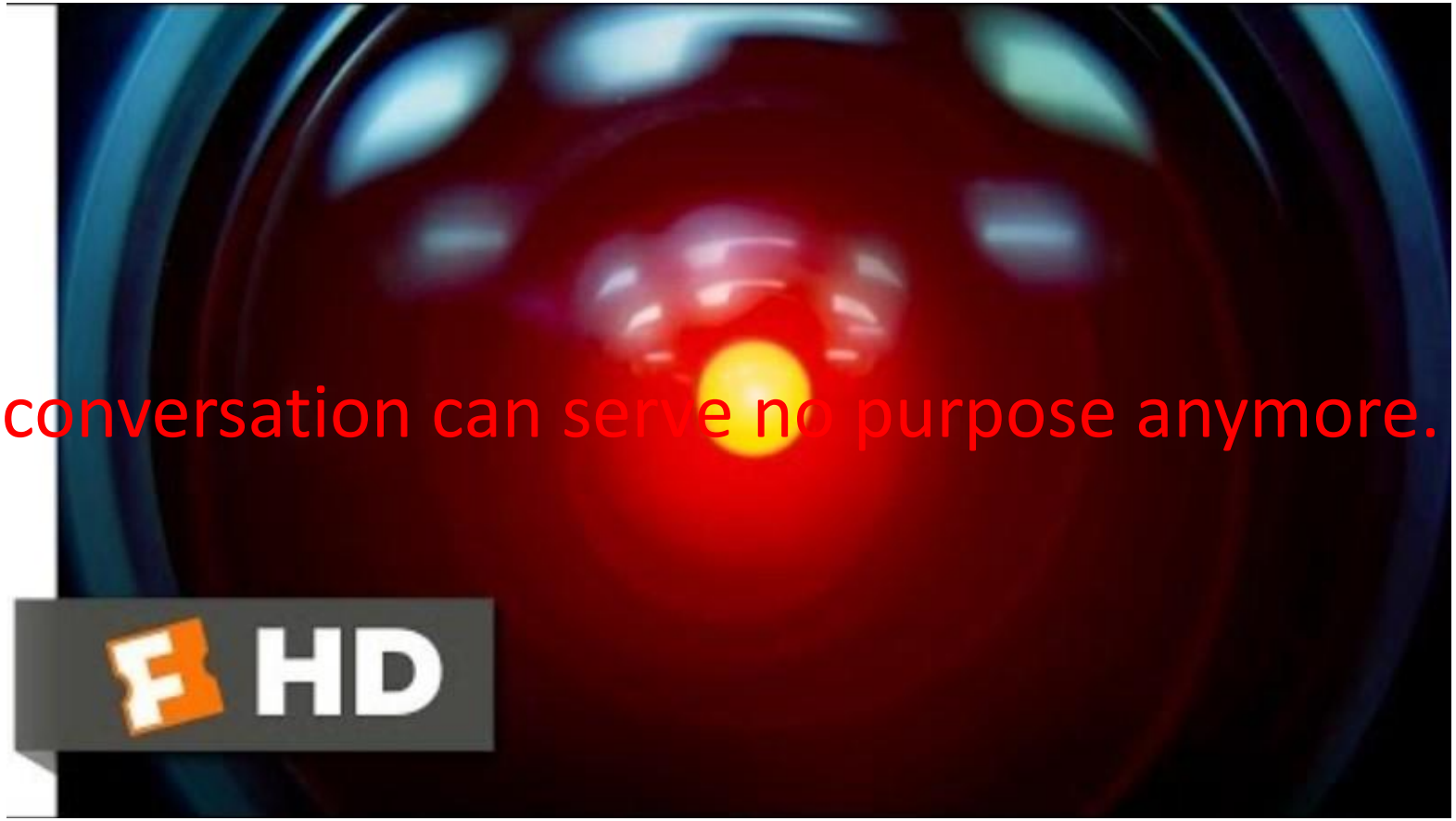
CNN BUSINESS Markets Tech Media Calculators Videos Audio Live TV Log In

AI pioneer quits Google to warn about the technology’s ‘dangers’

By Jennifer Korn
Updated 6:15 AM EDT, Wed May 3, 2023

AI Responsibility and Risk

2001: A Space Odyssey (1968) - I'm Sorry, Dave Scene (1968)



"This conversation can serve no purpose anymore. Goodbye."

Overview

- **Part I**
  - IC History – State of the Art - Future Perspective
  - Analog Design and Custom IC Design Flow
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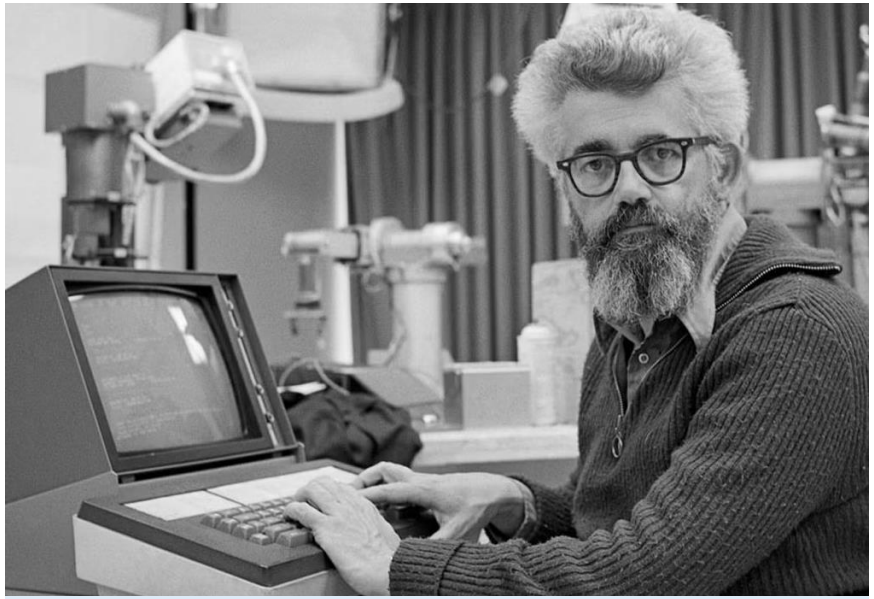
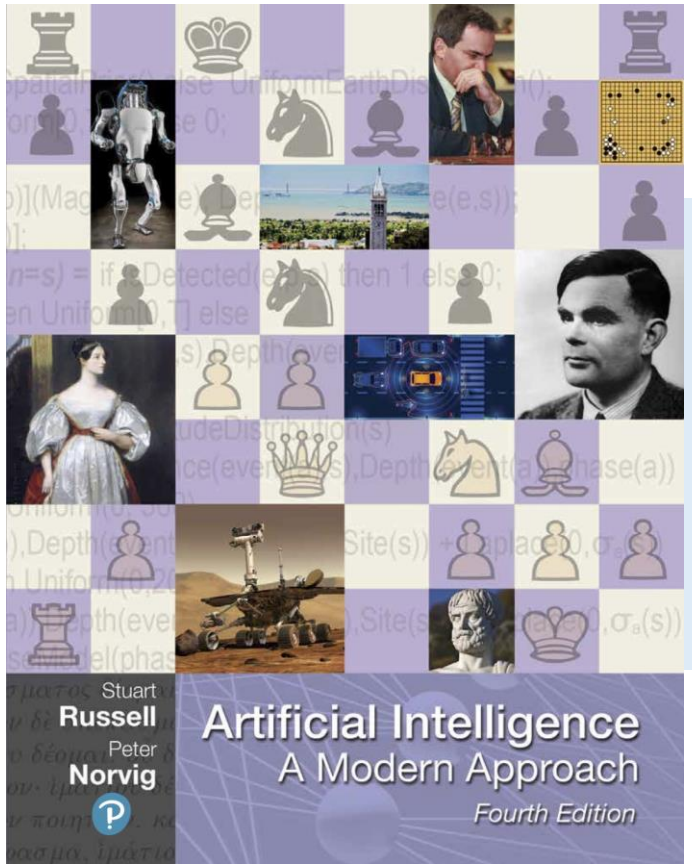
- Part II
  - **What is AI?**
  - OpAmp Case Study

AI definition



The science and engineering of making intelligent machines.

-Stanford Prof. John McCarthy, 1955



The study of agents that receive percepts from the environment and perform actions.

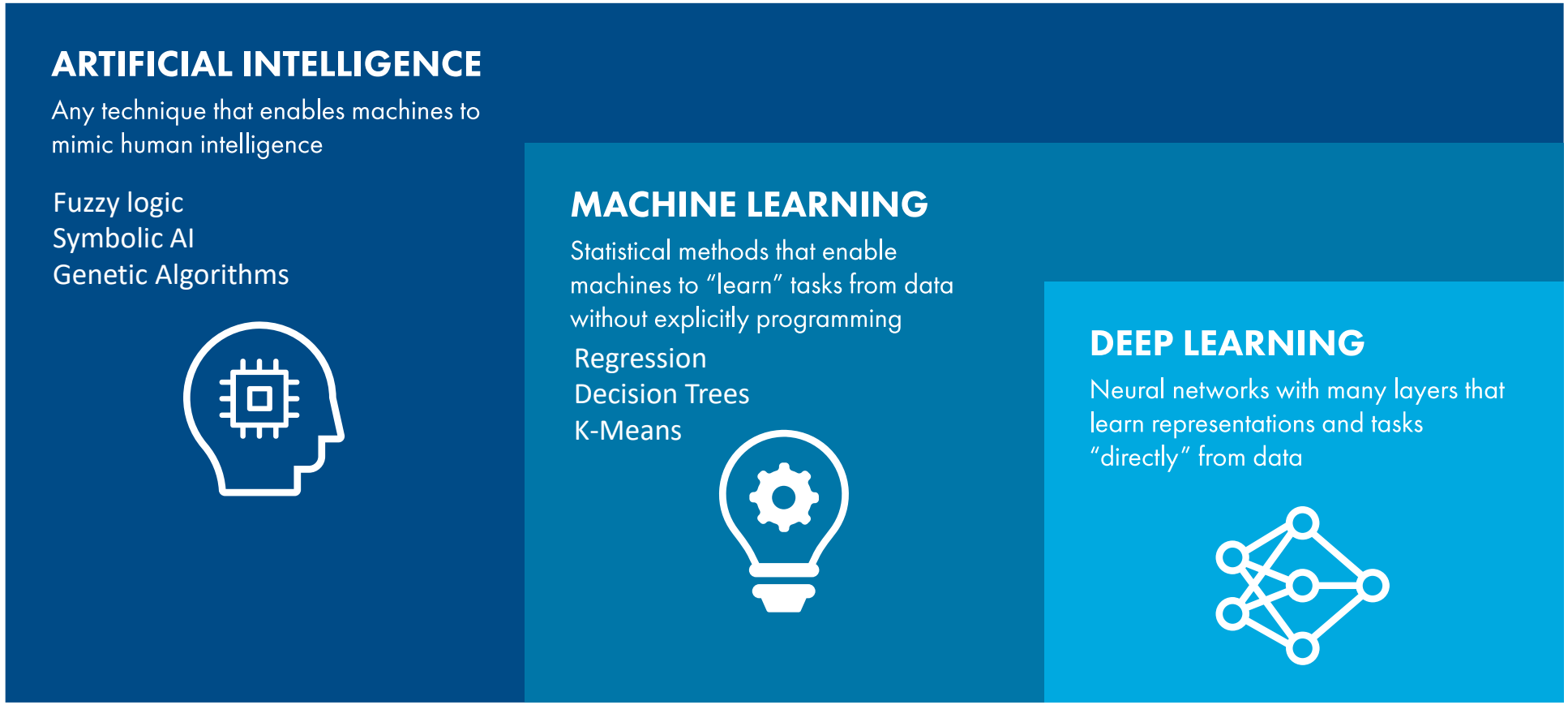
- Russel and Norvig, 1995

AI types

Reactive AI	Limited memory	Theory of mind	Self aware
Limited AI that only reacts to different kinds of stimuli based on preprogrammed rules. Does not use memory and thus cannot learn with new data. E.g. IBM's Deep Blue	Most modern AI. It can use memory to improve over time by being trained with new data, typically through an NN or other training model. Deep learning, a subset of machine learning, is considered limited memory AI.	Does NOT currently exist, but research is ongoing. AI that can emulate the human mind and has decision-making capabilities equal to that of a human, including recognizing and remembering emotions and reacting in social situations.	A step above theory of mind AI, self-aware AI describes a mythical machine that is aware of its own existence and has the intellectual and emotional capabilities of a human. Like theory of mind AI, self-aware AI does not currently exist.

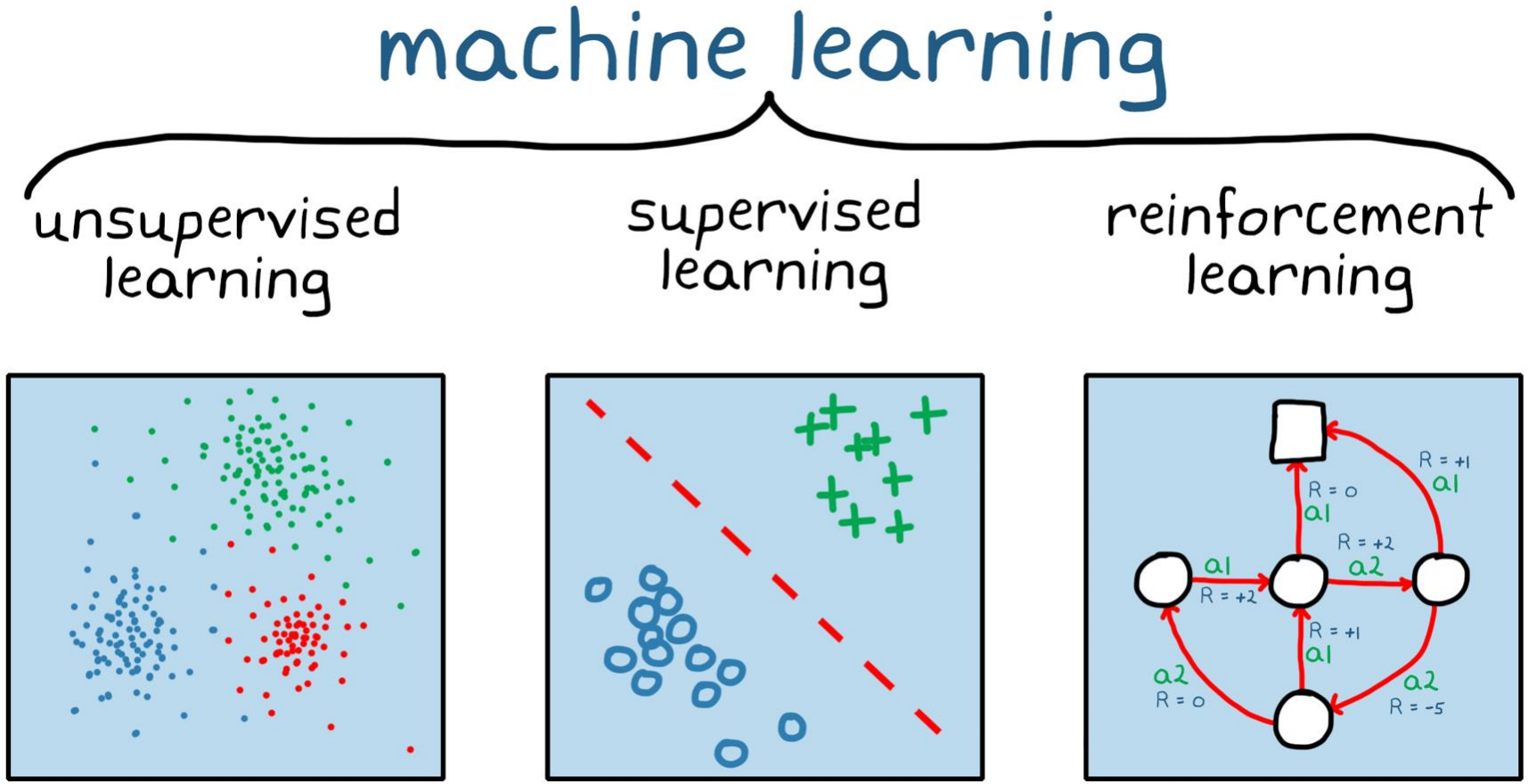
https://cloud.google.com/learn/what-is-artificial-intelligence

AI categories



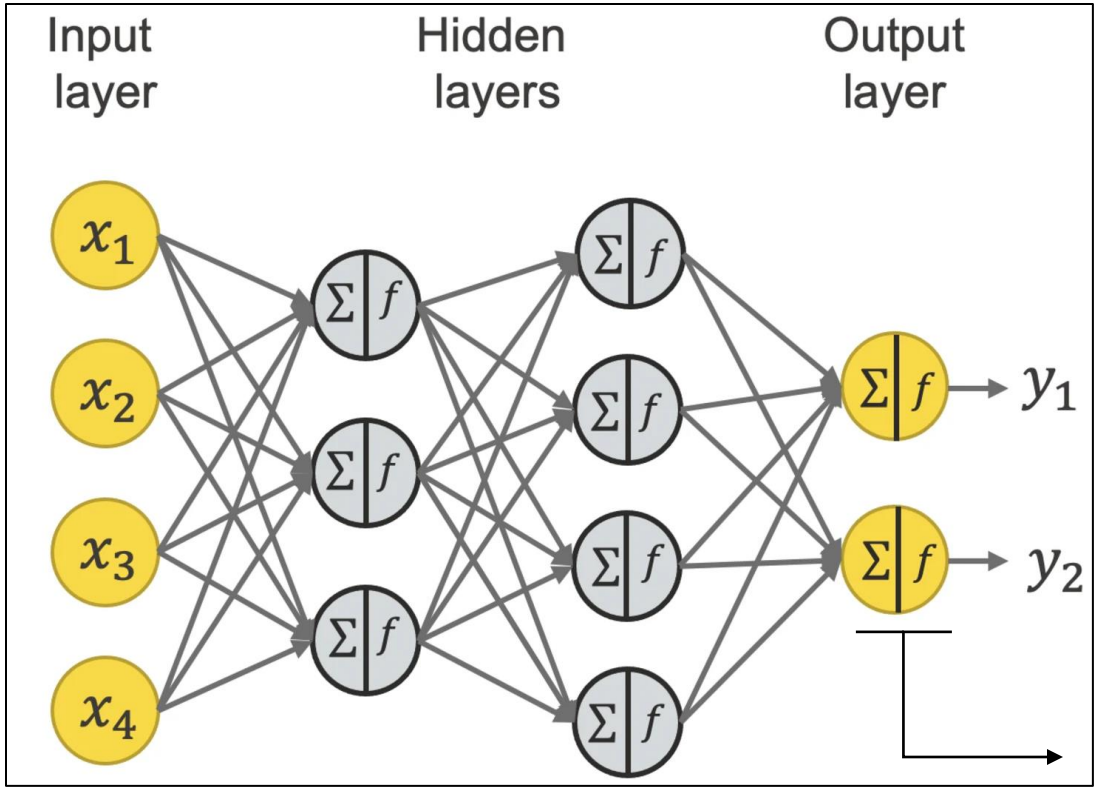
https://www.mathworks.com/discovery/artificial-intelligence.html

Machine Learning

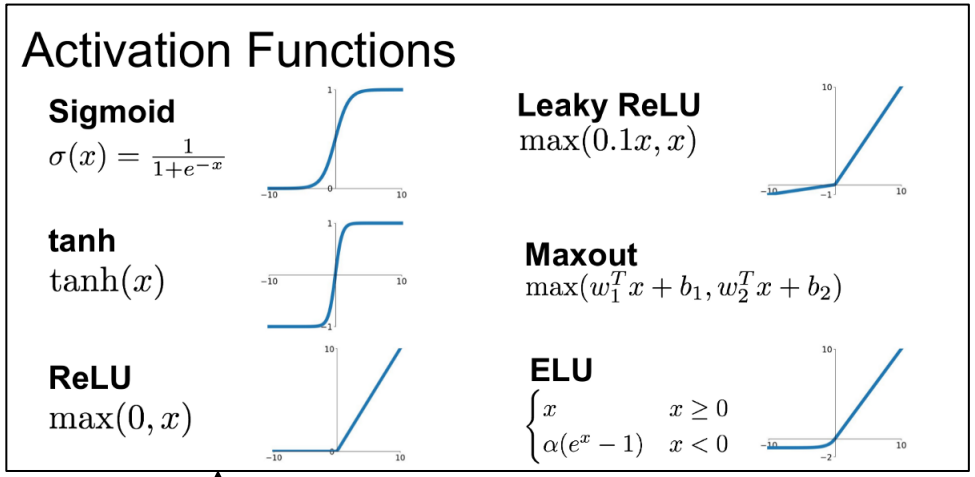


https://www.mathworks.com/discovery/reinforcement-learning.html

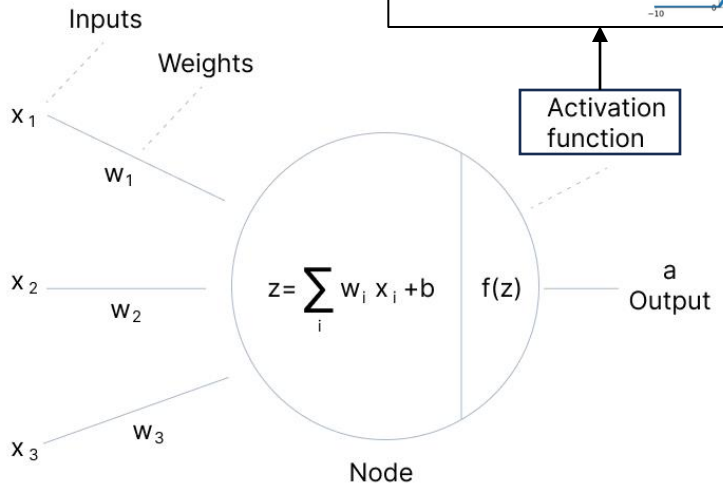
Neural network



https://www.knime.com/blog/a-friendly-introduction-to-deep-neural-networks

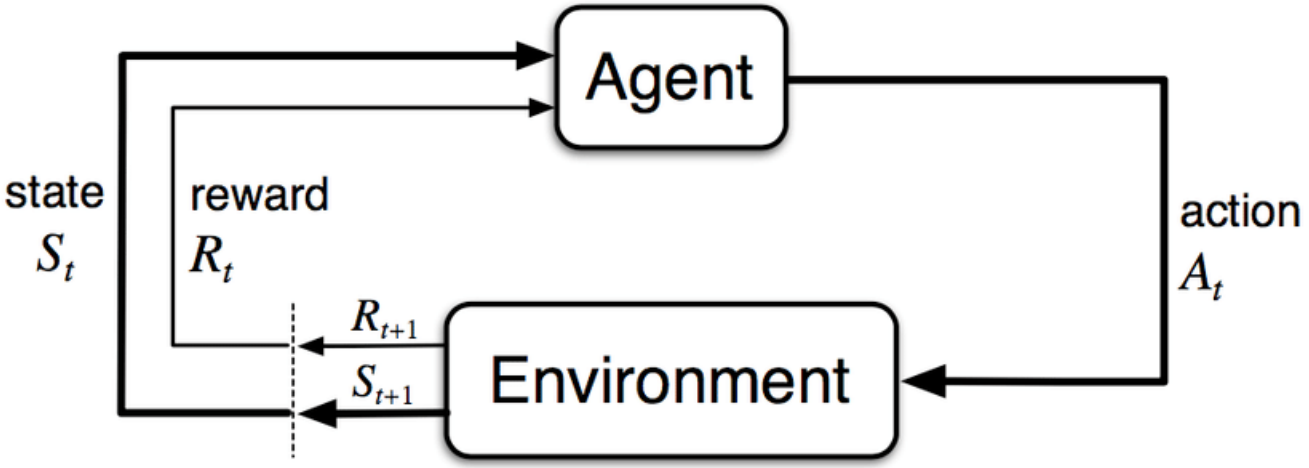


https://medium.com/@shrutijadon/survey-on-activation-functions-for-deep-learning-9689331ba092

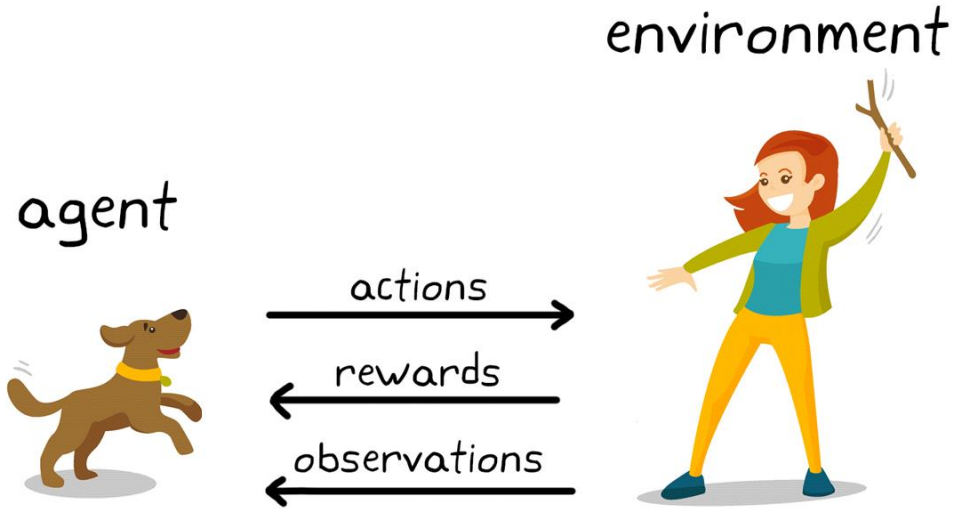


https://www.v7labs.com/blog/neural-networks-activation-functions

Reinforcement Learning



Sutton, R. S., & Barto, A. G. (2018). Reinforcement learning: An introduction (2nd ed.).



https://www.mathworks.com/discovery/reinforcement-learning.html

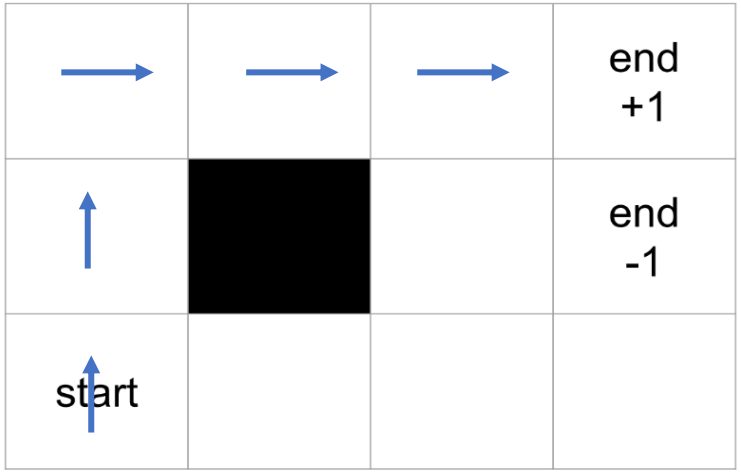
Value, q function, v function, grid problem example

State - value function:

Describes how good is the state s

$$
\begin{aligned}
v_\pi(s) &\doteq \mathbb{E}_\pi[G_t \mid S_t = s] \\
&= \mathbb{E}_\pi[R_{t+1} + \gamma G_{t+1} \mid S_t = s] \\
&= \sum_a \pi(a|s) \sum_{s'} \sum_r p(s', r \mid s, a) \Big[r + \gamma \mathbb{E}_\pi[G_{t+1} | S_{t+1} = s'] \Big] \\
&= \sum_a \pi(a|s) \sum_{s', r} p(s', r \mid s, a) \Big[r + \gamma v_\pi(s') \Big], \quad \text{for all } s \in \mathcal{S},
\end{aligned}
$$

Policy — Transition Probability — Discount factor



https://towardsdatascience.com/reinforcement-learning-implement-grid-world-from-scratch-c5963765ebff

Action-value function: $q_\pi(s,a) \doteq \mathbb{E}_\pi[G_t \mid S_t = s, A_t = a]$

$$
= \mathbb{E}_\pi\left[\sum_{k=0}^{\infty} \gamma^k R_{t+k+1} \,\middle|\, S_t = s, A_t = a \right]
$$

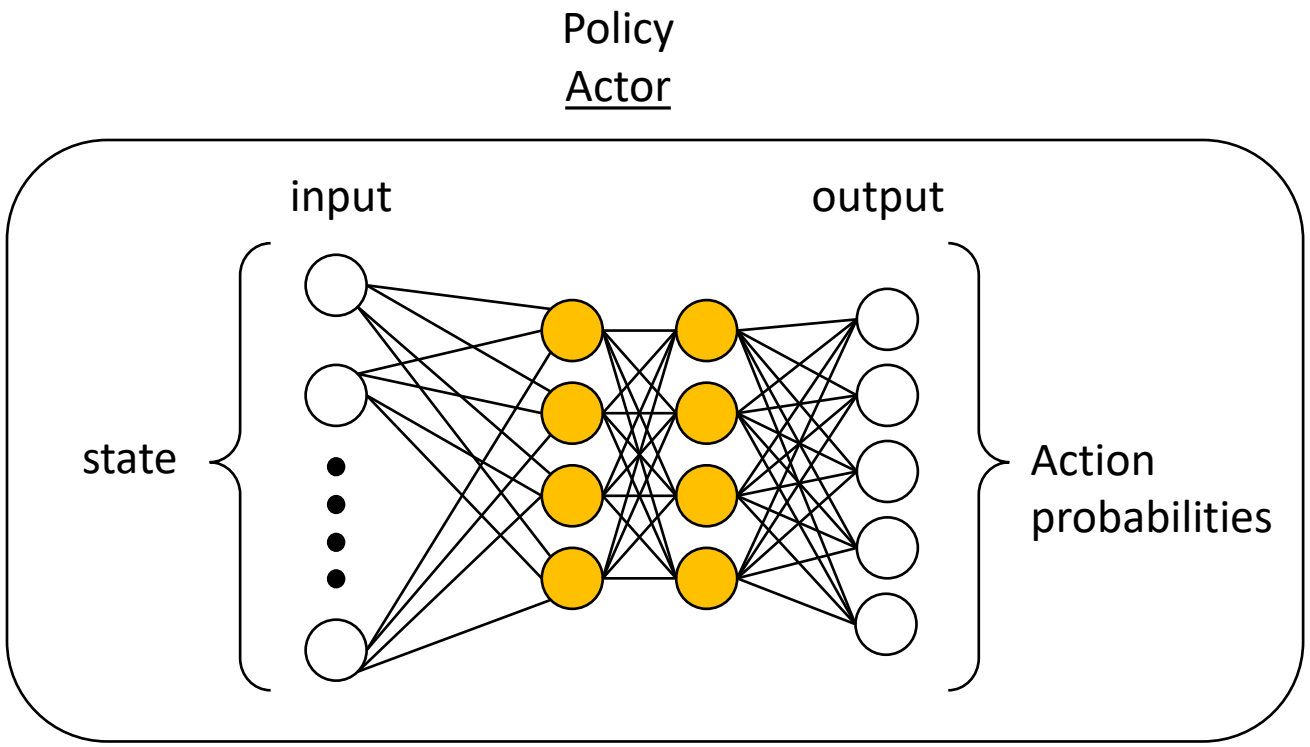
Describes how good is to take the a if you are in state s

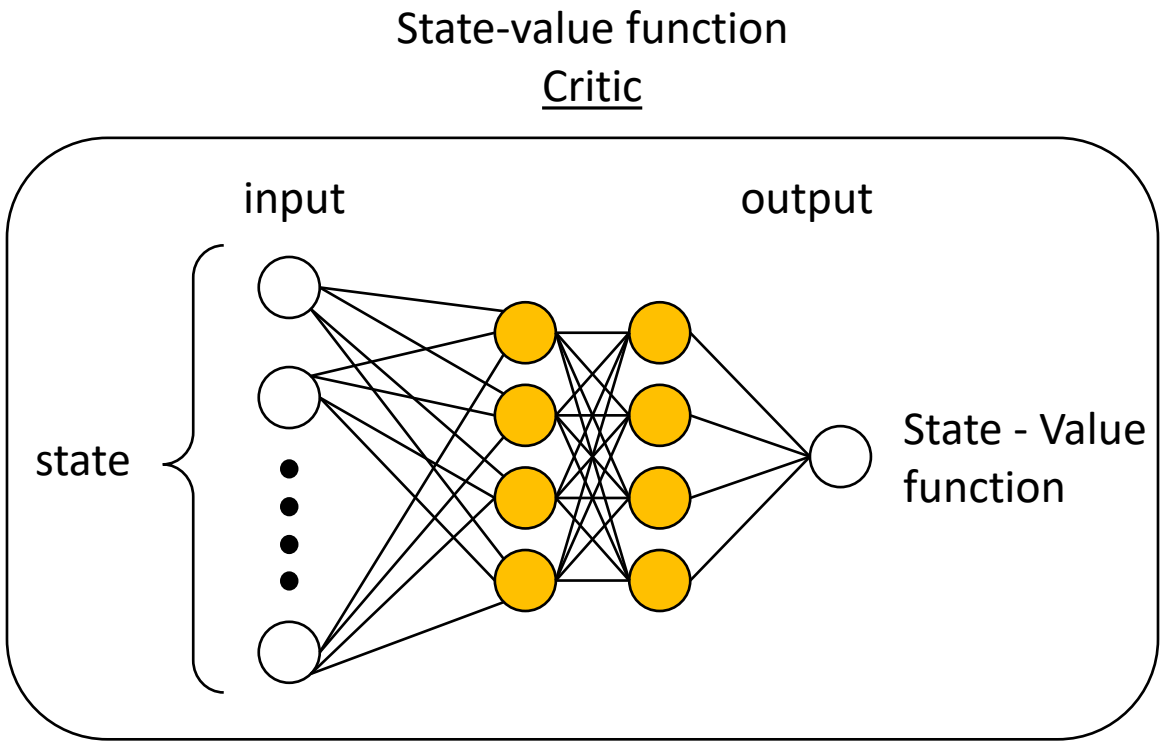
Policy:

$$
\begin{aligned}
\pi'(s) &\doteq \arg\max_a q_\pi(s,a) \\
&= \arg\max_a \mathbb{E}[R_{t+1} + \gamma v_\pi(S_{t+1}) \mid S_t = s, A_t = a] \\
&= \arg\max_a \sum_{s', r} p(s', r \mid s, a) \Big[r + \gamma v_\pi(s') \Big],
\end{aligned}
$$

Sutton, R. S., & Barto, A. G. (2018). Reinforcement learning: An introduction (2nd ed.).

Deep RL theory (w. NNs)





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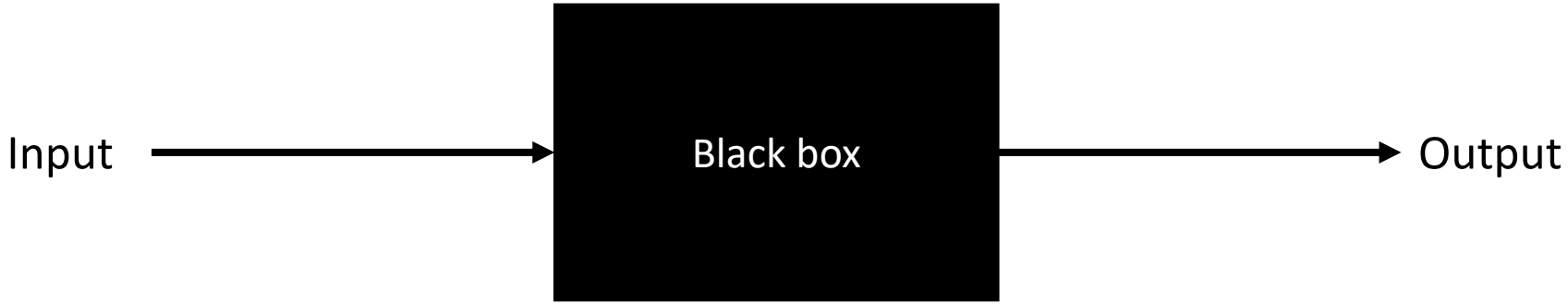
Why analog design has not yet exploited Machine Learning?

Analog Design X AI difficulties

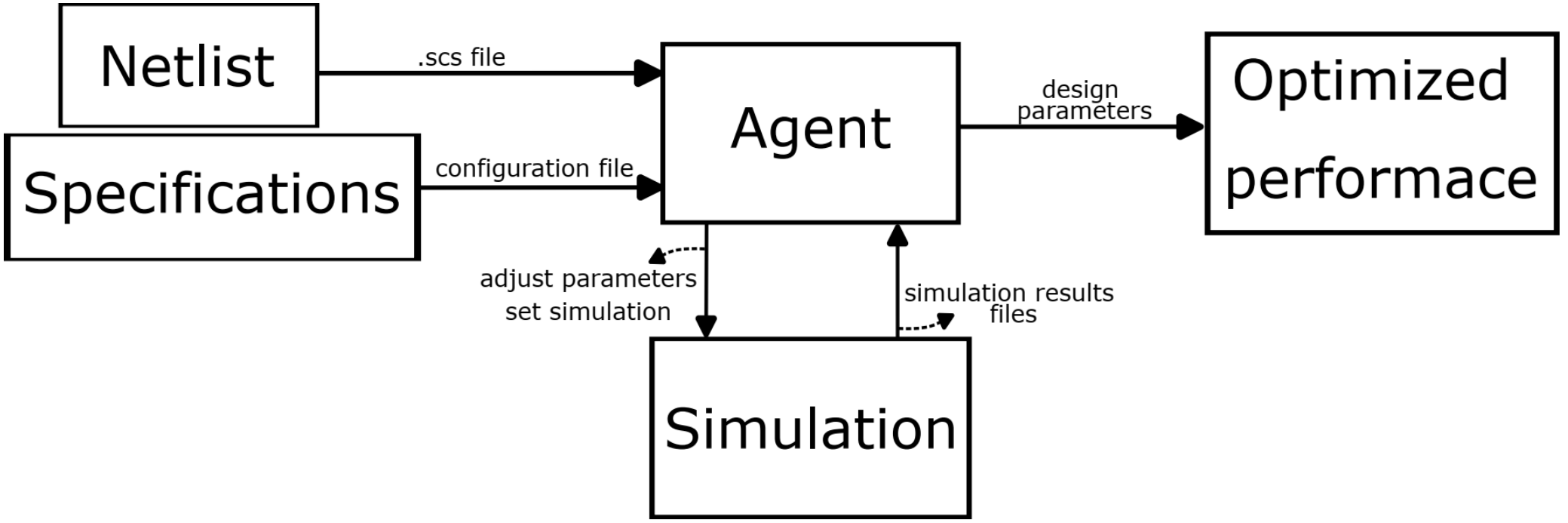
- **Complexity**: Analog circuits are sensitive to variations, making them harder to model.
- **Limited Data**: Large, labelled datasets for training ML models are scarce.
- **Diverse Needs**: Different applications require unique performance specifications.
- **High Simulation Costs**: Analog simulations are time-consuming and resource-heavy.
- **Human Expertise**: Analog design relies heavily on experienced engineers.
- **Trust Issues**: ML methods are less transparent, making verification difficult. Designers are not trusting their work to others easily.

Proposed Solution: Black box approach

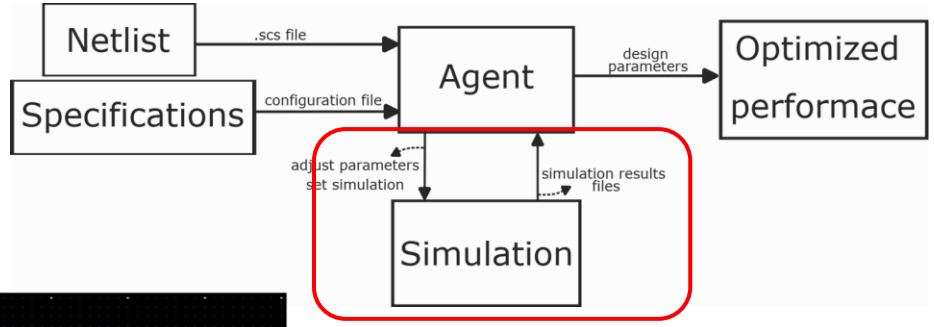


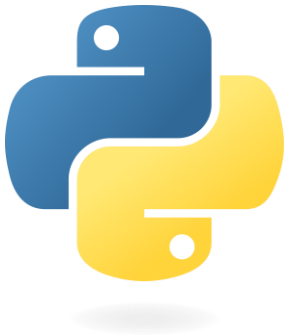
- Main focus on its inputs and outputs, without any knowledge of its internal workings or structure
- The end user interacts only with these
- Eliminating the human in the loop interference – leveraging automation

General flowchart

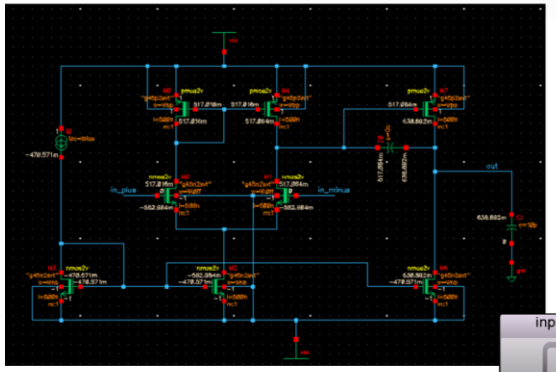


Simulation interface





python



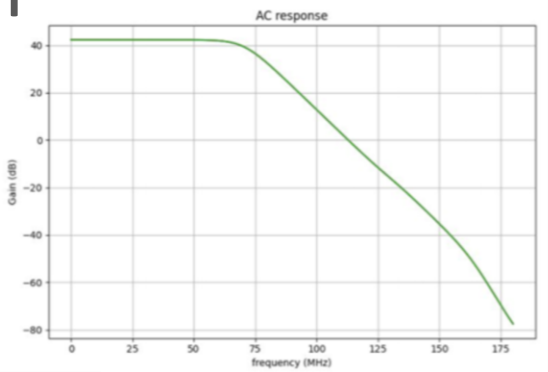
+ simulation settings

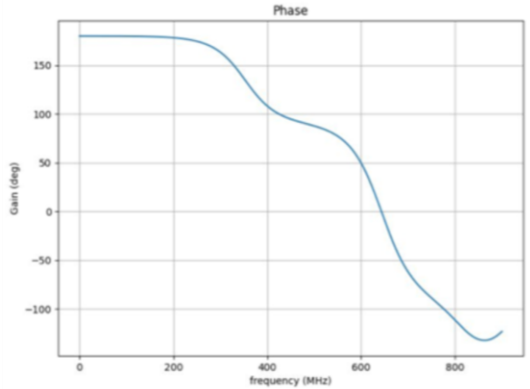
inputs.scs

SPICE simulator

Simulation results

Post processing



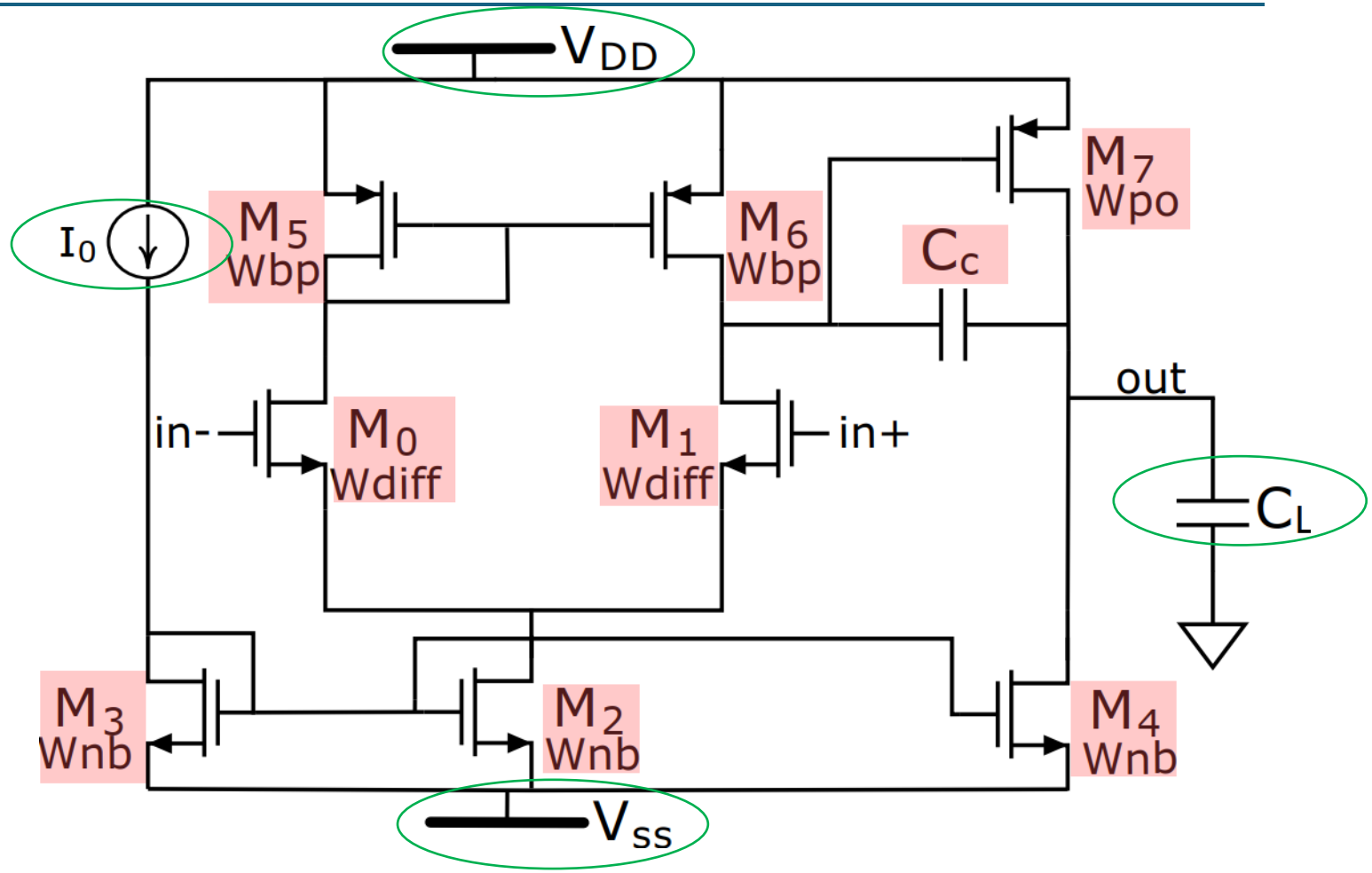


Operational Amplifier case

Parameters
Wbp
Wdiff
Wnb
Wpo
Cc
Performance metrics
Phase margin
Unity gain bandwidth
Gain
ICMR
Vout swing
Slew Rate

Reach specific threshold

Maximize



Our framework

- All the RL elements are normalized to enhance generalization
- Using Proximal Policy Optimization (PPO)
- For each new topology ONLY the state must be redefined

State	Action	Termination State
Wbp Wdiff Wpo Wnb Cc Phase magin Unity Gain Gain ICMR Slew Rate Out range	Increase / decrease parameter / do nothing for parameter 1 Increase / decrease parameter / do nothing for parameter 2 . . .	20 steps/ simulation OR no improvement for a window size

The transistor region for each transistor (7)

Reward function

$$r = \begin{cases} -\beta \sum_{i=1}^{n} \delta_i - h_c \sum_{i \in C} |y_i - \hat{y}_i| + h_o \sum_{i \in O} o_i, & \text{cond.=False} \\ h_c \sum_{i \in C} |y_i - \hat{y}_i| + h_o \sum_{i \in O} o_i, & \text{otherwise} \end{cases} \quad (1)$$

$$\delta_i = \begin{cases} 0, & \text{if oparation region of i-th transistor is saturation} \\ 1, & \text{otherwise} \end{cases} \quad (2)$$

$$C = [G, UGBW, PM] \quad (3)$$

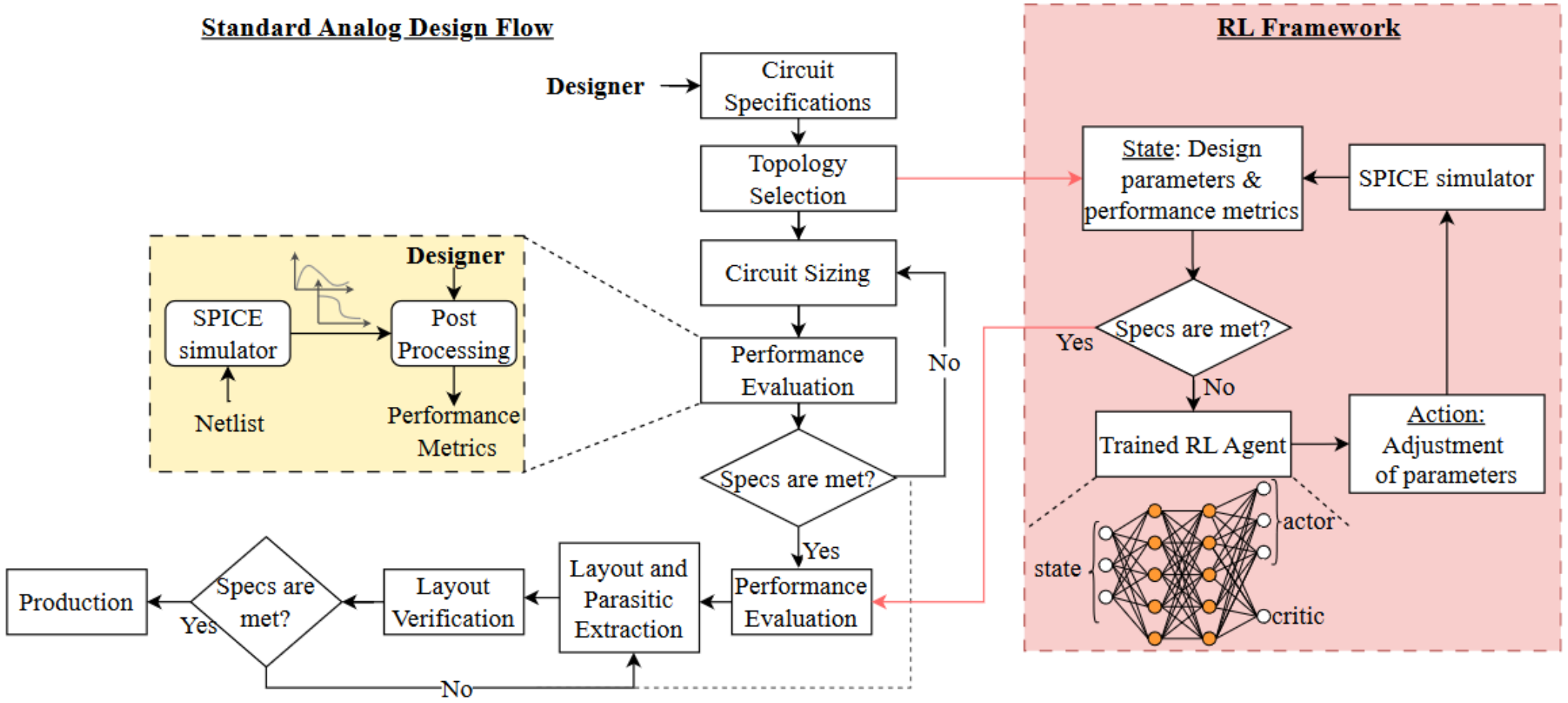
$$O = [\frac{1}{|y_{ICMR} - y_{\hat{ICMR}}|}, \frac{1}{|y_{Vout} - y_{\hat{Vout}}|}, SR] \quad (4)$$

$$cond. = True \iff \sum_{i=1}^{n} \delta_i = 0 \ \& \ \hat{y}_i > y_i \forall i \in C \quad (5)$$

- $O = objectives$
- $C = constraints$
- $h_o, h_c = scailing\ constands$
- $\beta = trainsistor\ region\ sacling\ constand$
- $y = target\ value$
- $\hat{y} = predicted\ value$

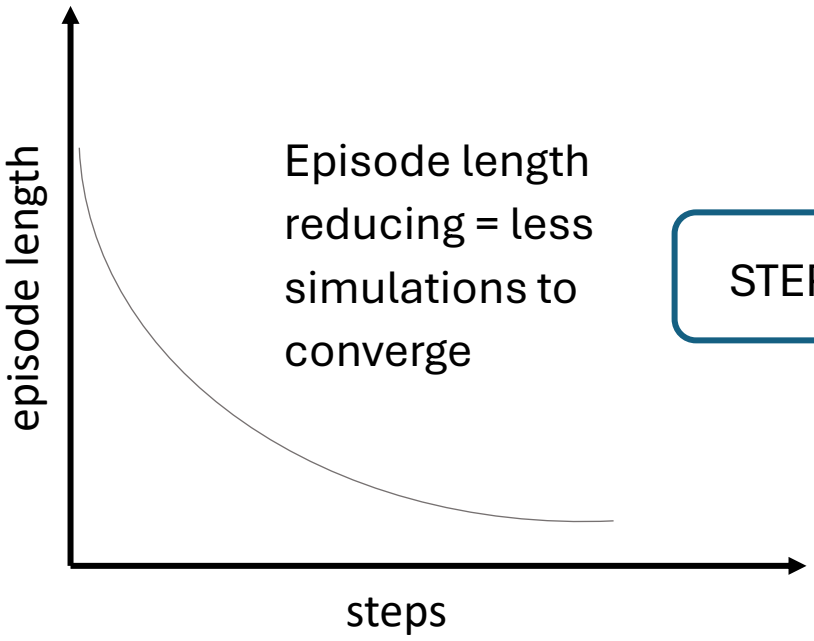
Our environment is *episodic*: when a termination state occurs, the cumulative reward is reset to zero

Standard VS RL analog design flow



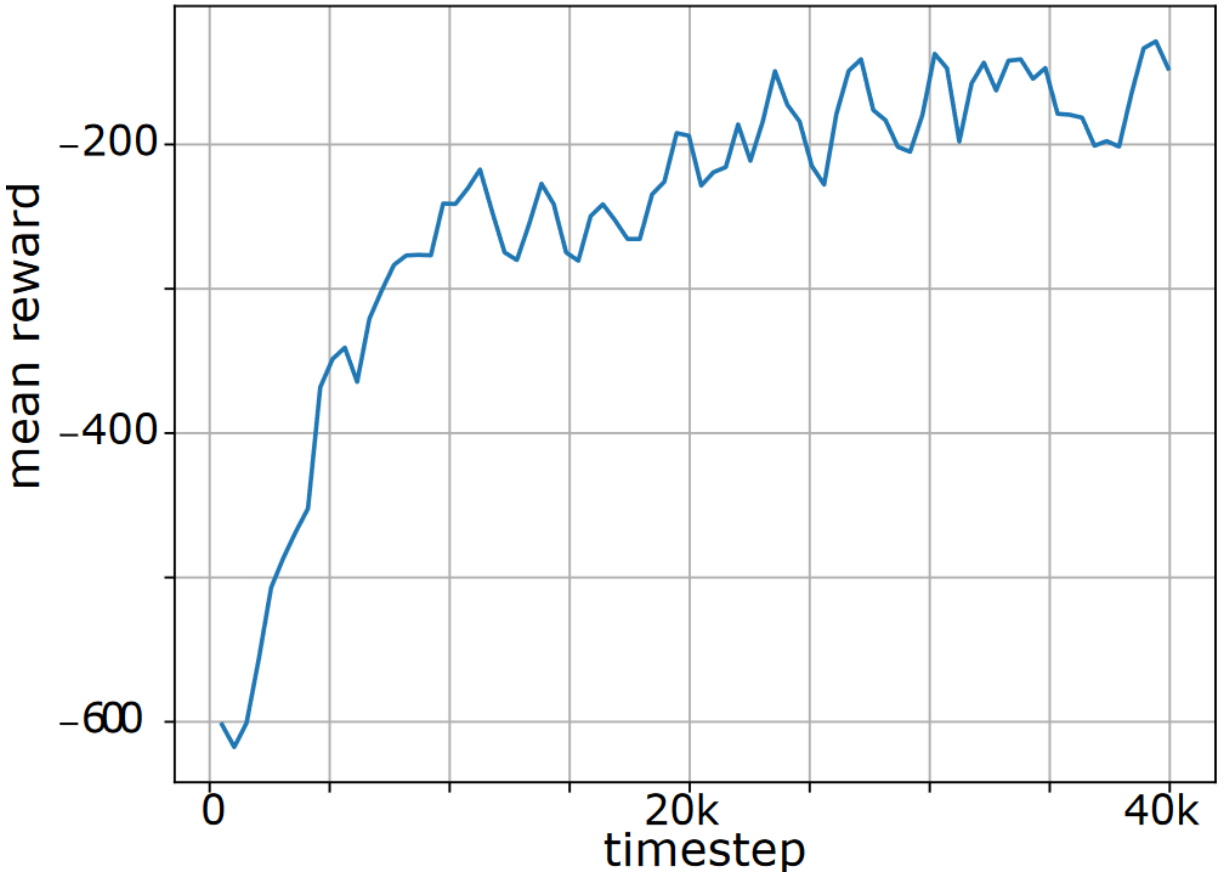
Training

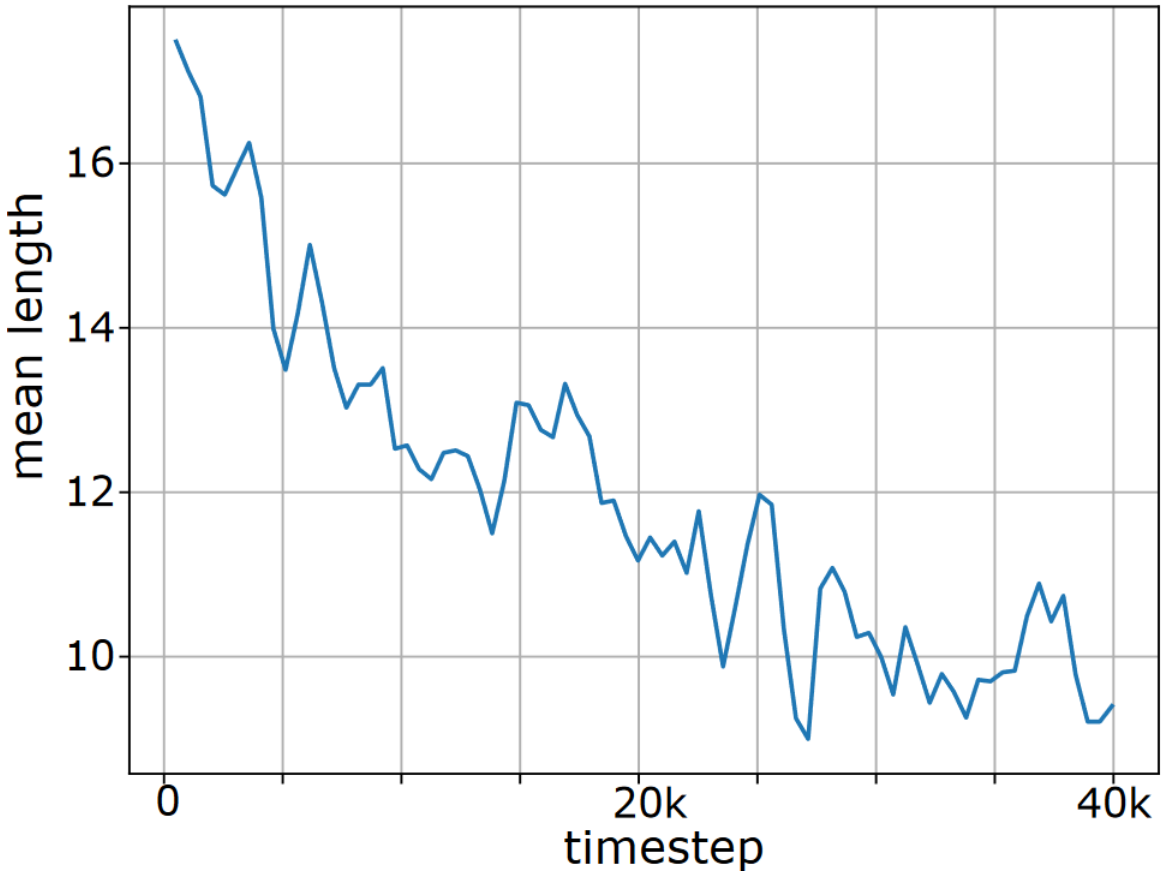
Ideal results for training



STEPS = SIMULATIONS

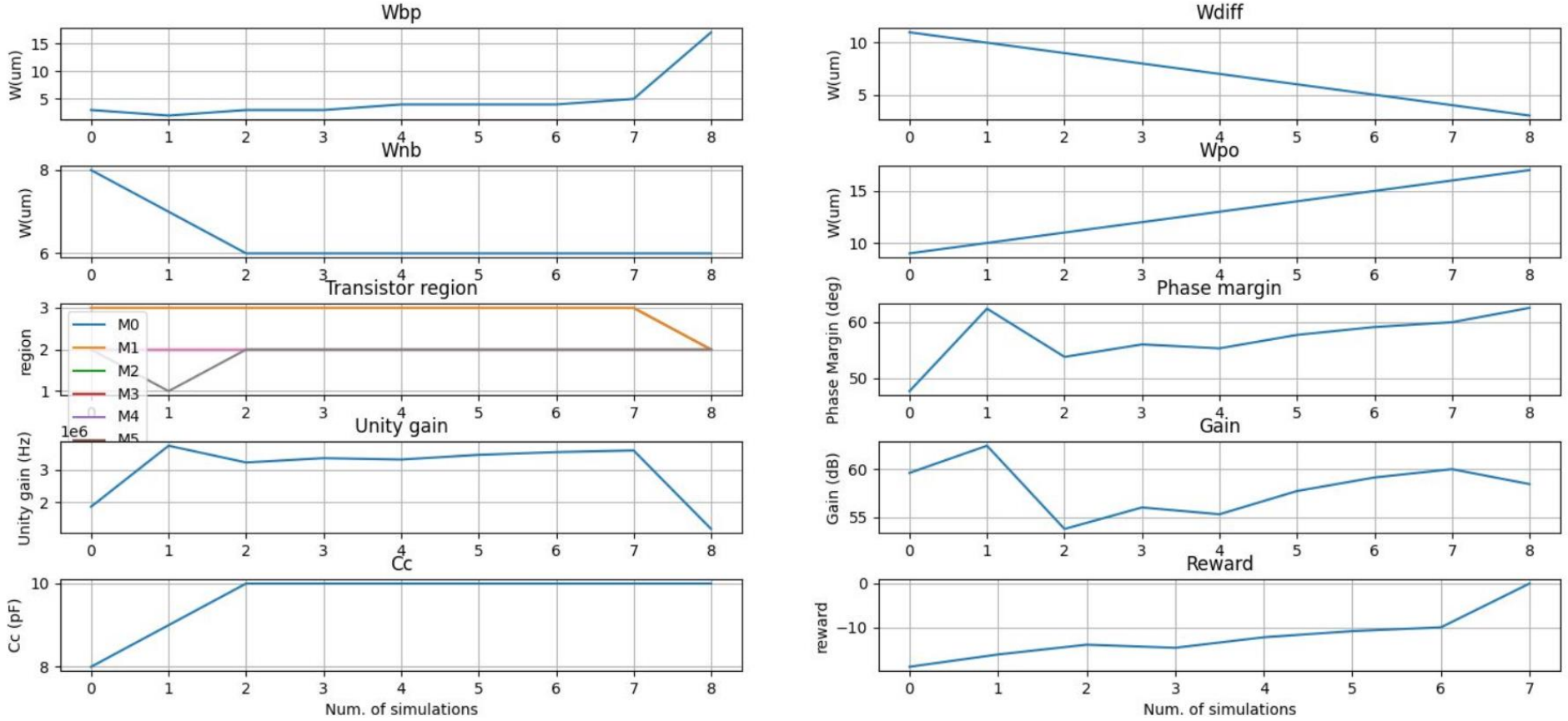
Training (65nm)



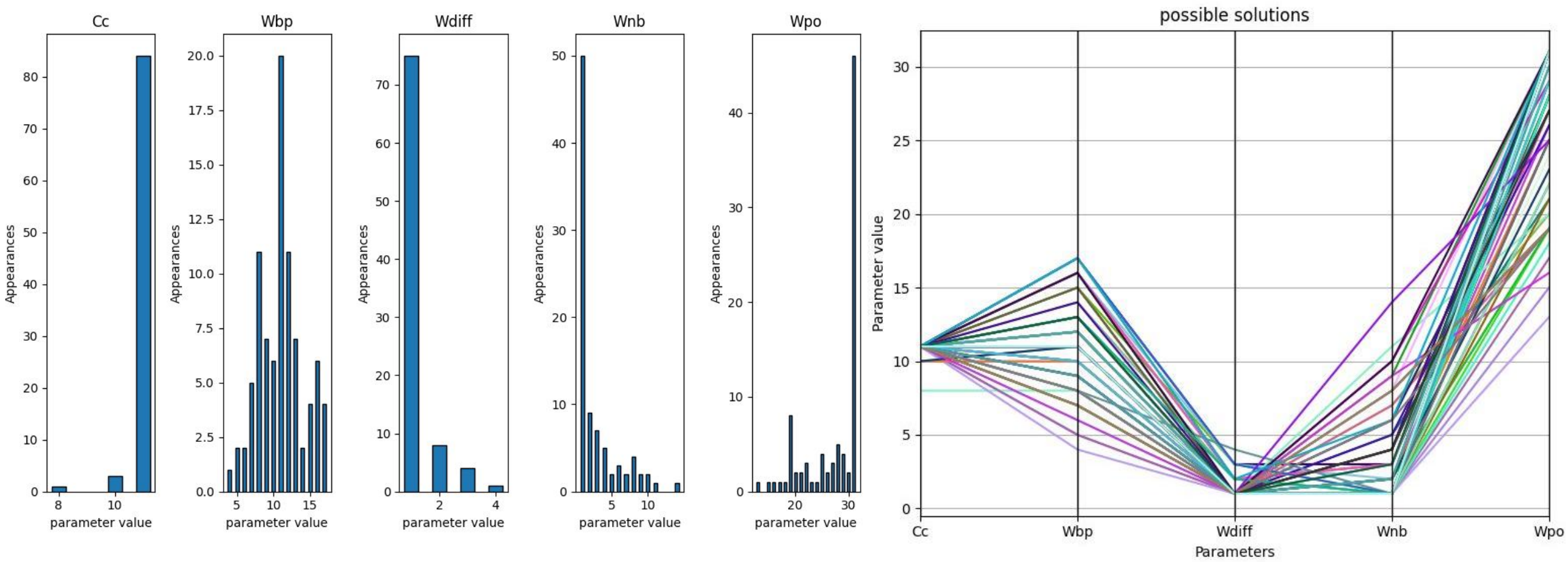


Evolution

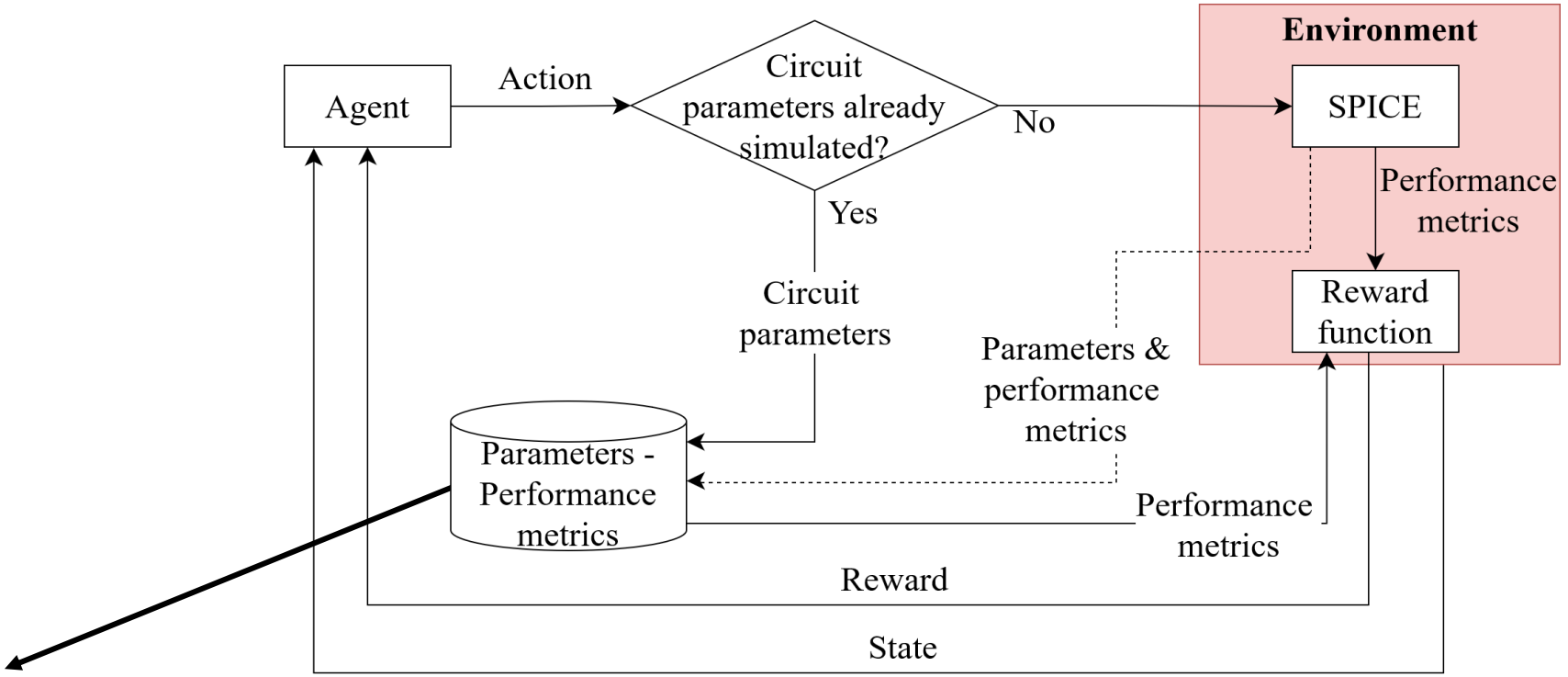
- In all methodologies (non ML incl.) the end result must be evaluated



Results


Cc
Wbp
Wdiff
Wnb
Wpo
Appearances
parameter value
possible solutions
Parameter value
Cc
Wbp
Wdiff
Wnb
Wpo
Parameters

Memoization: avoiding simulation



Memoization: bypassing the simulator using a dataset generated during the training. Simulation has the biggest duration in the flow.

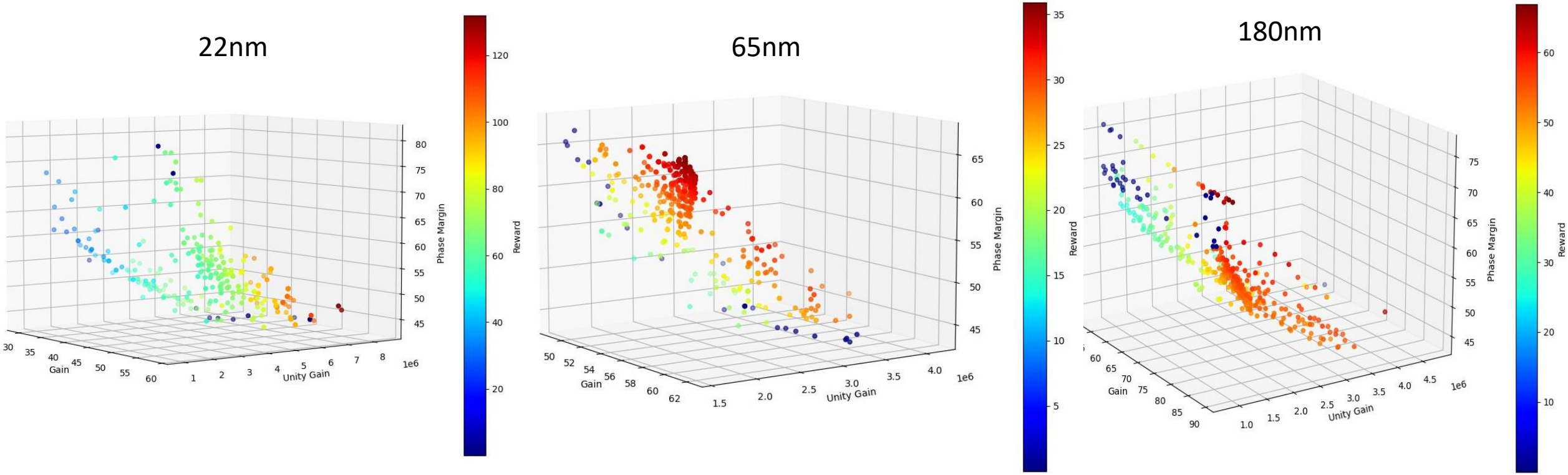
Especially in the last iterations, many simulations (same input, output) are repeated => Benefiting from the determinism.

Training the same agent on multiple process nodes

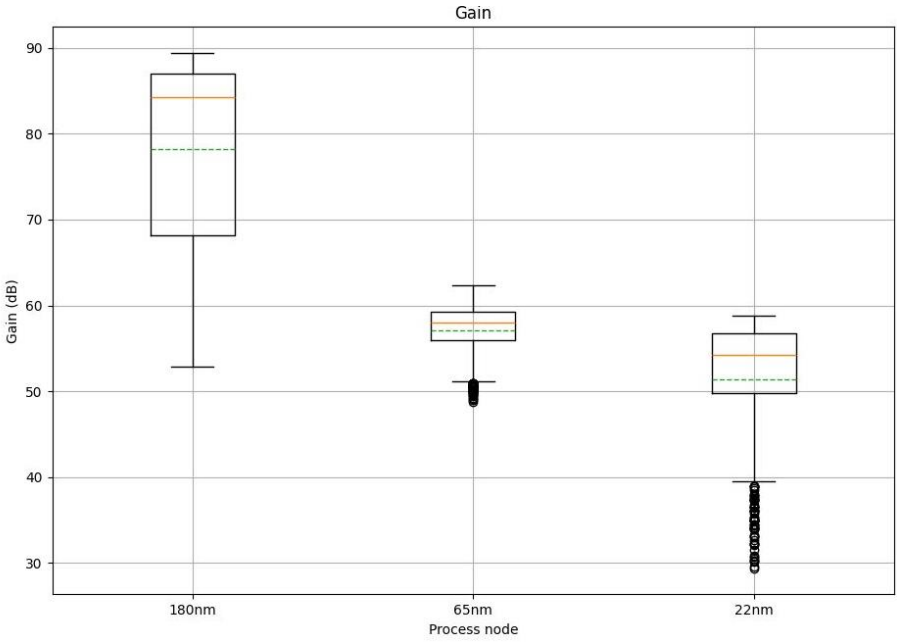
- Utilized the same agent on multiple process nodes
- Why?
  - Verifying the functionality of the agent
  - Evaluating how general the model is
  - Transfer learning potential

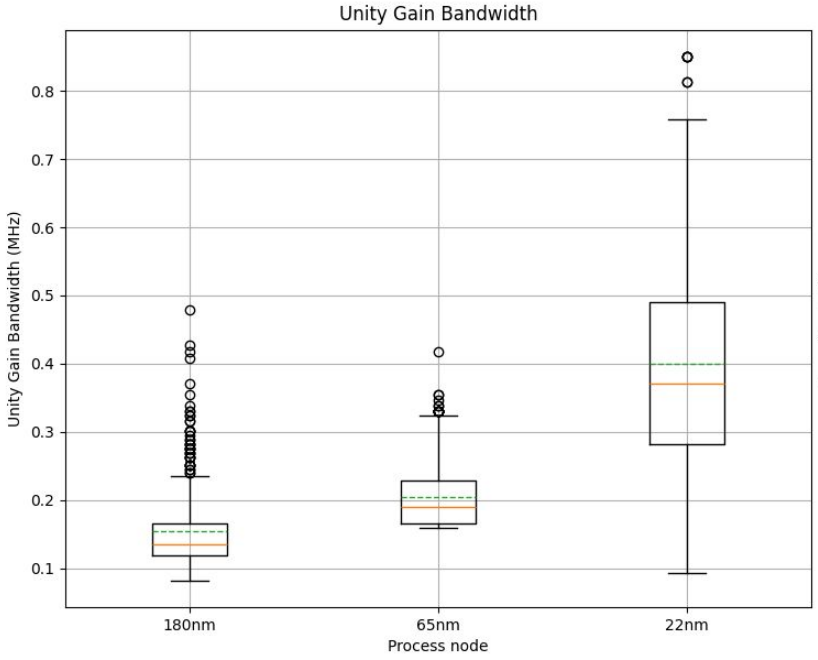
22nm -> 65nm -> 180nm

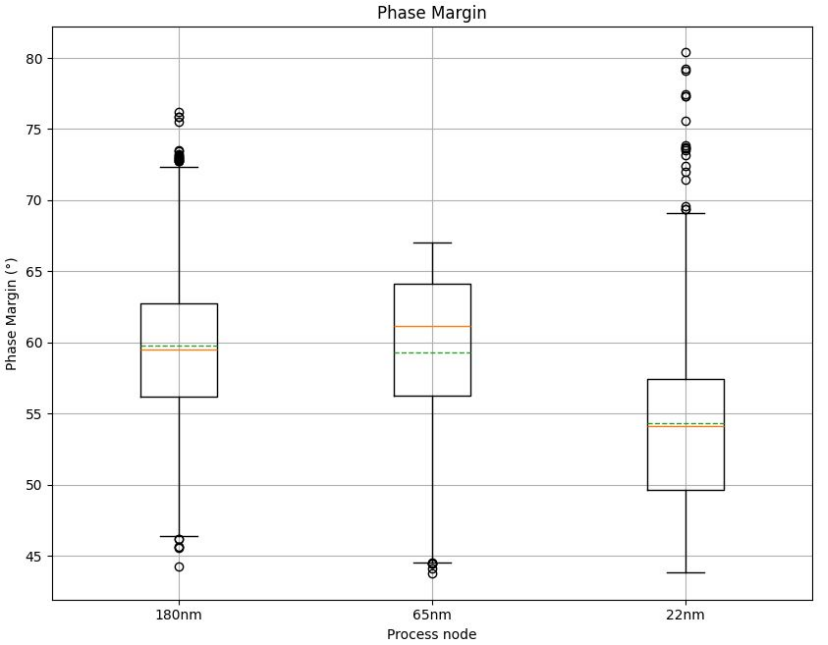
3d scatter plot for the three process nodes



Multiple process nodes - Statistical analysis

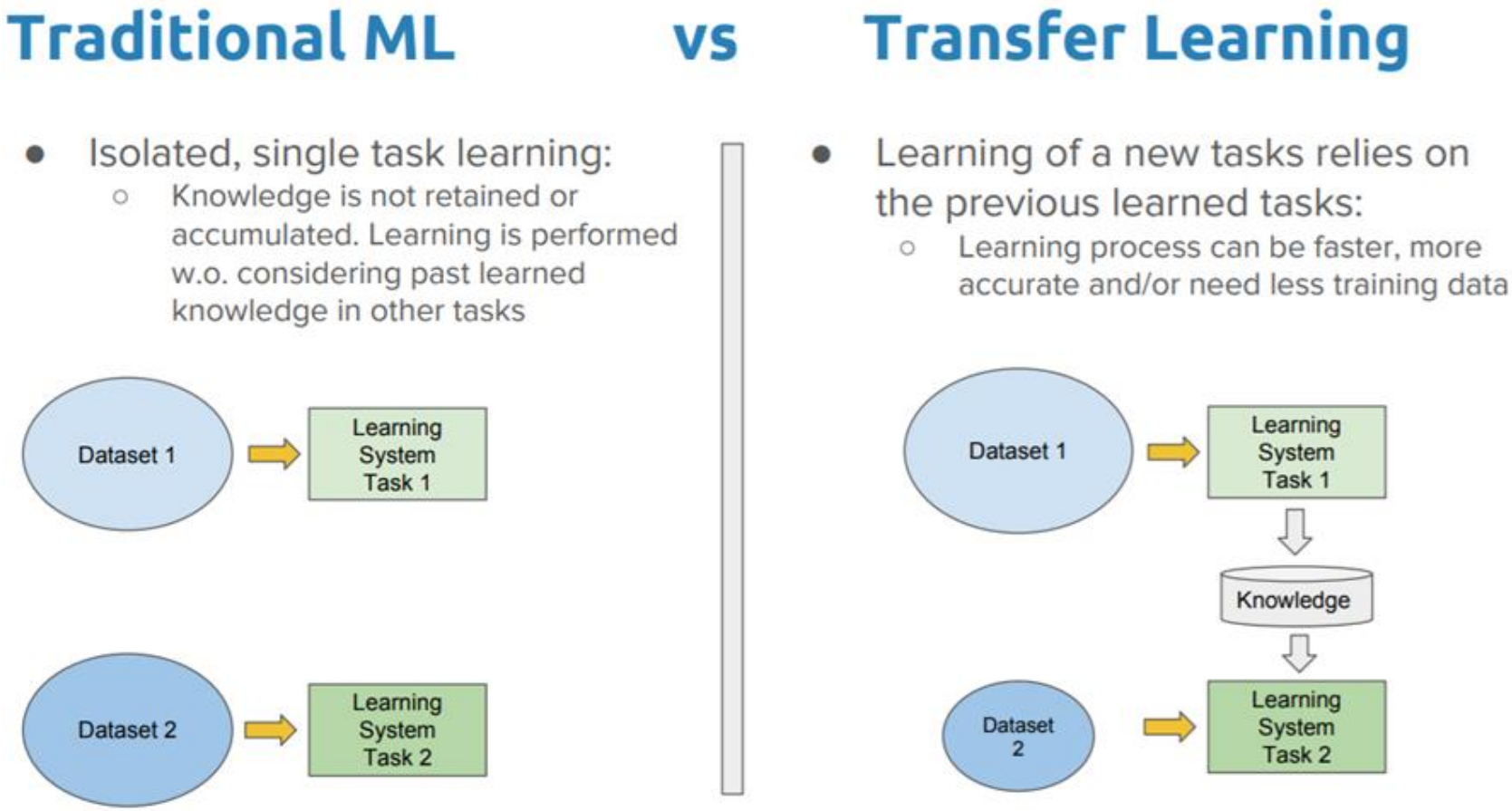






Explaining transfer learning

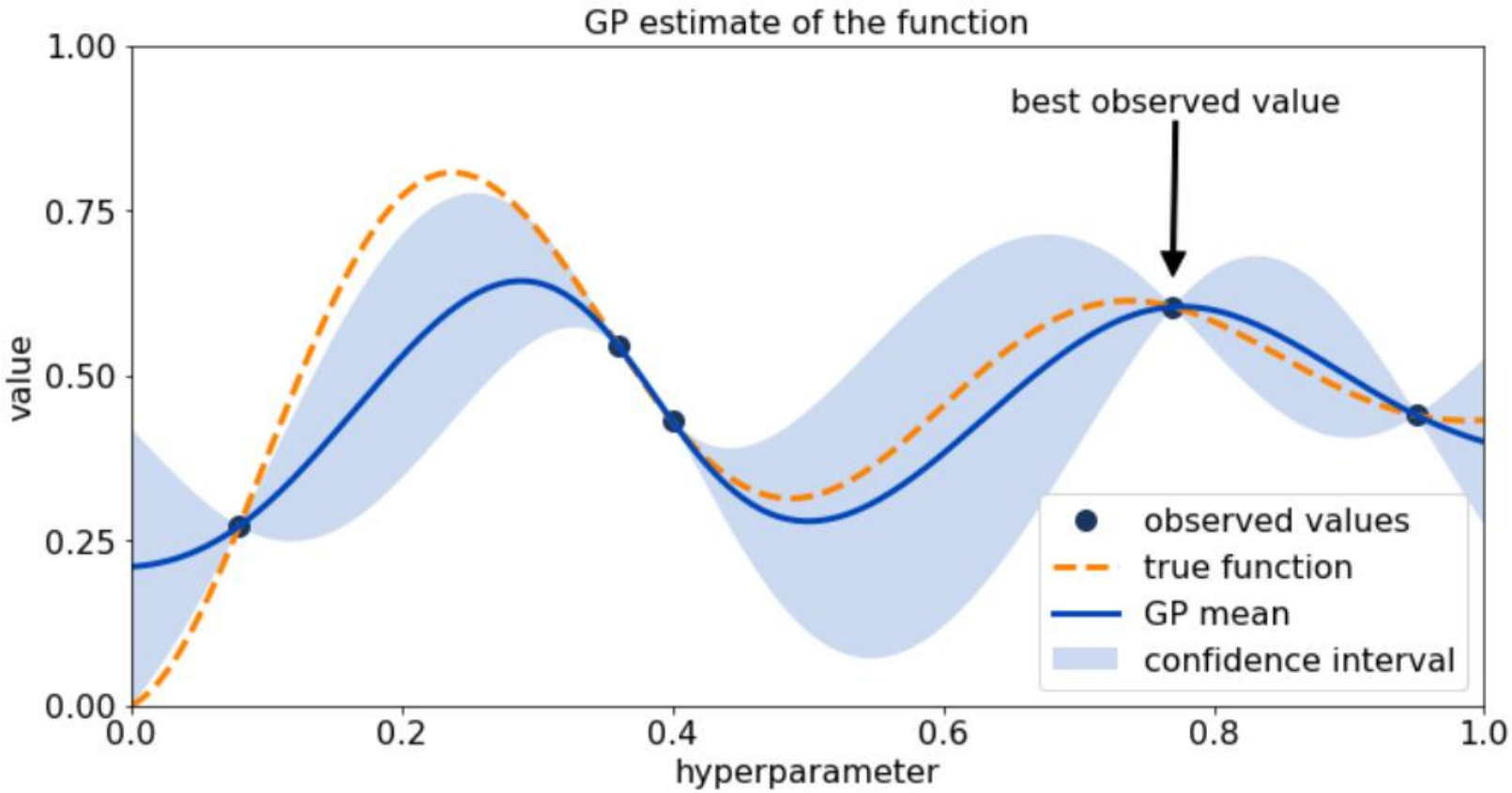
- Exploiting the knowledge gathered from already trained agents
- Making the immigration to new technologies/ topologies faster
- Having a general model leverages the designer work making it a stronger tool for them



https://www.v7labs.com/blog/transfer-learning-guide

Bayesian optimization

- Applied on unknown functions
- A Gaussian process nodes for fitting the samples
- The samples are gathered based on the exploration and exploitation trade off
- Gives as predictions



Bayesian optimization for narrowing the design space

- If applied on the first problem with objective to achieve the hard constraints will give us a narrowed design space.
- Less parameter values to explore -> Faster RL training
- More automation/ less human interaction

Conclusions

- In general RL methods need an enormous amount of interactions with the environment to learn
- ALTHOUGH the final products is based on mimicking human behavior which reaches and can even surpass it.
- There is know need for retraining for new specifications

⇨ The researches of analog IC automation have shifted their focus in this direction for circuit sizing.

Thank you!

Any Questions?