Readout Front-End ASIC Design for Radiation Detection

Anastasios Michailidis

Ph.D. Student

Electronics Laboratory, Physics Department

Aristotle University of Thessaloniki, Greece

✉ anamicha@physics.auth.gr

UNIVERSITÄT BONN

Powered By
DAAD
Deutscher Akademischer Austauschdienst
German Academic Exchange Service

ARISTOTLE
UNIVERSITY
OF THESSALONIKI

1. Introduction to Readout Electronics
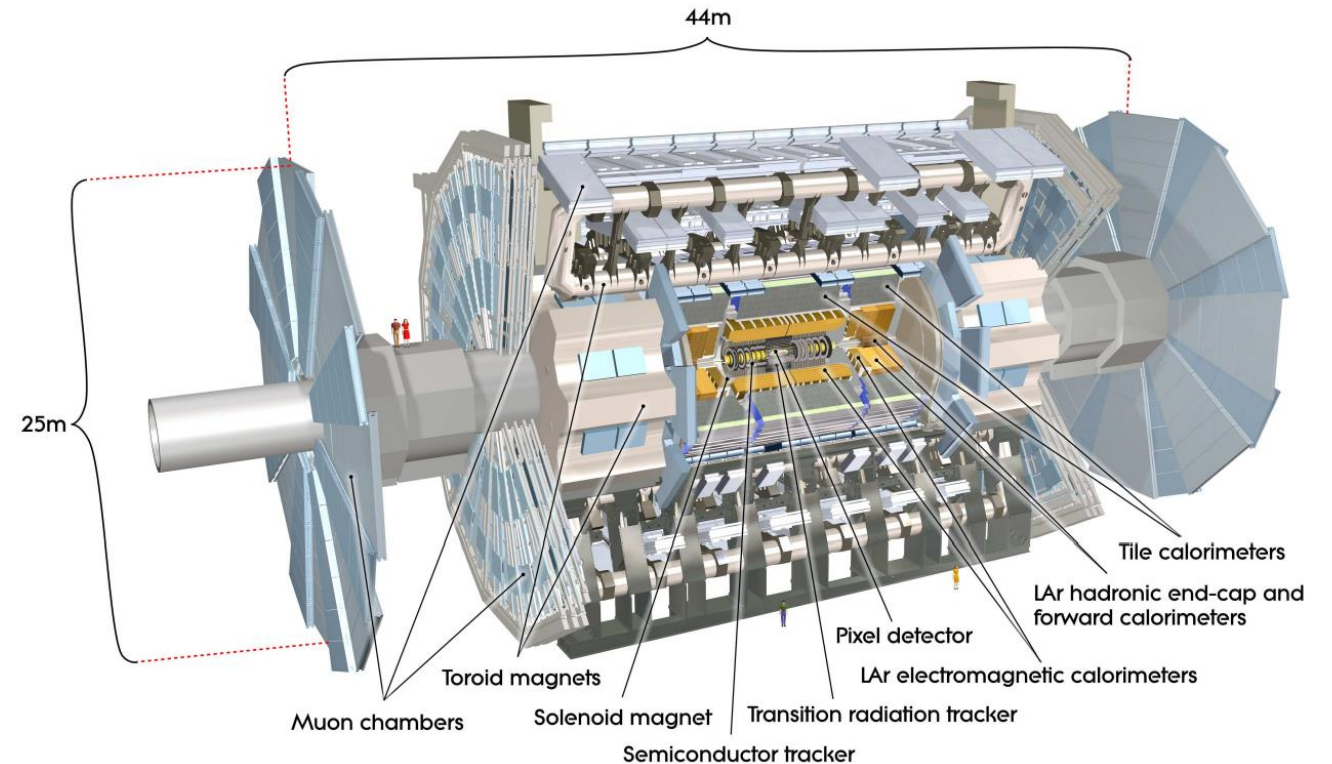
2. Planar and 3D Pixel Detectors

3. Analog Front-End Circuitry and Analysis

4. Readout Front-End ASIC Design

5. Conclusion and Discussion

Introduction to Readout Electronics

- Modern experiments using particle colliders require simultaneous detection of hundreds of particle tracks with micrometer spatial and **nano-to-picosecond timing resolution.**
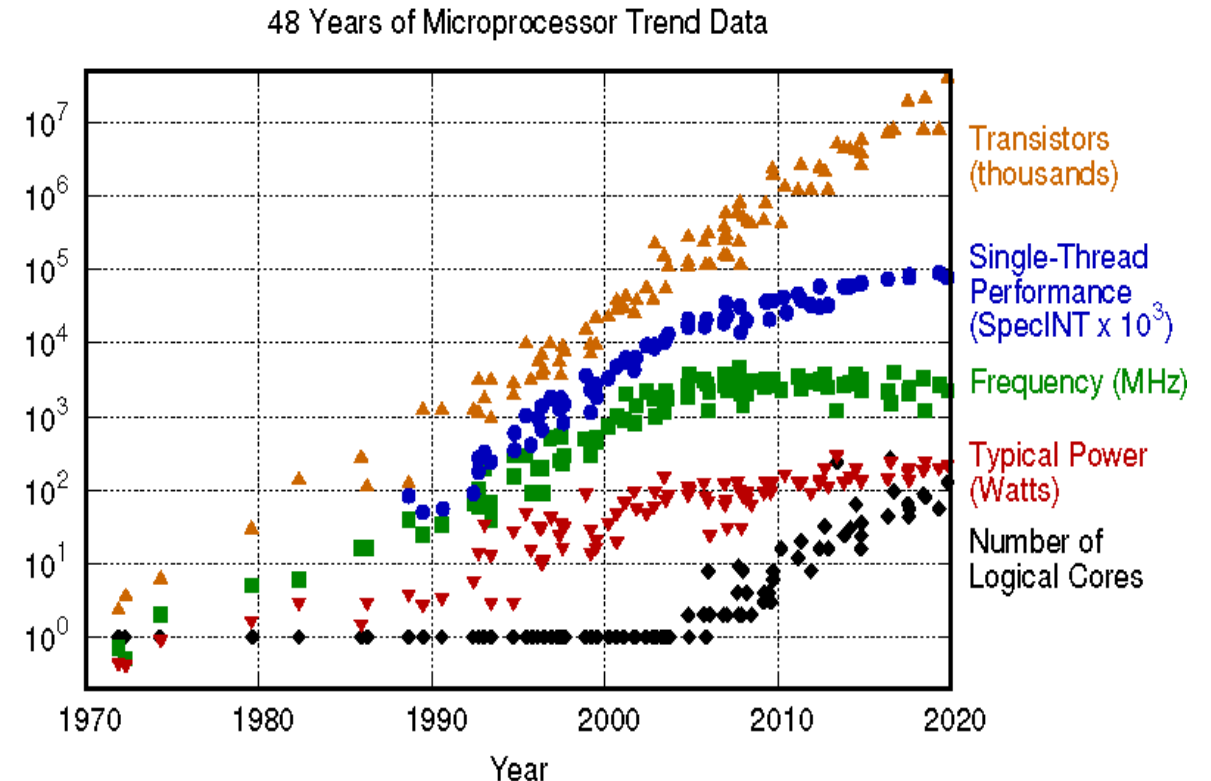

Layout of the ATLAS detector (taken from: [1])

Introduction to Readout Electronics

- Readout ASICs for radiation detection were developed using **high-level of integration** due to the miniaturization of electronics according to Moore's Law:

    "... *The number of transistors in an integrated circuit doubles about every two years...*"


48 Years of Microprocessor Trend Data

Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2019 by K. Rupp

Taken from: www.semianalysis.com/p/a-century-of-moores-law.

Introduction to Readout Electronics
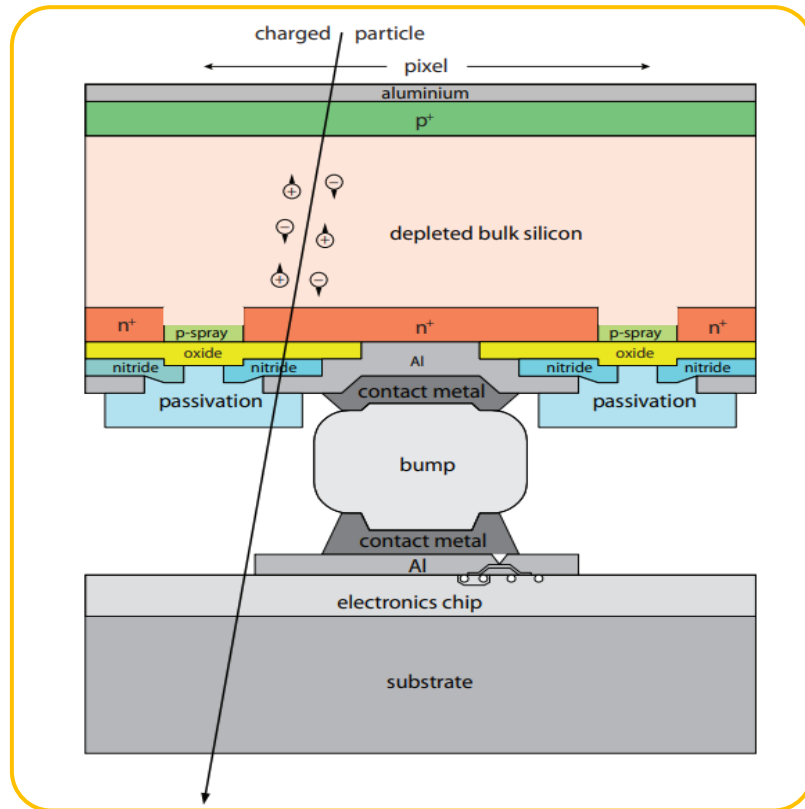
Individual pixel cross-section and readout electronics connected through a bump-bond.
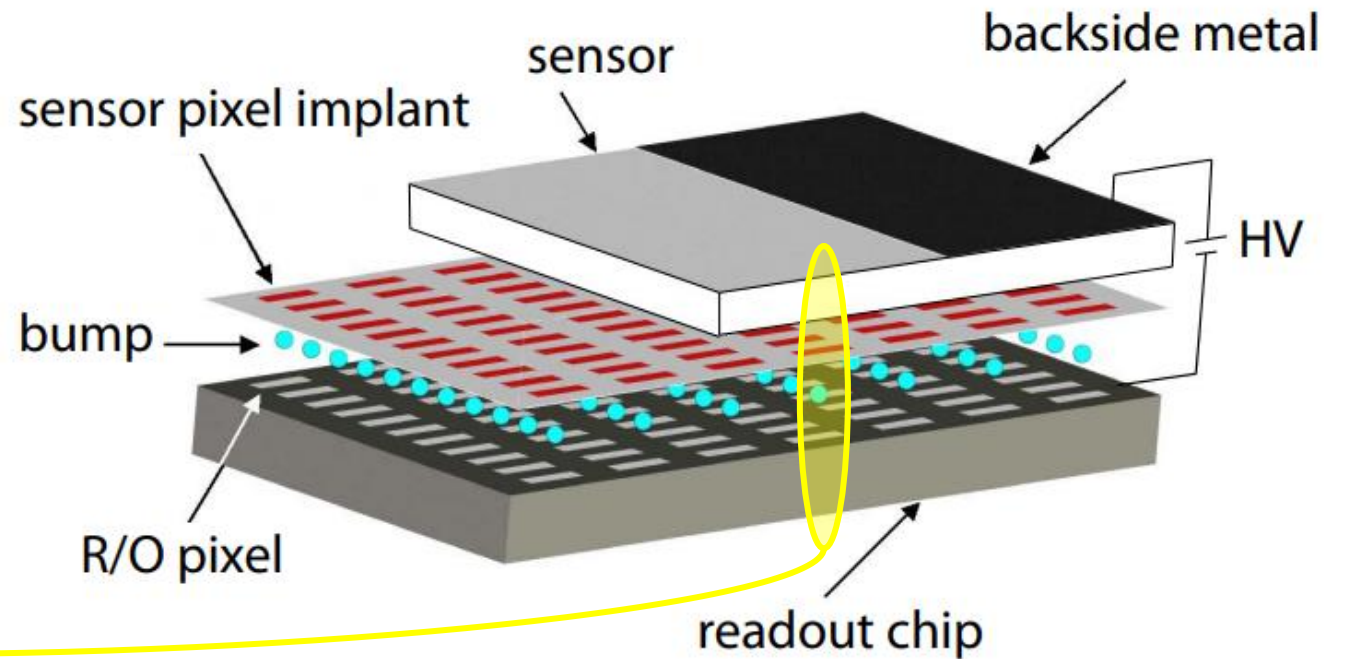
Representation of a hybrid pixel detector matrix ASIC (taken from: [2])

Introduction to Readout Electronics

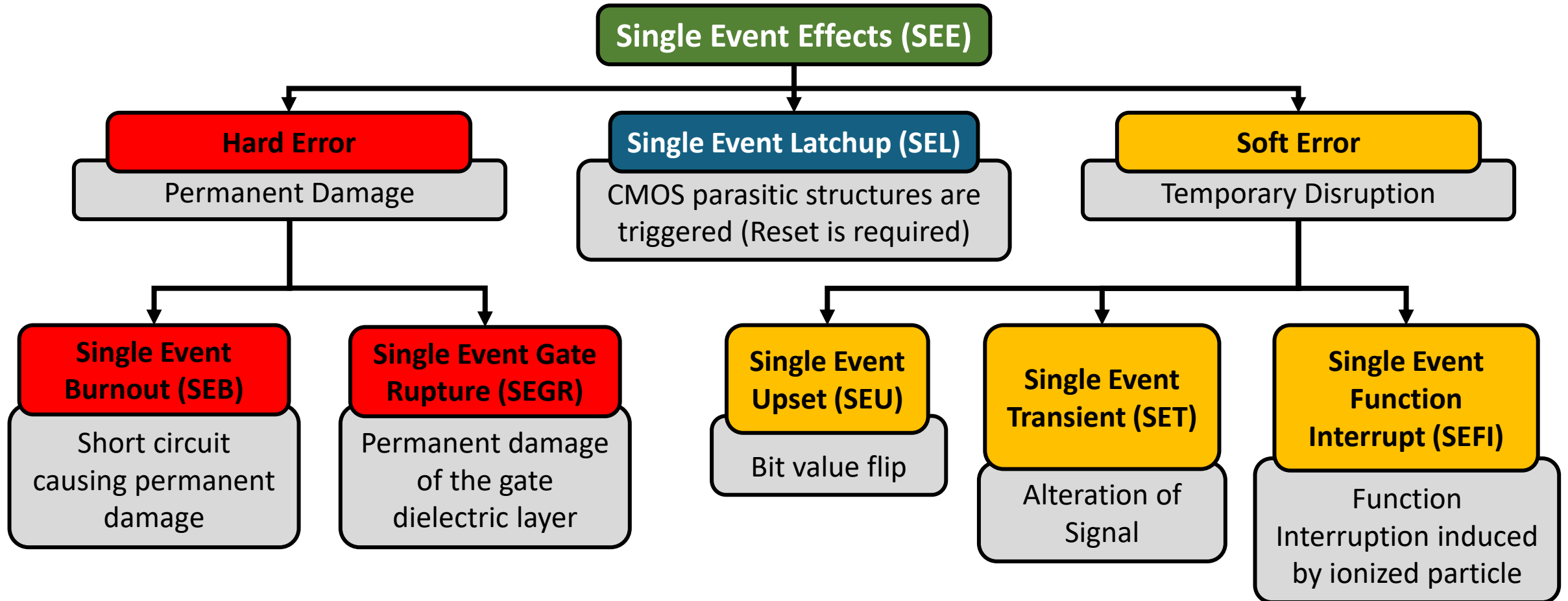**Ionizing Radiation Impact on Readout Electronic Circuits:**

Surface Damage ⚡

- Alters transistor characteristics (threshold, transconductance).
- High leakage currents.
- High risk of activating parasitic transistor structures.

Charge Deposition ⚡

- Single Event Effects (SEE).
- Bit value flipping – Information corruption (Single Event Upsets - SEU).
- High risk of triggering parasitic thyristor structures (Single Event Latchup – SEL).

Introduction to Readout Electronics

Hochschulpartnerschaften mit Griechenland 2023-2025
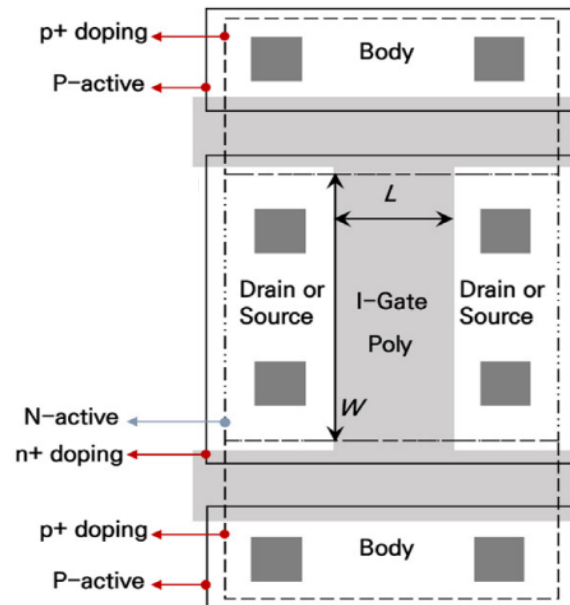
Introduction to Readout Electronics

Surface Damage ⚡
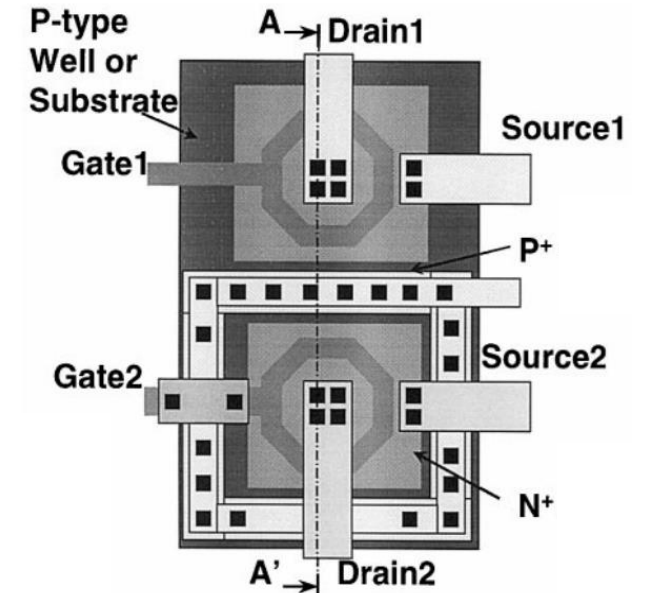
- Alters Transistor DC Characteristics
- High Leakage Currents
- High Risk of Activating Parasitic Transistor Structures

Radiation-Hardened Transistor Structures

I-gate NMOS structure
(taken from: [3])

Enclosed Layout Transistor (ELT)
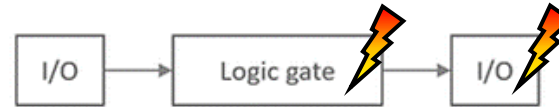structure (taken from: [4])

Introduction to Readout Electronics

Charge Deposition ⚡
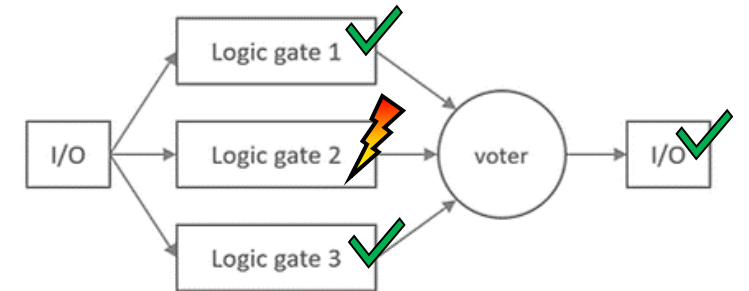
Single Event Effects (SEE)

Single Event Upsets (SEU) - Information Corruption

Single Event Latchup (SEL) - High risk of triggering parasitic structure in transistors
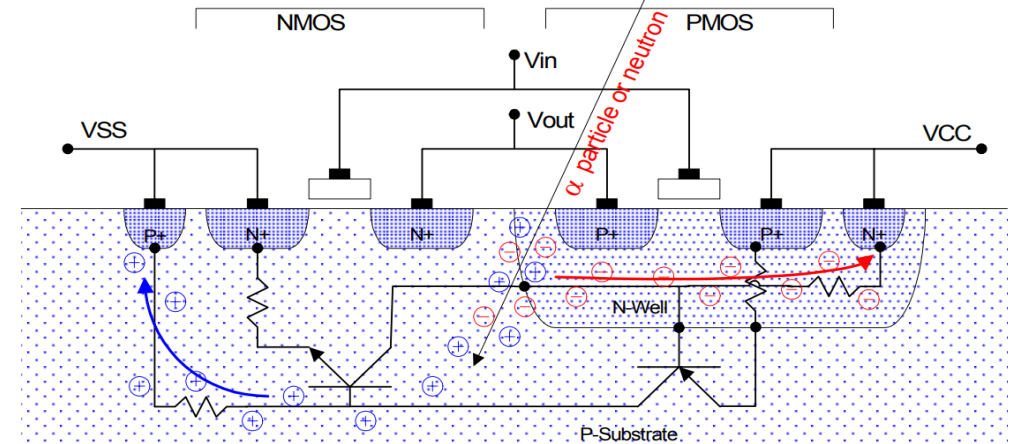

No Redundancy

Triple Modular Redundancy (TMR)

Latchup triggering by ionizing radiation in a typical CMOS structure (taken from [5])

1. Introduction to Readout Electronics
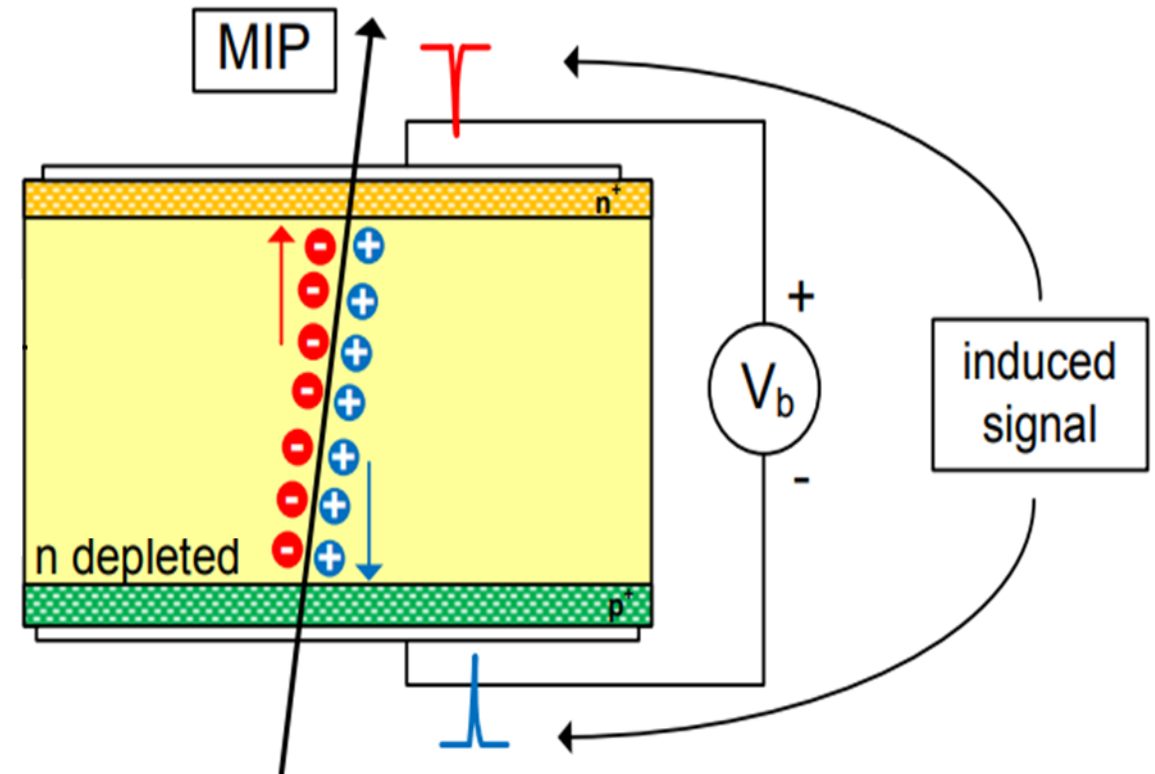
2. Planar and 3D Pixel Detectors

3. Analog Front-End Circuitry and Analysis

4. Readout Front-End ASIC Design

5. Conclusion and Discussion

Planar and 3D Pixel Detectors

- An electric field is applied to sensor electrodes.

- Charge carriers are drifting towards the electrode with the most favorable potential.

- A current signal is induced at both electrodes which can be read out.

Depleted sensor diode with ionized e/h pairs along the MIP track
(taken from: [6])

Planar and 3D Pixel Detectors
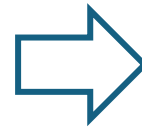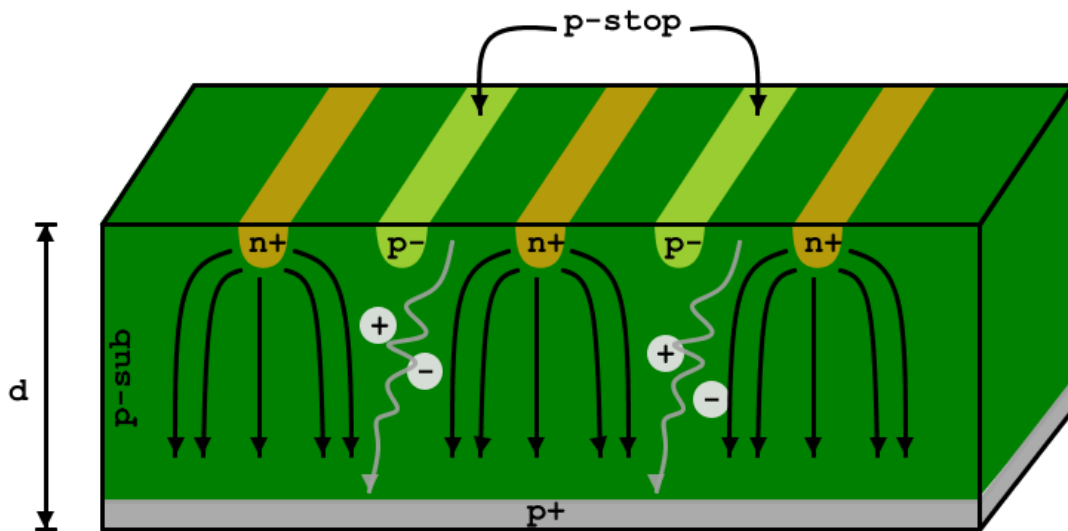
Planar Pixel Sensor

Pros
- Low detector capacitance
- Low charge losses

Cons
- High voltages for full depletion
- Collected charges are sensor thickness dependent

Planar and 3D Pixel Detectors
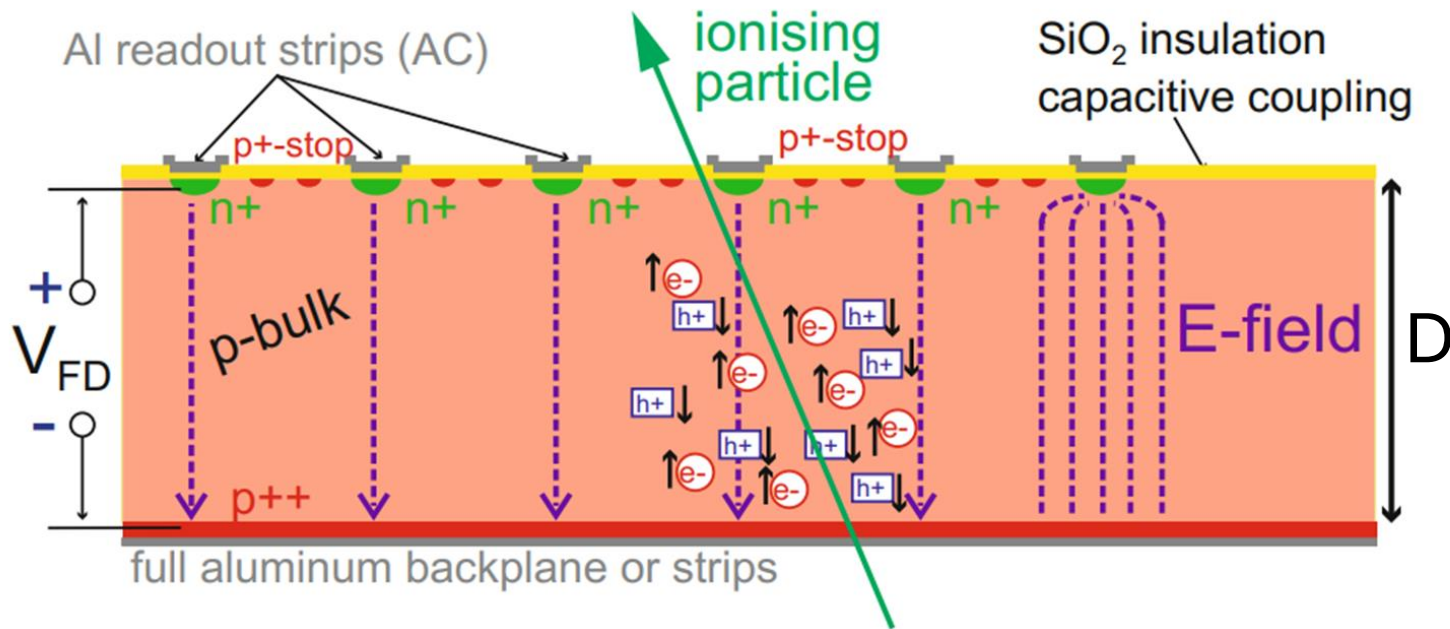
Working principle of an n-in-p AC-coupled silicon microstrip detector (taken from: [7])
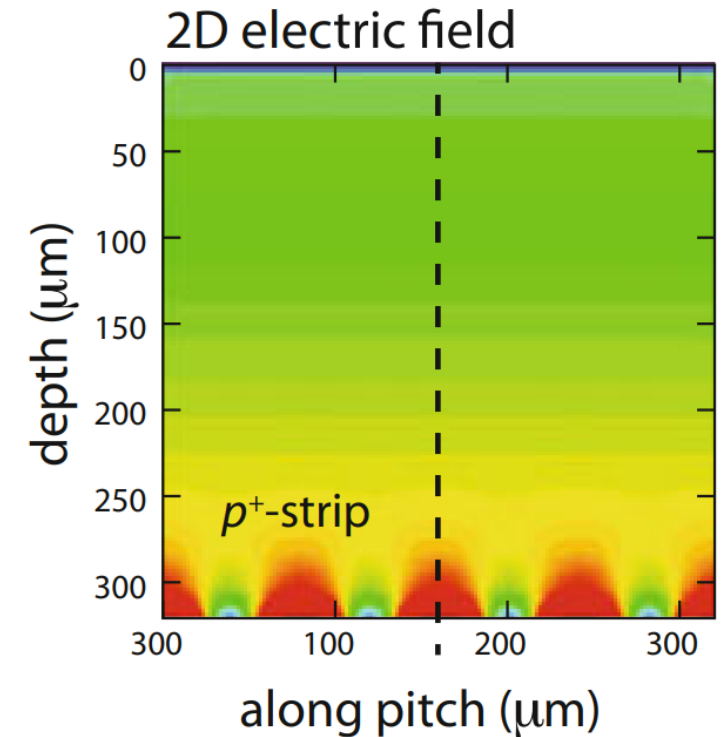
Two-dimensional electric field configuration (taken from: [7])

Planar and 3D Pixel Detectors
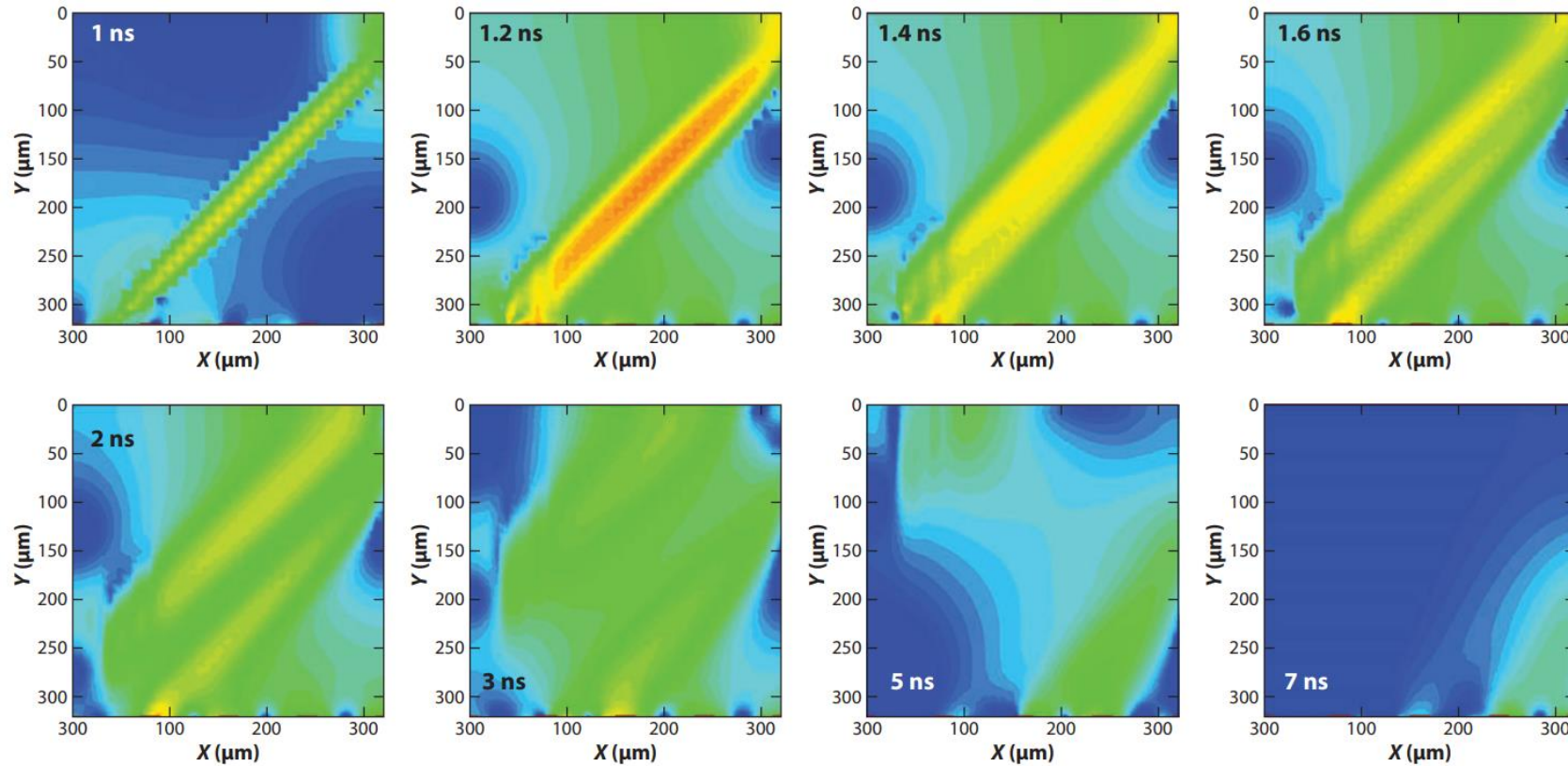
Time evolution of the absolute charge densities of the e/h generated by an ionizing particle passing through the sensor at a 45° angle (taken from [8]).

Planar and 3D Pixel Detectors
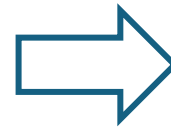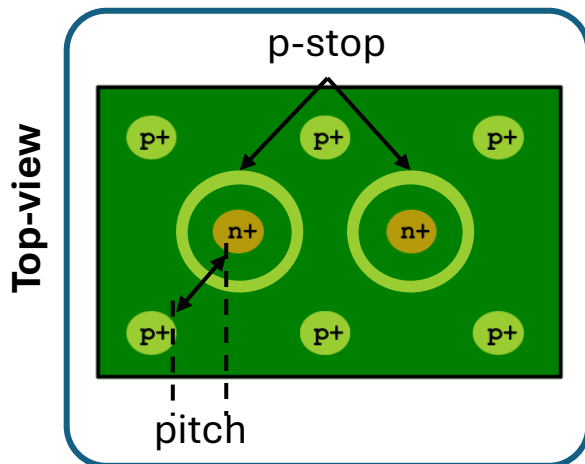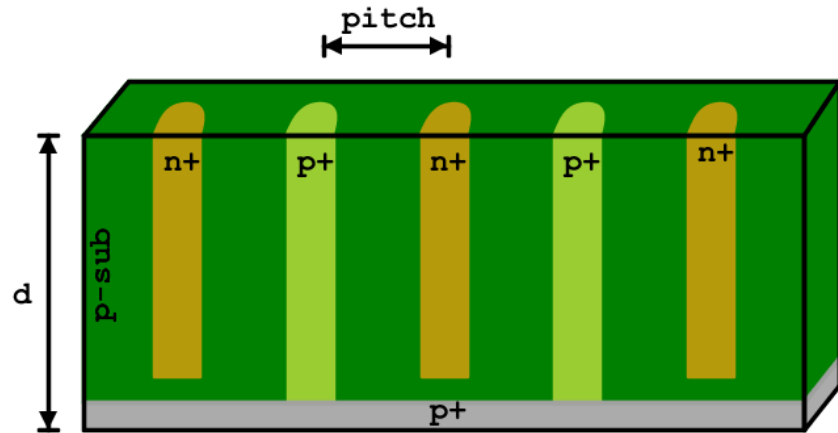
3D Pixel Sensor

Pros

Collected charges are pitch-dependent rather than sensor's thickness dependent

Can be fully depleted using a lower voltage when compared to planar

Cons

Higher detector capacitance

Higher manufacturing complexity

Planar and 3D Pixel Detectors
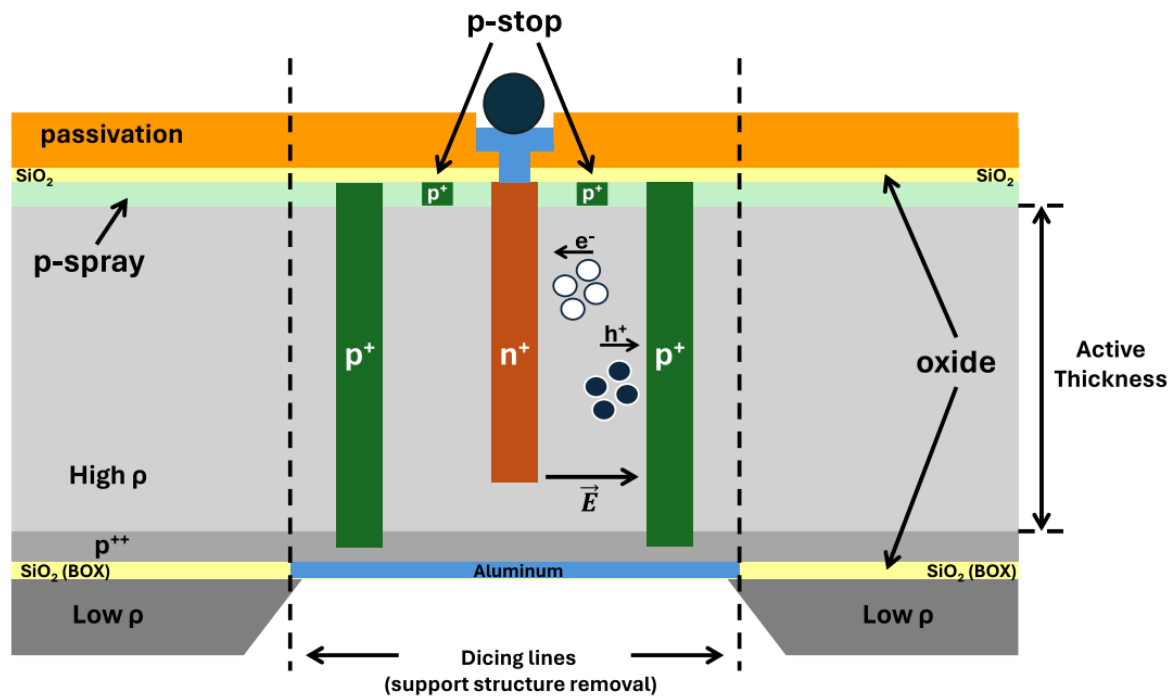
Cross-section of a 3D silicon detector pixel
(taken from: [9])

15200 μm
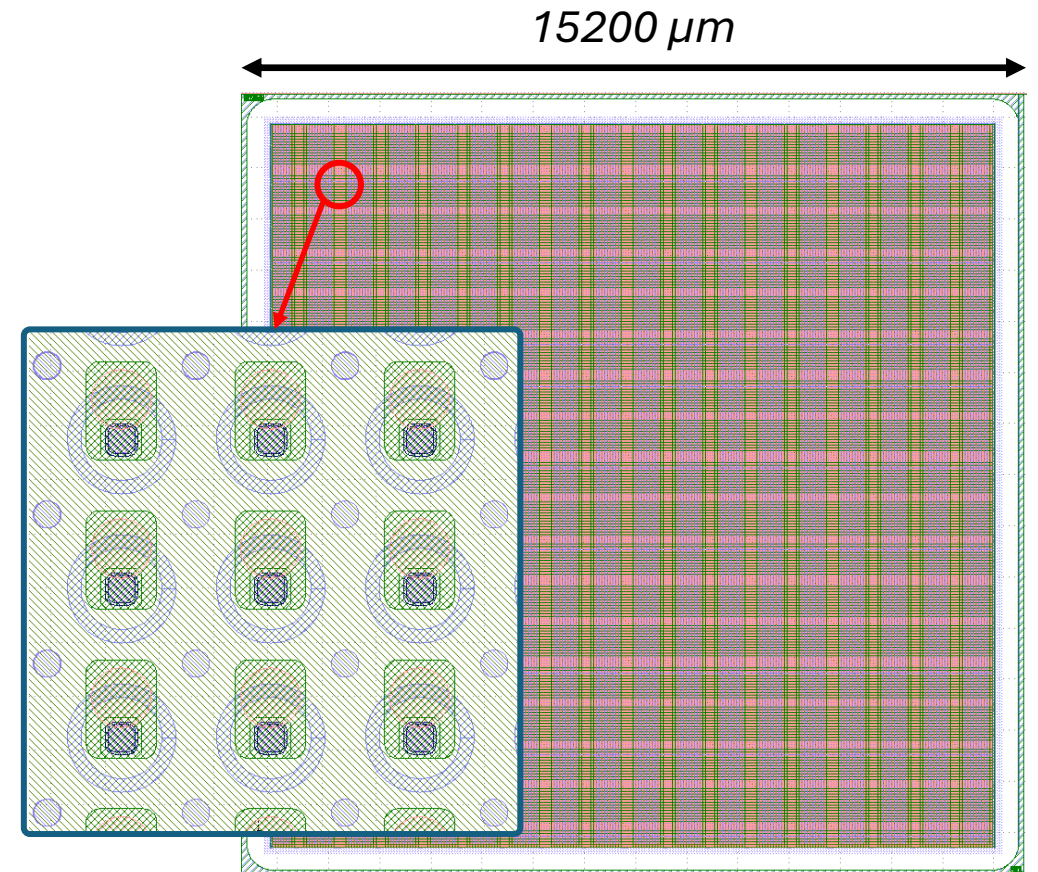
Planar and 3D Pixel Detectors
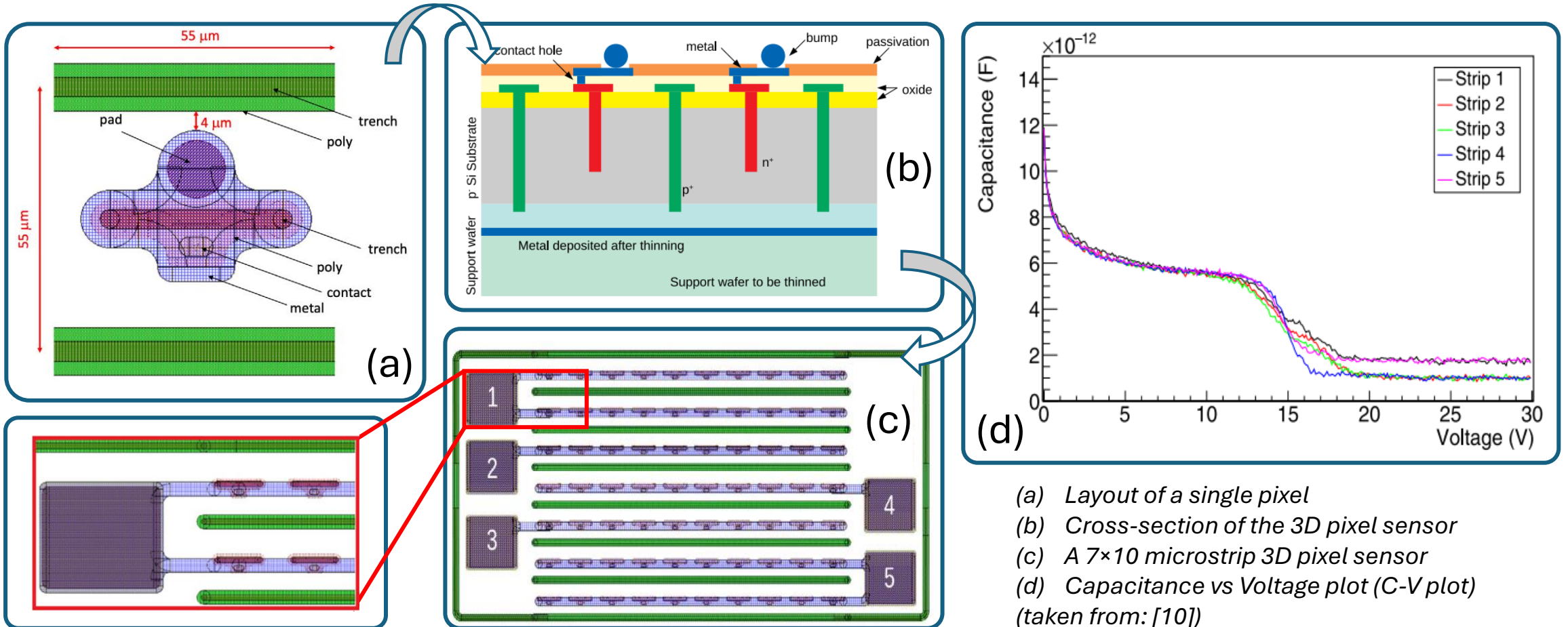
(a) Layout of a single pixel
(b) Cross-section of the 3D pixel sensor
(c) A 7×10 microstrip 3D pixel sensor
(d) Capacitance vs Voltage plot (C-V plot)
(taken from: [10])

Planar and 3D Pixel Detectors
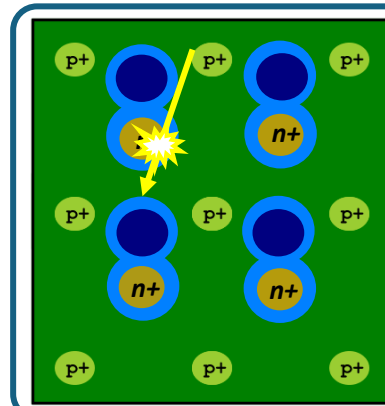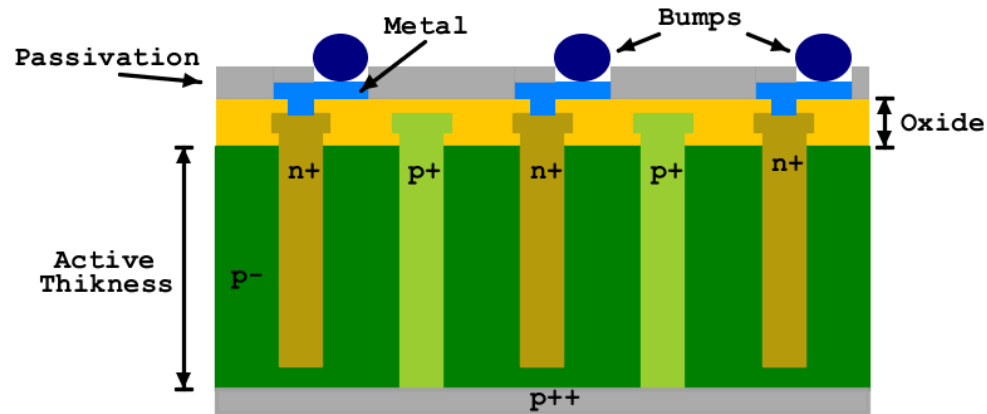
Most Probable Value (MPV)

- MPV is the most probable value of charges that the specified sensor can generate.

- MPV mostly depends on the bias voltage and the type of the silicon sensor.
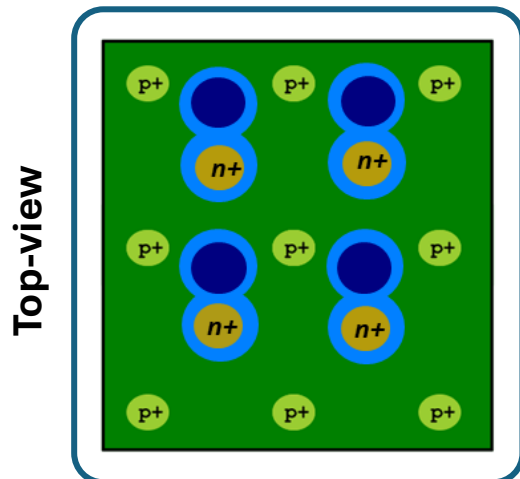
Charge Sharing

- e/h generation is created in a larger proximity from the n+ columns of each pixel.

- The generated charges were split between each pixel.

- A small fraction of charges is collected by a single pixel.
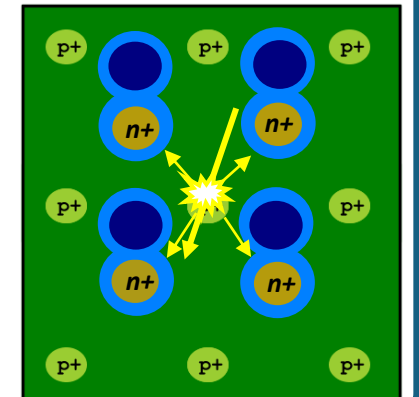
1. Introduction to Readout Electronics

2. Planar and 3D Pixel Detectors

3. Analog Front-End Circuitry and Analysis

4. Readout Front-End ASIC Design

5. Conclusion and Discussion

Analog Front-End Circuitry and Analysis

- In 3D pixel detector schemes, where timing precision is needed, the response time of the analog front-end circuit is crucial, and it should not be significantly degraded due to high detector capacitance.
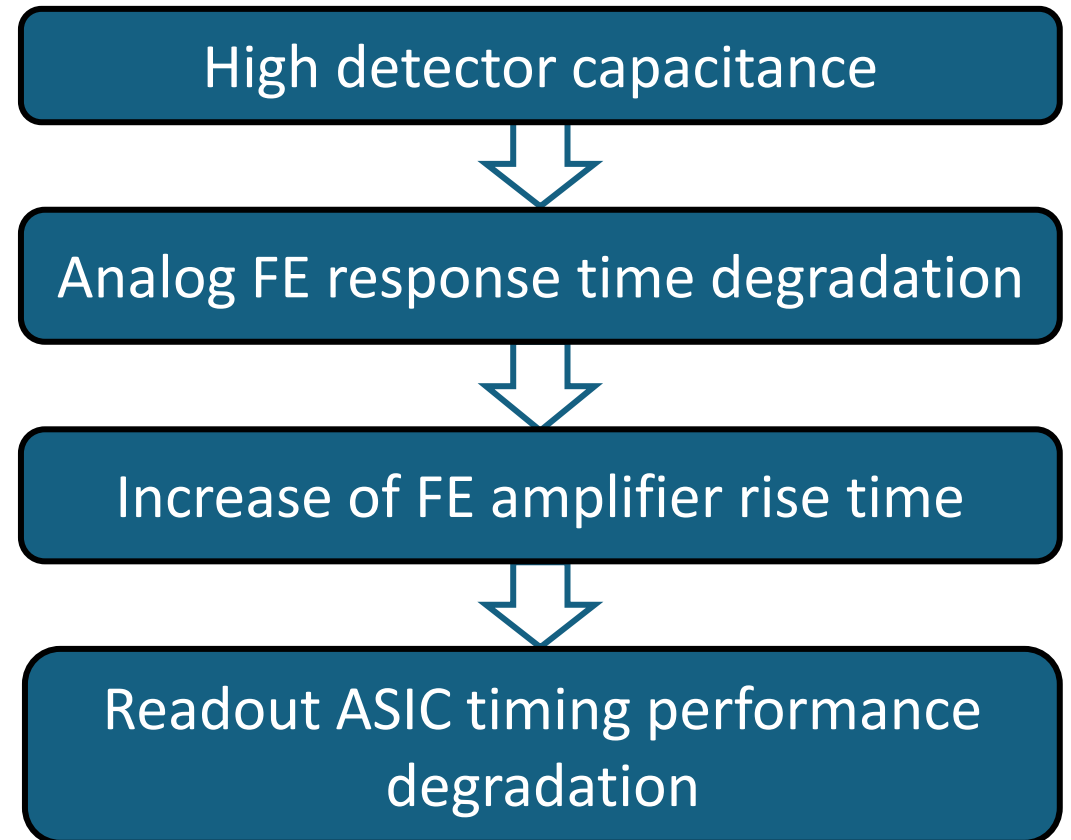
```
┌─────────────────────────────────┐
│      High detector capacitance    │
└─────────────────────────────────┘
                 ⬇
┌─────────────────────────────────┐
│  Analog FE response time degradation │
└─────────────────────────────────┘
                 ⬇
┌─────────────────────────────────┐
│   Increase of FE amplifier rise time │
└─────────────────────────────────┘
                 ⬇
┌─────────────────────────────────┐
│  Readout ASIC timing performance  │
│            degradation            │
└─────────────────────────────────┘
```

Analog Front-End Circuitry and Analysis
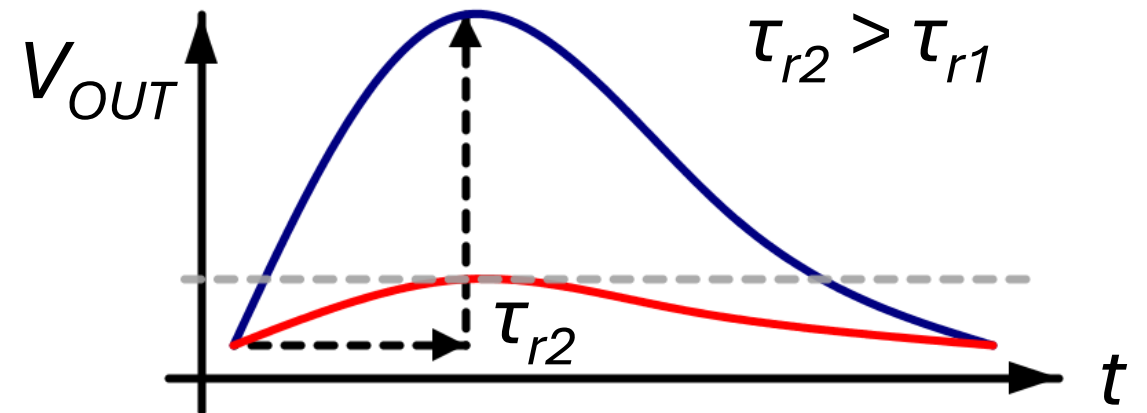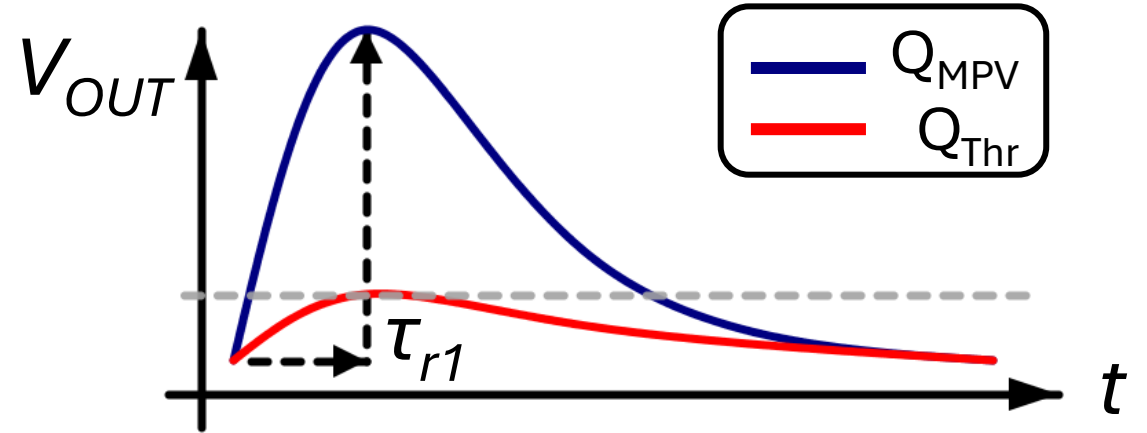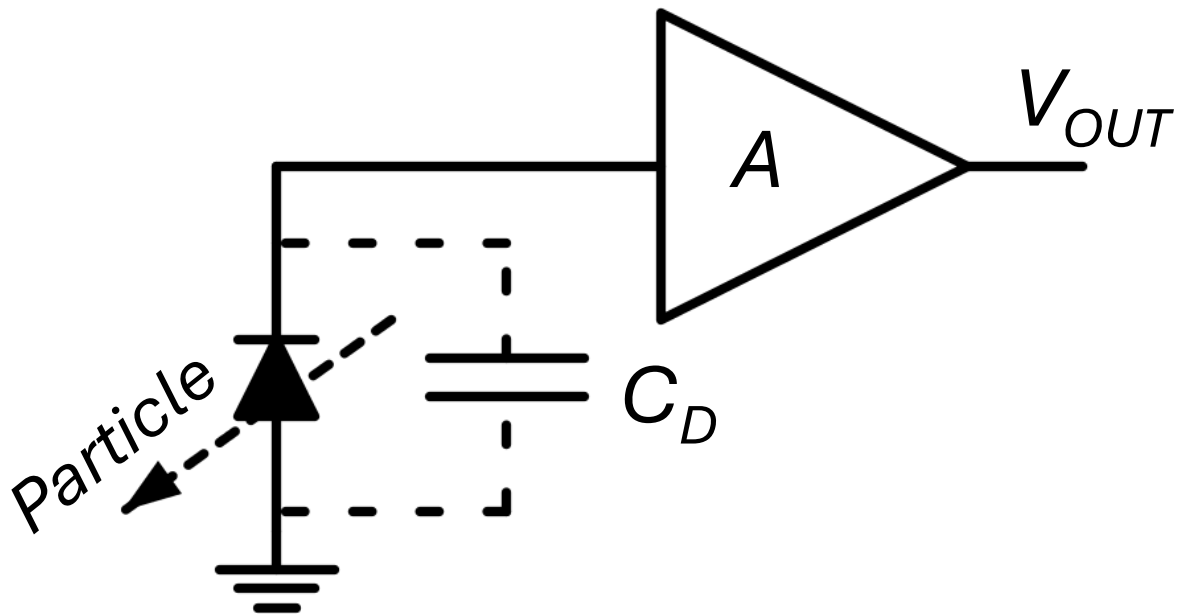
Analog Front-End Circuitry and Analysis

- The **Time-Walk (TW) specification** is of high importance in high timing precision particle detection applications. Fast analog FE response leads to low TW overhead thus higher time precise detection.

Timing response of Analog FE for MPV of input charge (Q_{MPV})

↓

Timing response of Analog FE for minimum detectable input charge (Q_{Thr})

↓

TW = Time difference of MPV and Q_{Thr} while crossing a fixed charge threshold

Analog Front-End Circuitry and Analysis
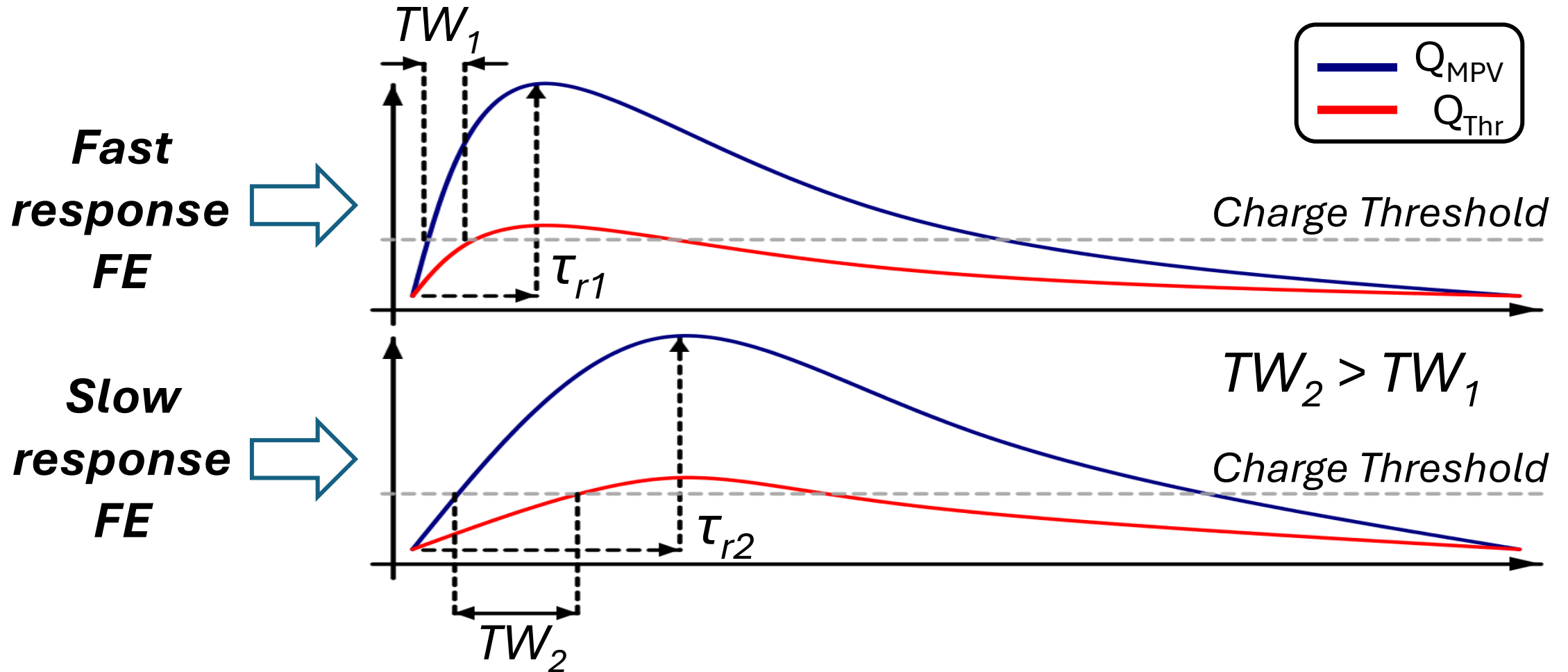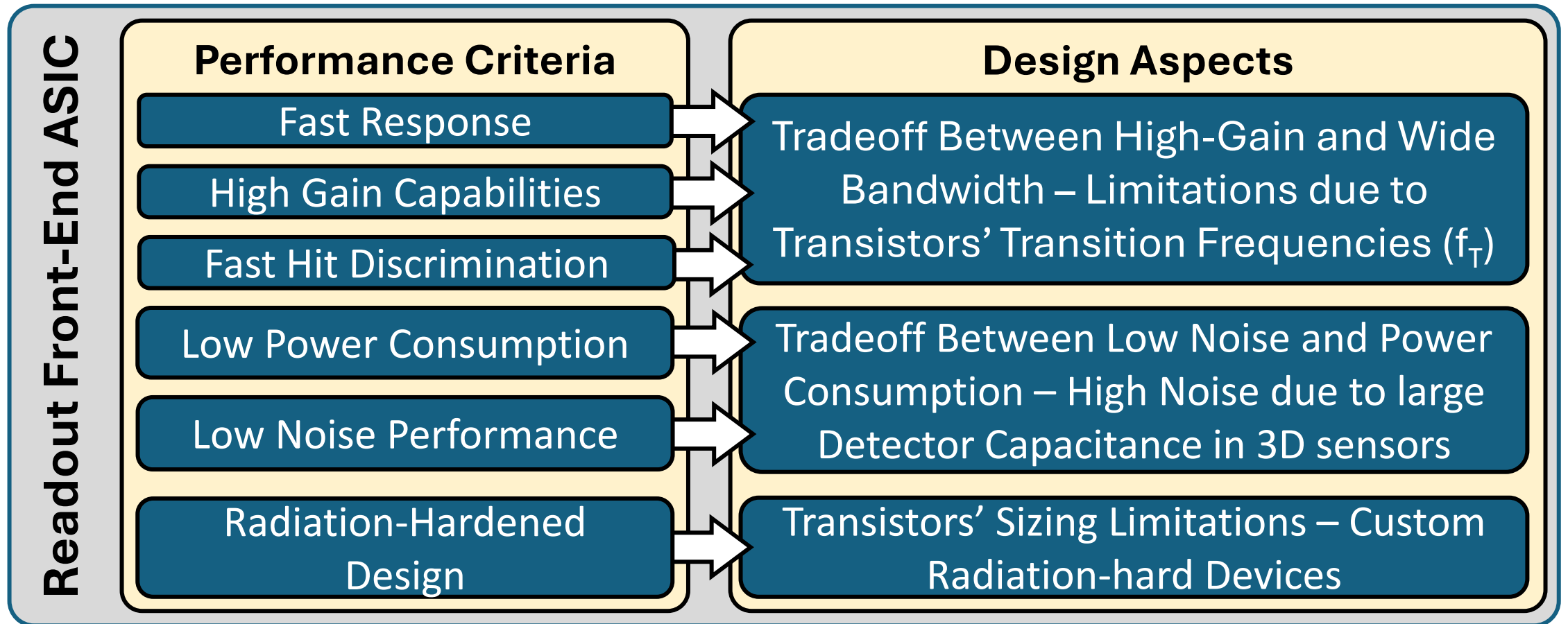
Analog Front-End Circuitry and Analysis

Readout Front-End ASIC

Performance Criteria	Design Aspects
Fast Response	Tradeoff Between High-Gain and Wide Bandwidth – Limitations due to Transistors' Transition Frequencies (f_T)
High Gain Capabilities	
Fast Hit Discrimination	
Low Power Consumption	Tradeoff Between Low Noise and Power Consumption – High Noise due to large Detector Capacitance in 3D sensors
Low Noise Performance	
Radiation-Hardened Design	Transistors' Sizing Limitations – Custom Radiation-hard Devices
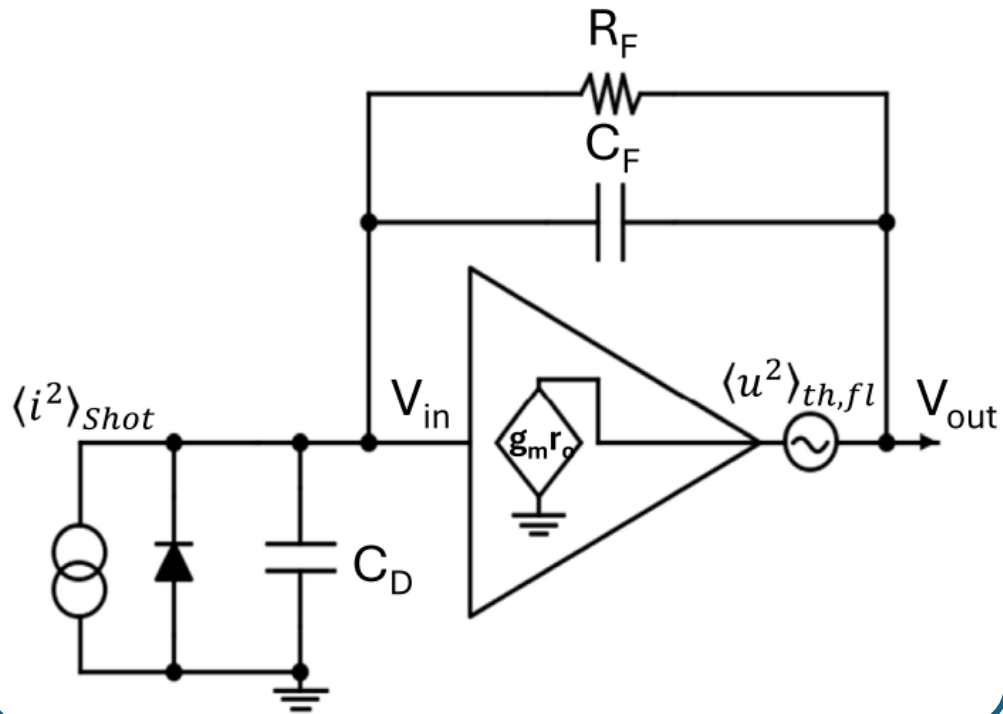
Analog Front-End Circuitry and Analysis
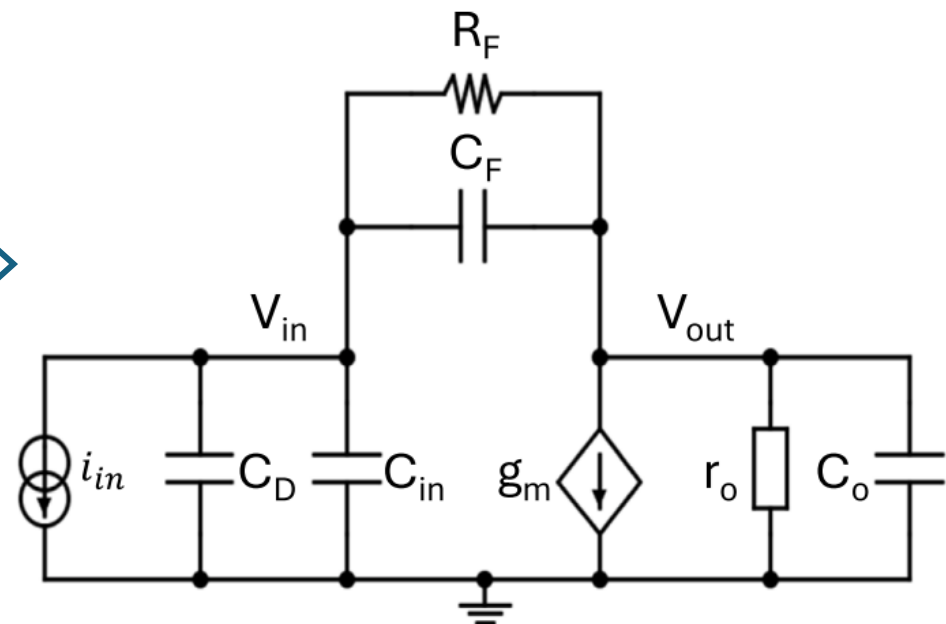
Analog Front-End Circuitry and Analysis

- Output voltage: Integrating input charge (generated into silicon detector) through feedback capacitor C_F,

$$v_{out} = \frac{1}{C_F} \int_0^\infty i_F dt = \frac{q_F}{C_F} \implies V_{out} = \frac{I_F}{sC_F}$$

- The above expression assumes that all current, generated in the sensor, **flows only through C_F**, without flowing though C_D, C_{in} or R_F.

Small-Signal Equivalent Circuit
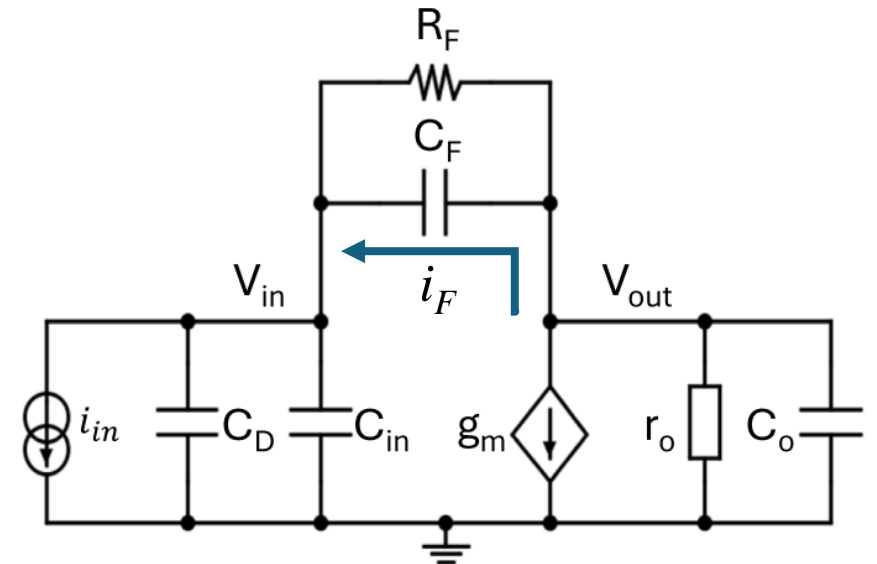
Analog Front-End Circuitry and Analysis

$$v_{\text{out}} = \frac{1}{C_F} \int_0^{\infty} i_F \, dt = \frac{q_F}{C_F} \implies V_{out} = \frac{I_F}{sC_F}$$

- The magnitude of the output voltage is **directly proportional** to the input charge q_F (generated into the sensor) and **inversely proportional** to the feedback capacitance C_F.

Small-Signal Equivalent Circuit
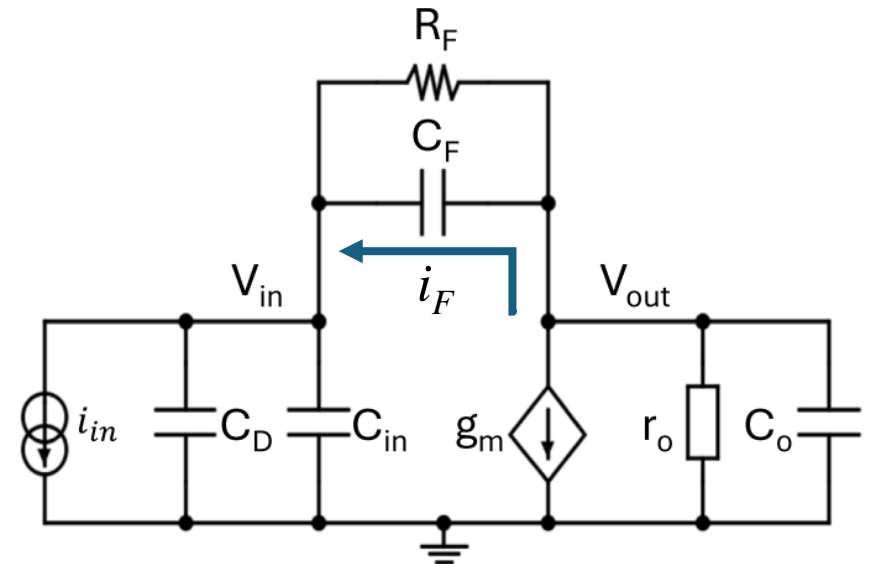
Analog Front-End Circuitry and Analysis

- A more precise expression of the CSA's transfer function by **including both feedback resistor R$_F$ and detector capacitance C$_D$** into the calculations:

$$I_{in} = I_F - I_D = \frac{V_{out}(1+A)}{A \times Z_F} + \frac{s(C_D + C_{in})V_{out}}{A}$$

$$= \frac{V_{out}\left(sZ_F(C_D + C_{in}) + A + 1\right)}{A \times Z_F}$$

- The input charge is integrated on both C$_D$ and C$_F$ capacitors.

Small-Signal Equivalent Circuit
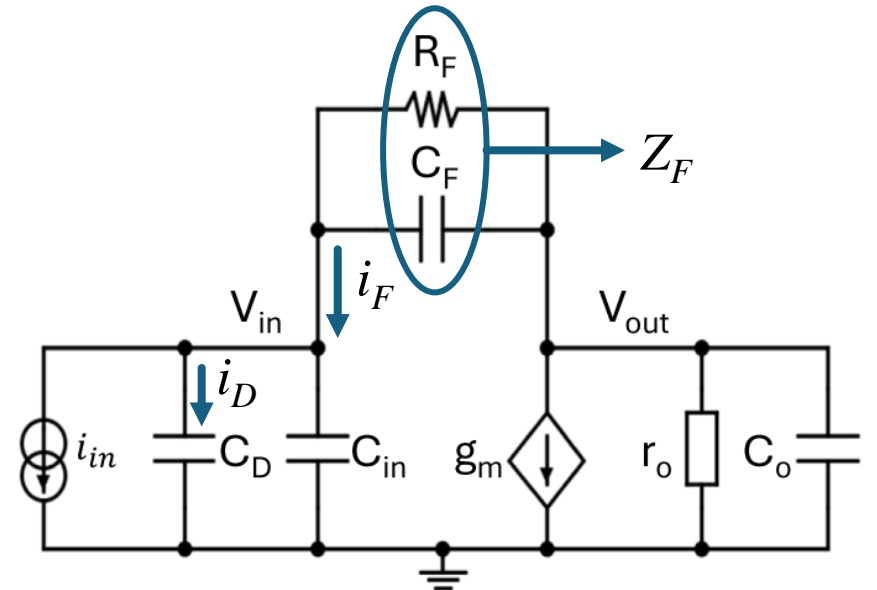
Analog Front-End Circuitry and Analysis

- The feedback complex impedance of the CSA with continuous reset:

$$Z_F = R_F / (1 + s R_F C_F)$$

- Substituting the complex feedback impedance, the transfer function H(s) of the CSA with continuous reset can be expressed:

$$H(s) = \frac{V_{out}}{I_{in}} = \frac{A \times R_F}{s R_F \left((1+A)C_F + C_D + C_{in}\right) + A + 1}$$

Small-Signal Equivalent Circuit
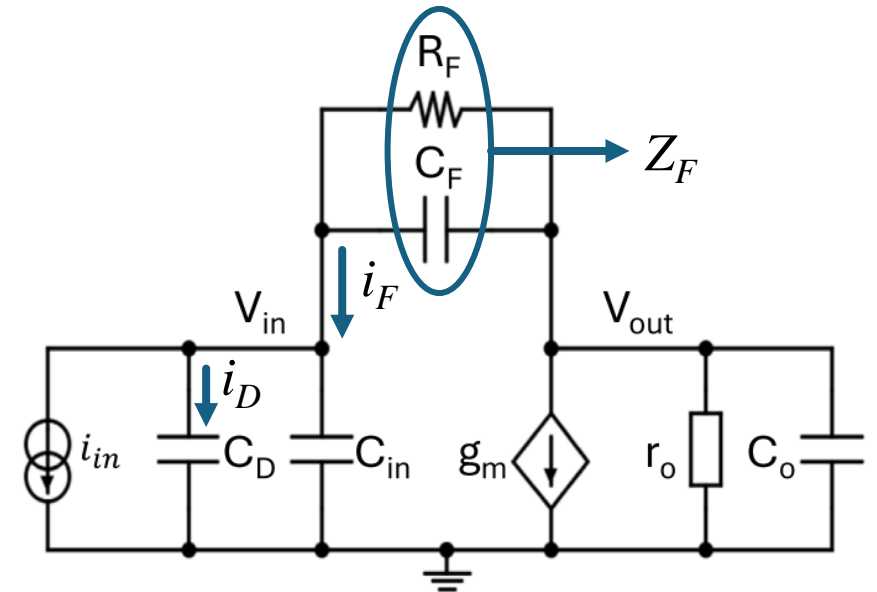
Analog Front-End Circuitry and Analysis

- Still, the output capacitance C_o and output impedance r_o were not included in the calculations of the CSA.

- Exploiting the admittance matrix from nodal analysis:

$$\begin{pmatrix} s\left(C_D + C_{in} + C_F\right) + 1/R_F & -sC_F - 1/R_F \\ g_m - sC_F - 1/R_F & s(C_F + C_o) + 1/R_F + 1/r_o \end{pmatrix} \cdot \begin{pmatrix} v_{in} \\ v_{out} \end{pmatrix}$$
$$= \begin{pmatrix} i_{in} \\ 0 \end{pmatrix}$$

Small-Signal Equivalent Circuit
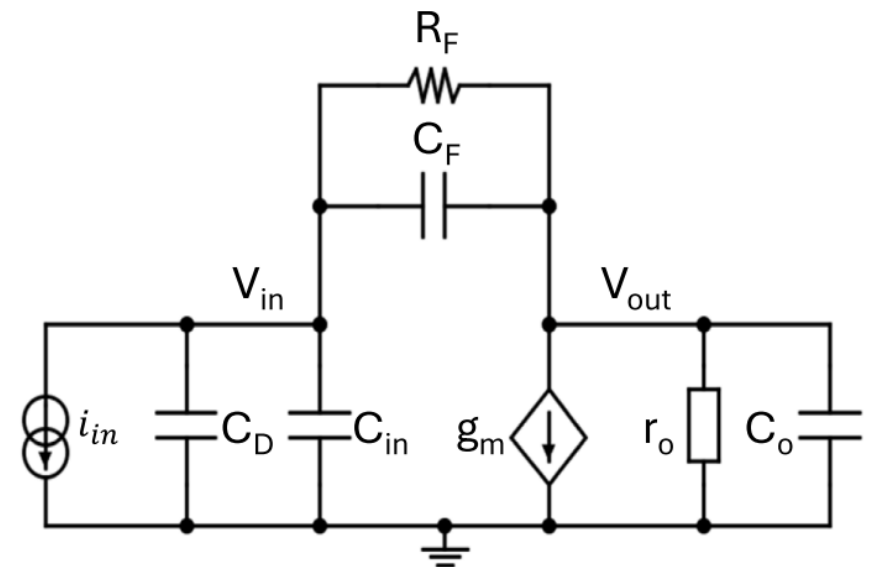
Analog Front-End Circuitry and Analysis

- Assuming next stage circuitry is **a high-impedance input node** (unity-gain buffer), the output resistance of the CSA is practically equal to r_o.

- A high-gain implementation implies that:

$$g_m r_o \gg 1$$

Small-Signal Equivalent Circuit

High Impedance node (buffer)
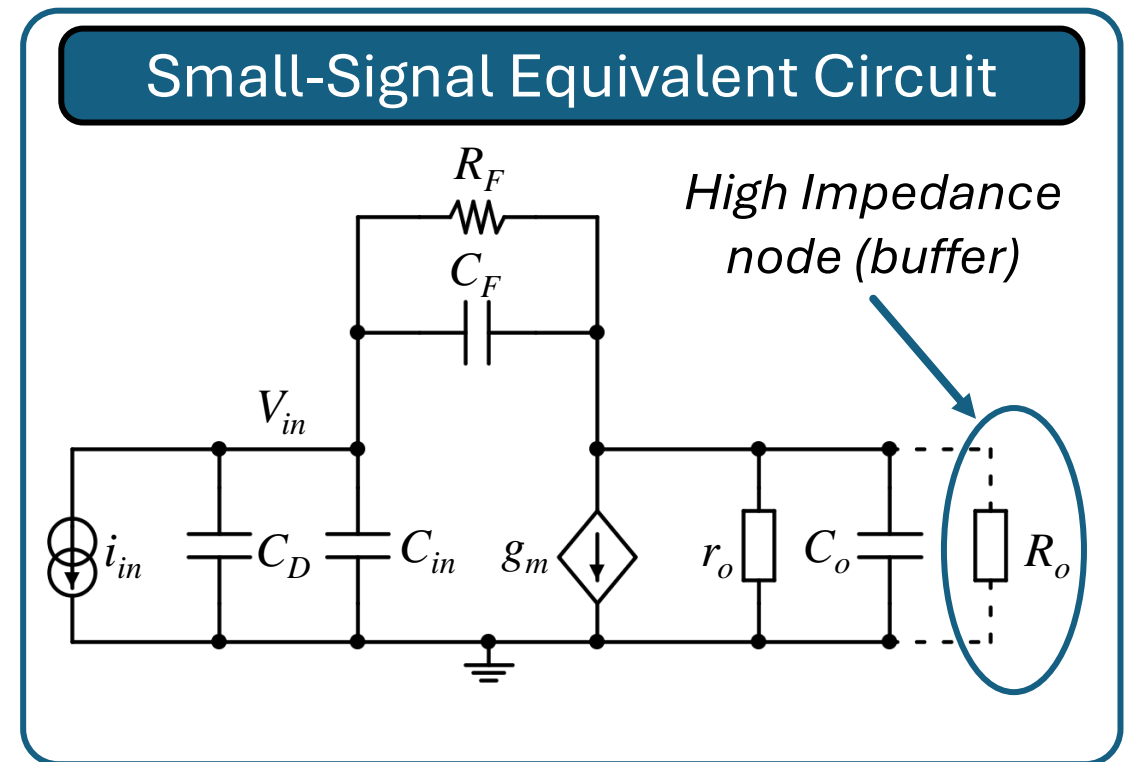
Analog Front-End Circuitry and Analysis

- Considering g_mr_o >> 1 and applying the Cramer's rule, the CSA transfer function with continuous reset can be approximated as:

$$H(s) = \frac{v_{out}}{i_{in}} = -\frac{R_F\left(1 - s\frac{C_F}{g_m}\right)}{1 + sR_FC_F + s\left(\frac{C_D+C_{in}+C_o}{g_m}\right) + s^2R_F\left(\frac{C_F(C_D+C_{in}+C_o)+(C_D+C_{in})C_o}{g_m}\right)}$$

Transimpedance Transfer Function

- DC Gain = R_F (s → 0)
- Lowpass Char. (s → ∞)

Two-pole System

CSA's rise time

CSA's fall time
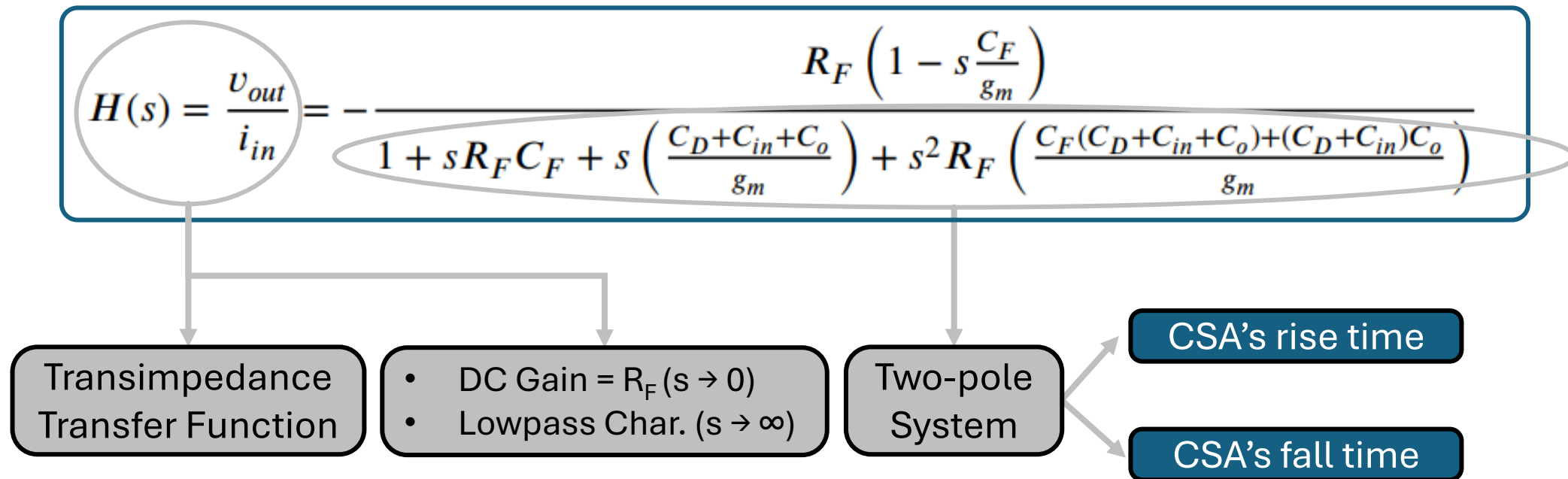
Analog Front-End Circuitry and Analysis

- The full CSA's transfer function with continuous reset is a **two-pole system**:

$$s_{p1,2} = \frac{-(C_D + C_{in} + C_o + g_m R_F C_F)}{2R_F(C_F(C_D + C_{in} + C_o) + (C_D + C_{in})C_o)} \times$$

$$\left(1 \pm \sqrt{1 - \frac{4g_m R_F(C_F(C_D + C_{in} + C_o) + (C_D + C_{in})C_o)}{(C_D + C_{in} + C_o + g_m R_F C_F)^2}}\right)$$

- To simplify the pole expressions, Taylor expansion of the square root can be applied, neglecting higher-order terms:

$$s_{p1} \approx -\frac{C_D + C_{in} + C_o + g_m R_F C_F}{R_F(C_F(C_D + C_{in} + C_o) + (C_D + C_{in})C_o)}$$

$$s_{p2} \approx -\frac{g_m (C_D + C_{in} + C_o + g_m R_F C_F)}{(C_D + C_{in} + C_o + g_m R_F C_F)^2}$$

Analog Front-End Circuitry and Analysis

- An assumption that $R_F C_F \gg (C_{in} + C_o)/g_m$ can be made in cases when the feedback time constant is chosen much higher than the CSA's peaking time (rise time).

- Further simplification of the pole expressions can be made, leading to a good approximation of **the rise and fall times** of the two-pole CSA topology:

CSA's rise time	CSA's fall time
$s_{p1} \approx -\dfrac{g_m C_F}{C_F(C_D + C_{in} + C_o) + (C_D + C_{in})C_o} = -\dfrac{1}{\tau_r}$	$s_{p2} \approx -\dfrac{1}{R_F C_F} = -\dfrac{1}{\tau_f}$

Analog Front-End Circuitry and Analysis

- To calculate the output voltage signal of the CSA with continuous reset, an **inverse Laplace transform** should be performed while assuming a **Dirac-like input current signal** with an integrated **charge of Q$_S$**.

- Hence, CSA's transfer function can be expressed into the time domain as follows:

$$H(s) = \frac{-R_F}{(1 + s\tau_r)(1 + s\tau_f)} \Rightarrow \boxed{V_{out}(t) = -\left(\frac{Q_S}{C_F}\right) \frac{\tau_f}{\tau_f - \tau_r} \left(1 - e^{-t\frac{\tau_f - \tau_r}{\tau_r \cdot \tau_f}}\right) \cdot e^{-\frac{t}{\tau_f}}}$$

Analog Front-End Circuitry and Analysis

- For fast time-response CSA topologies, the rise time is much lower than the fall time and thus, the assumption of $\tau_F \gg \tau_R$ can be made.

- The **Charge-to-Voltage Conversion Gain A_Q** can be defined as:

$$A_Q = \frac{V_{out}}{Q_S} = -\frac{e^{-\frac{t}{\tau_f}}\left(1 - e^{-\frac{t}{\tau_r}}\right)}{C_F}$$

- The point at which **the output voltage has reached its maximum value**, hence A_Q has also reached its maximum value, can be derived by solving:

$$\partial A_Q / \partial t = 0$$

Analog Front-End Circuitry and Analysis

- The time at which the output voltage reaches its **maximum value** can be calculated as follows:

$$A_Q = \frac{V_{out}}{Q_S} = -\frac{e^{-\frac{t}{\tau_f}}\left(1 - e^{-\frac{t}{\tau_r}}\right)}{C_F} \Rightarrow \frac{\partial A_Q}{\partial t} = -\frac{e^{-t\left(\frac{\tau_r + \tau_f}{\tau_r \cdot \tau_f}\right)}\left(\tau_f + \tau_r - \tau_r \cdot e^{\frac{t}{\tau_r}}\right)}{C_F \cdot \tau_f \cdot \tau_r}$$

$$\frac{\partial A_Q}{\partial t} = 0 \Rightarrow t = \tau_r \cdot \ln\left(\frac{\tau_f + \tau_r}{\tau_r}\right)$$

Substituting solution

$$A_Q = -\frac{\tau_f\left(\frac{\tau_f + \tau_r}{\tau_r}\right)^{-\frac{\tau_r}{\tau_f}}}{C_F(\tau_f + \tau_r)}$$

Rise/Fall time ratio dependent

Analog Front-End Circuitry and Analysis

CSA's Output Voltage

$$V_{out} = -\frac{\mathrm{e}^{-\frac{t}{\tau_f}}\left(1 - \mathrm{e}^{-\frac{t}{\tau_r}}\right)Q_S}{\mathrm{C_F}}$$

CSA's Maximum Charge-to-Voltage Gain

$$A_Q = -\frac{\tau_f\left(\frac{\tau_f + \tau_r}{\tau_r}\right)^{-\frac{\tau_r}{\tau_f}}}{C_F\left(\tau_f + \tau_r\right)}$$

Analysis Parameters

	C_F	Q_S	τ_f	τ_r
Min	10 fF	0.1 fC	0.1 ns	10 ps
Max	100 fF	1 fC	10 ns	10 ns

Analog Front-End Circuitry and Analysis

Feedback Capacitance Sweep C_F (Q_S, τ_F = Max & τ_R = Min)

$C_F = 10\ fF$

$C_F = 20\ fF$

$C_F = 100\ fF$
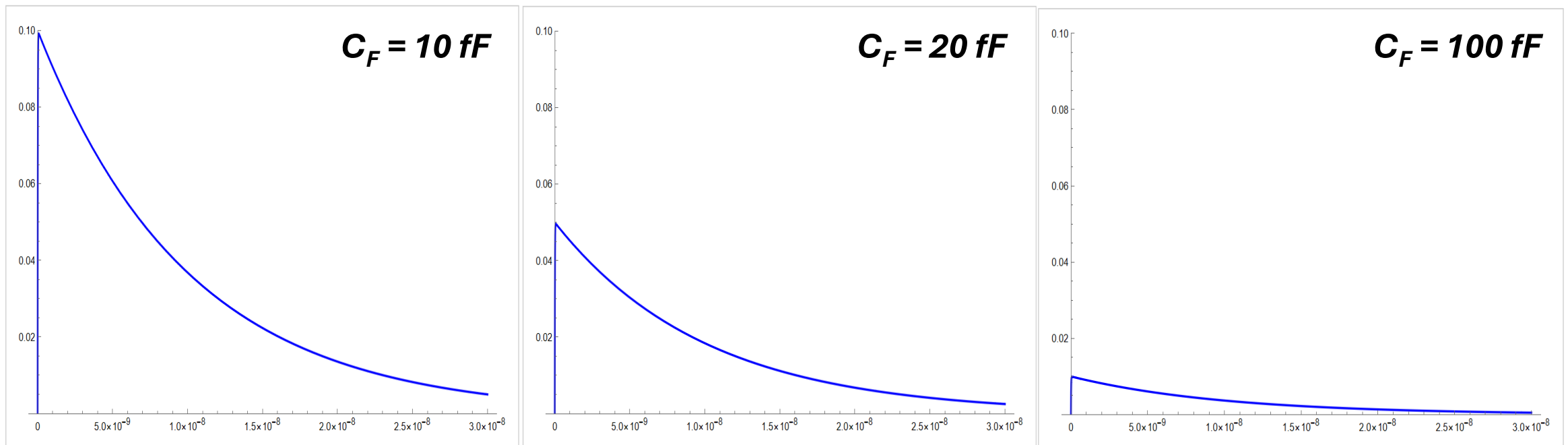
Analog Front-End Circuitry and Analysis

Input Charge Sweep Q_S (τ_F = Max & C_F , τ_R = Min)

Q_S = 0.1 fC

Q_S = 0.5 fC

Q_S = 1 fC
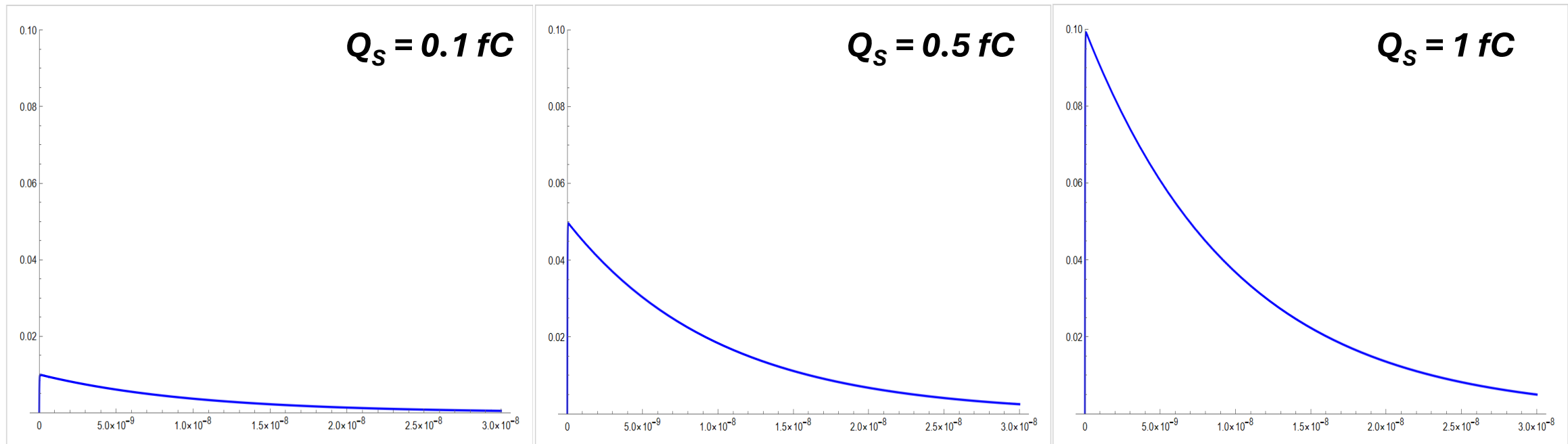
Analog Front-End Circuitry and Analysis

Fall Time Sweep τ_F (Q_S = Max & C_F , τ_R = Min)

τ_F = 10 ns

τ_F = 1 ns

τ_F = 0.1 ns
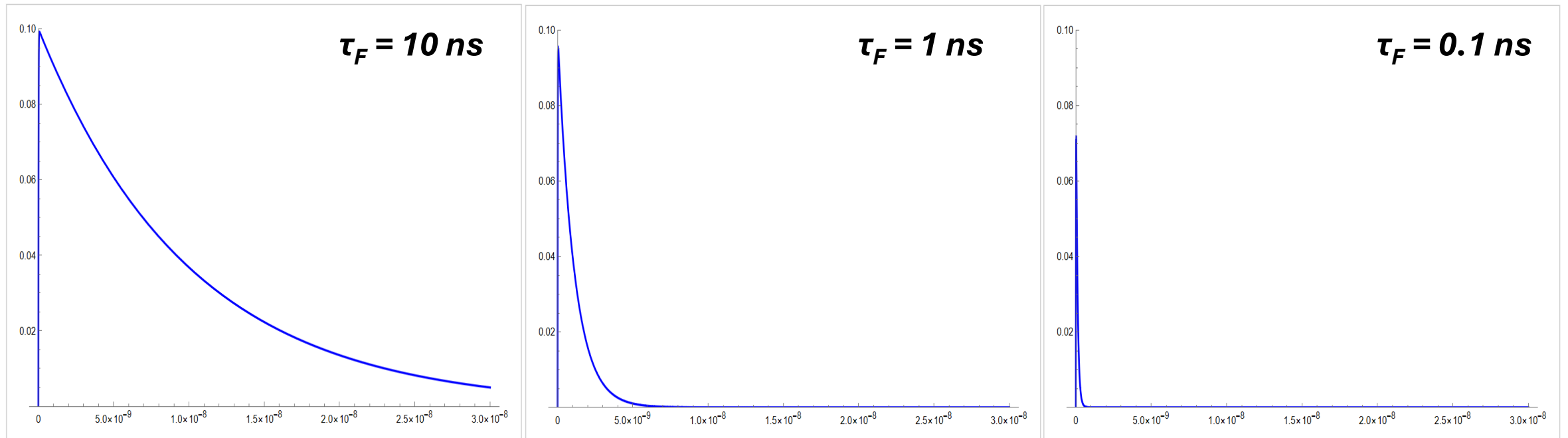
Analog Front-End Circuitry and Analysis

Rise Time Sweep τ_R (Q_S, τ_F = Max & C_F = Min)

$\tau_R = 10\ ps$

$\tau_R = 100\ ps$

$\tau_R = 1\ ns$

Analog Front-End Circuitry and Analysis

Charge-Sensitive Amplifier (CSA)

R_F
C_F
V_{in}
$g_m r_o$
$\langle u^2 \rangle_{th,fl}$
V_{out}
$\langle i^2 \rangle_{Shot}$
C_D

Flicker Noise
1st Gain Stage High Contribution – Dominant at low frequencies

Thermal Noise
1st Gain Stage High Contribution – Dominant at high frequencies

Shot Noise
Sensor's Diode Noise – White noise spectrum
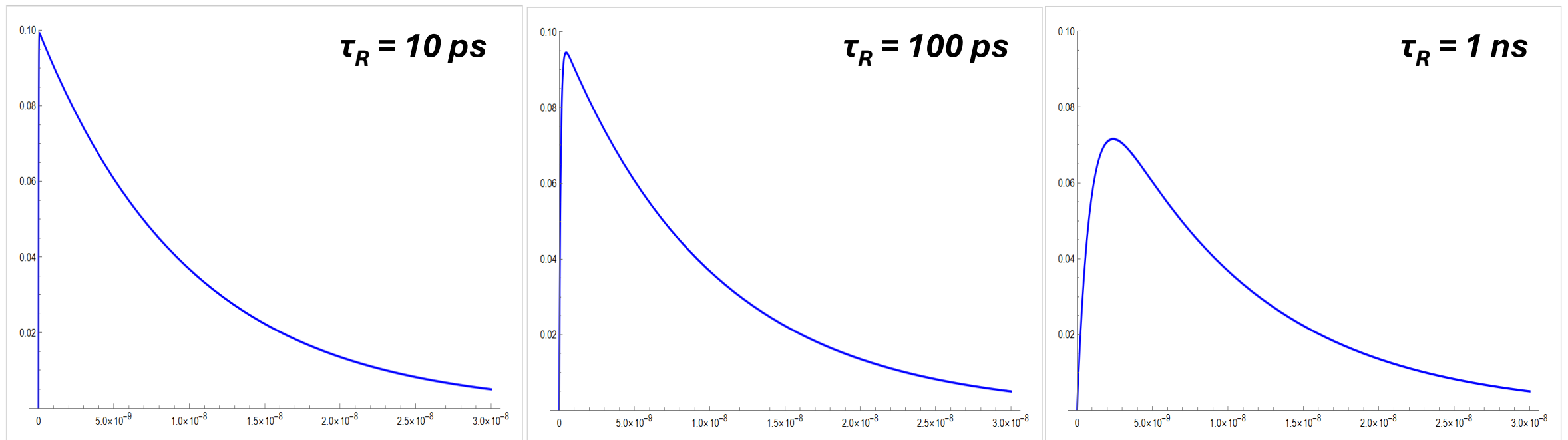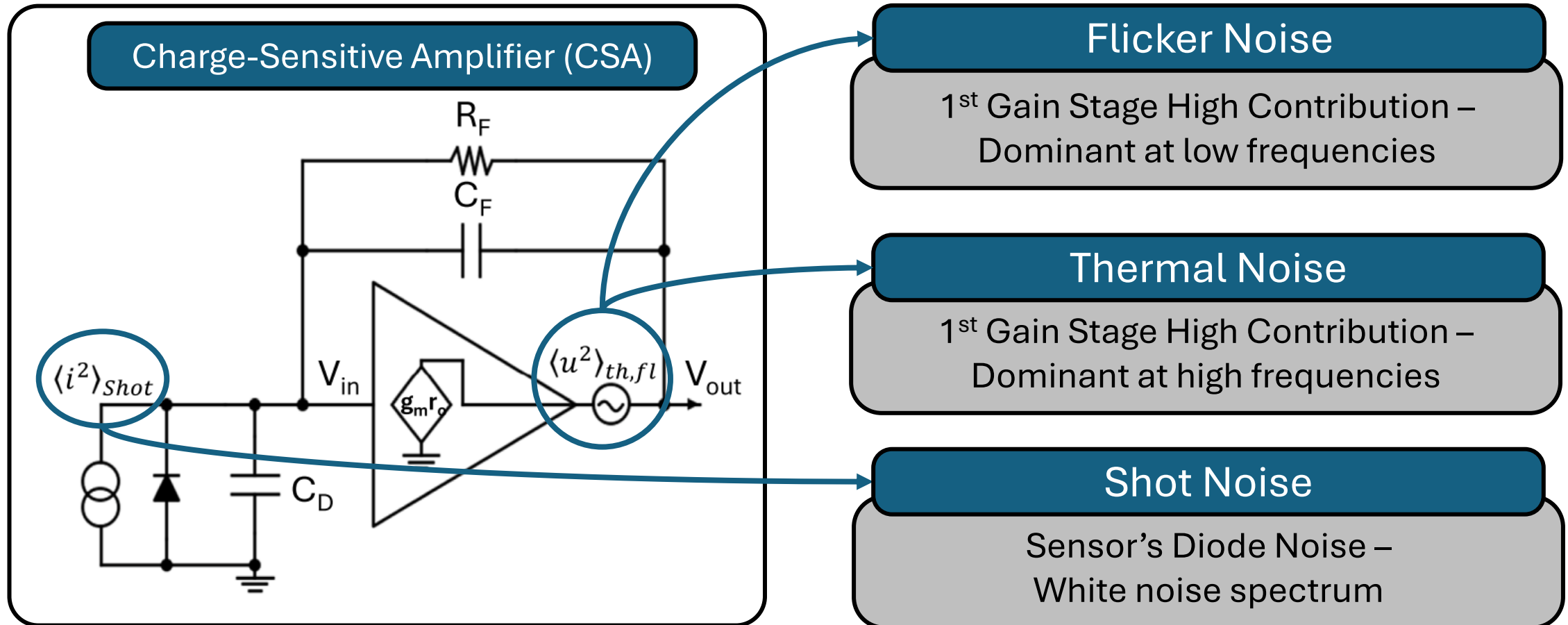
Analog Front-End Circuitry and Analysis

- In readout applications, **Equivalent Noise Charge (ENC)**, expressed in electrons (e⁻), is used to quantify the channel's noise:

$$ENC = \frac{\text{Output Noise (RMS)}}{\text{Induced Output Signal of 1 e}^-} = \frac{\sqrt{\langle v_{out}^2 \rangle}}{\text{Gain(V/e}^-)}$$

- The overall noise contribution is derived from the **superposition** of the detector's diode **shot noise** and the **thermal and flicker noise** contributions of the analog front-end amplification (CSA).

Analog Front-End Circuitry and Analysis

Thermal Noise

- Thermal velocity fluctuations of charge carriers into a conductor with resistance R, due to their thermal kinetic energy at a temperature T.

$$\mathrm{d}\langle i^2 \rangle_{therm} = \frac{1}{R} 4kT \,\mathrm{d}f$$
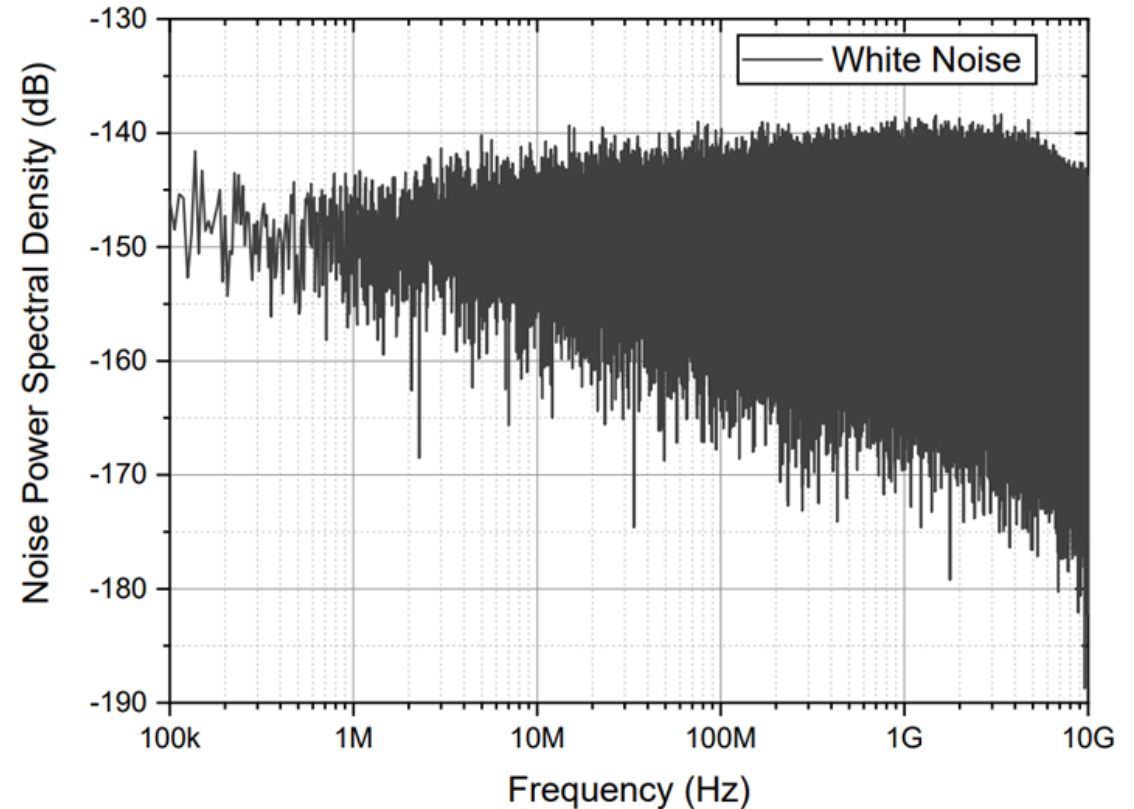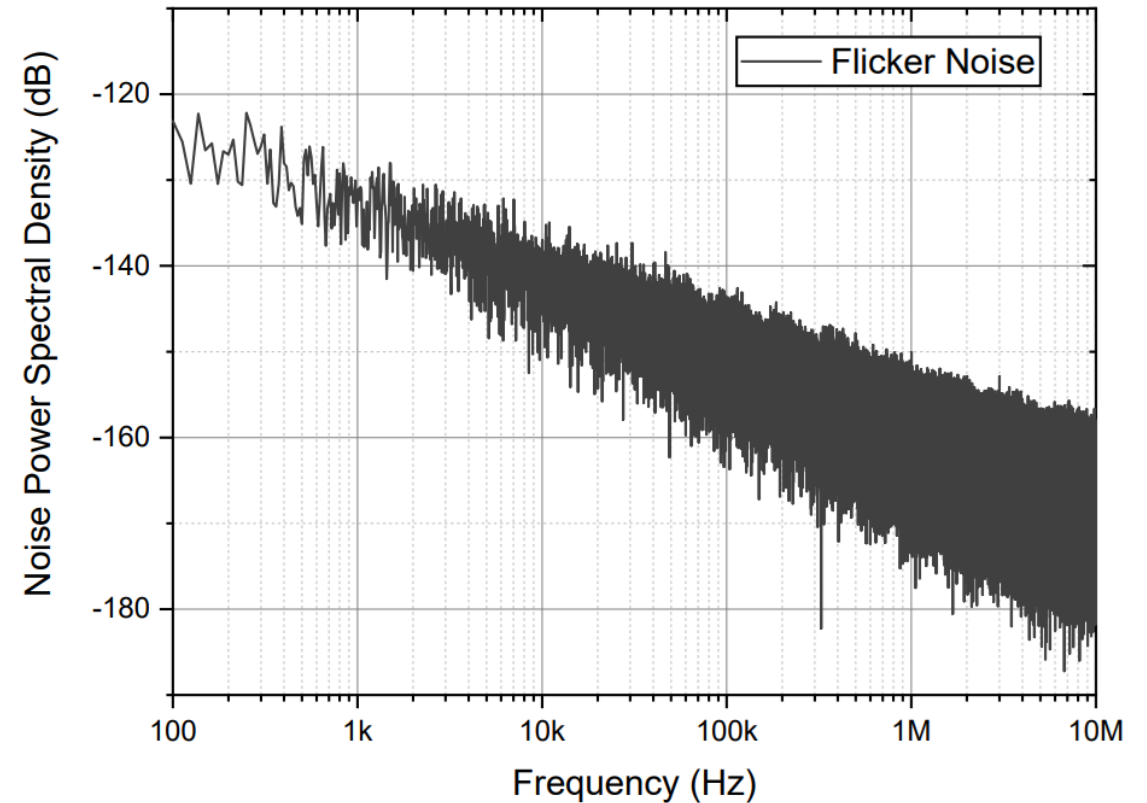

White noise source power spectral density (taken from: [12])

Analog Front-End Circuitry and Analysis

Flicker Noise

- Capture/release processes with different time constants such as charge carrier trapping near the gate-silicon interface of the transistor.

$$\mathrm{d}\langle i^2 \rangle_{\mathrm{flicker}} = K_\alpha \frac{1}{f^\alpha}\mathrm{d}f$$
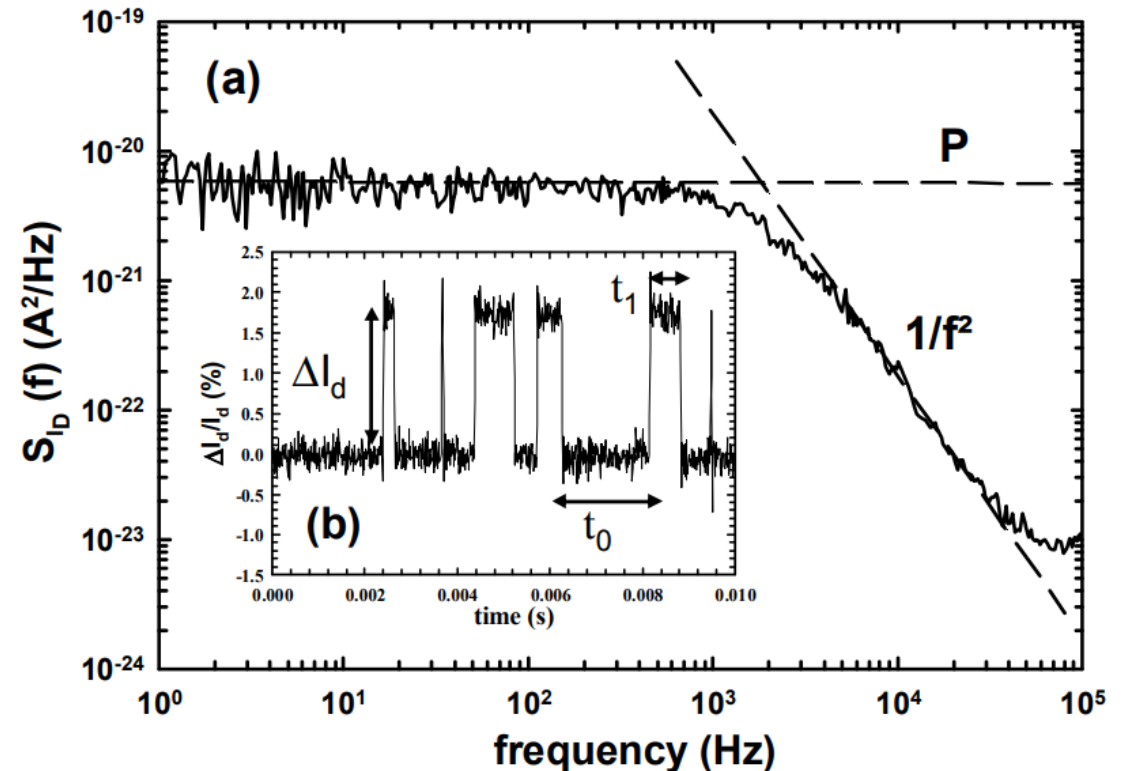

Flicker (1/f) noise power spectral density (taken from: [12])

Analog Front-End Circuitry and Analysis

Shot Noise

- Statistical fluctuations occurring when charges are emitted independently over a potential barrier (electron/hole generation and recombination).

$$d\langle i^2 \rangle_{\text{shot}} = 2eI_0 df$$

(a) Random Telegraph Signal (RTS) noise power spectral density
(b) Relative drain current fluctuations of a small-area MOSFET (taken from: [13])

Analog Front-End Circuitry and Analysis

- Having the MOSFET as reference, the equivalent input series noise, assuming that the transistor is operating into the **saturation region**, is as follows:

$$\frac{\mathrm{d}\langle v_{in}^2 \rangle}{\mathrm{d}f} = \frac{8kT}{3g_m} + K_f \frac{1}{C_{ox}^2 W L}\frac{1}{f}$$

Thermal Noise

Flicker Noise

- *k = Boltzmann constant*
- *T = Temperature*
- *g_m = Transistor's transconductance*
- *C_{ox} = Gate capacitance / unit area*
- *WL = Transistor's channel width and length*
- *K_f = Flicker noise constant (process dependent)*

Analog Front-End Circuitry and Analysis

- To gain insights about the overall ENC of the system, for simplicity reasons, only the **input transistor noise contribution** was considered (most dominant noise source).

- The output noise of the CSA, induced from sensor diode (shot noise), can be calculated assuming an **integration of the noise current** through the feedback capacitance:

$$\frac{d\langle v^2_{CSA}\rangle_{shot}}{d\omega} = \frac{eI_0}{\pi\omega^2 C_F^2}$$

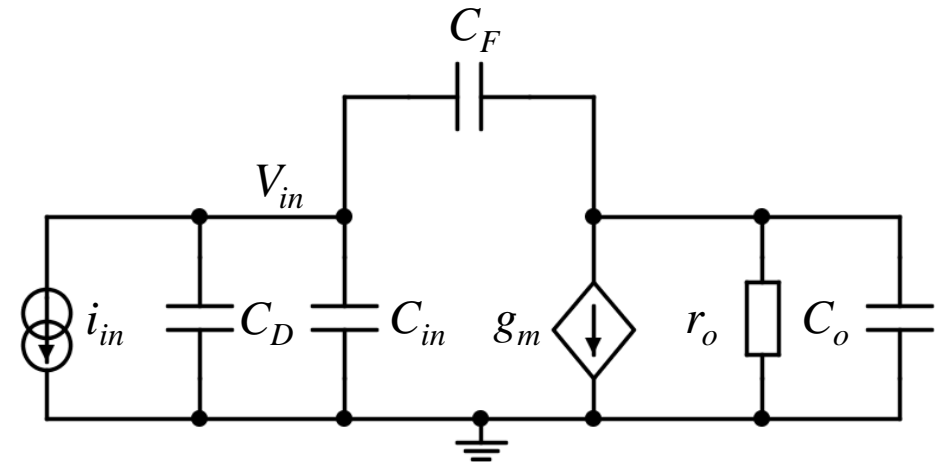# Analog Front-End Circuitry and Analysis

- By applying the feedback theory, the **feedback ratio** of the loop is equal to:

$$\beta = C_F / (C_F + C_D + C_{in})$$

- Considering that $C_D \gg C_F + C_{in}$ the feedback ratio can be expressed as:

$$\beta \approx C_F / C_D$$

CSA's Small-Signal Equivalent Circuit without continuous reset

Analog Front-End Circuitry and Analysis

- The **noise transfer function** of the CSA without a continuous reset can be calculated as follows:

$$-\beta^2 g_m^2 r_o^2 \langle v_{CSA}^2 \rangle_{th,fl} = \langle v_{CSA}^2 \rangle_{th,fl} - \langle v_{in}^2 \rangle_{th,fl} \Rightarrow \frac{\langle v_{CSA}^2 \rangle_{th,fl}}{\langle v_{in}^2 \rangle_{th,fl}} = \frac{1}{\beta^2}\frac{1}{g_m^2 r_o^2} = \frac{C_D^2}{C_F^2}\frac{1}{g_m^2 r_o^2}$$

- The CSA's output noise due to **the input transistor** can be calculated by substituting the following:

$$\langle v_{in}^2 \rangle_{th,fl} = \langle i_{in}^2 \rangle r_o^2$$

$$\frac{\langle v_{CSA}^2 \rangle_{th,fl}}{\langle v_{in}^2 \rangle_{th,fl}} = \frac{C_D^2}{C_F^2}\frac{1}{g_m^2 r_o^2} \quad\Longrightarrow\quad \langle v_{CSA}^2 \rangle_{th,fl} = \frac{C_D^2}{C_F^2}\frac{1}{g_m^2 r_o^2}\langle i_{in}^2 \rangle r_o^2 = \boxed{\frac{C_D^2}{C_F^2}\frac{\langle i_{in}^2 \rangle}{g_m^2}}$$

Analog Front-End Circuitry and Analysis

$$\frac{\mathrm{d}\langle v_{in}^2 \rangle}{\mathrm{d}f} = \frac{8kT}{3g_m} + K_f \frac{1}{C_{ox}^2 W L} \frac{1}{f}$$

(1)

$$\frac{\mathrm{d}\langle v_{CSA}^2 \rangle_{shot}}{\mathrm{d}\omega} = \frac{e I_0}{\pi \omega^2 C_F^2}$$

(2)

$$\langle v_{CSA}^2 \rangle_{th,fl} = \frac{C_D^2}{C_F^2} \frac{\langle i_{in}^2 \rangle}{g_m^2}$$

(3)

$$\frac{\mathrm{d}\langle v_{CSA}^2 \rangle}{\mathrm{d}\omega} = \frac{e I_0}{\pi \omega^2} \cdot \left(\frac{1}{C_F} \right)^2 + \frac{K_f}{\omega C_{ox}^2 W L} \cdot \left(\frac{C_D}{C_F} \right)^2 + \frac{4kT}{3\pi g_m} \cdot \left(\frac{C_D}{C_F} \right)^2$$

Analog Front-End Circuitry and Analysis

- The ENC calculation can be derived by integrating the CSA's noise spectral density over its **available bandwidth**, dictated by its **peaking time performance** (rise time – τ_R):

$$ENC^2 \approx eI_0 \cdot \tau_r + \frac{K_f \cdot C_D^2}{C_{ox}^2 W L} + \frac{4kT \cdot C_D^2}{3g_m \cdot \tau_r}$$

Shot Noise   *Flicker Noise*   *Thermal Noise*

Analog Front-End Circuitry and Analysis

$$ENC^2 \approx eI_0 \cdot \tau_r + \frac{K_f \cdot C_D^2}{C_{ox}^2 W L} + \frac{4kT \cdot C_D^2}{3g_m \cdot \tau_r}$$

- Charge amplification is proportional to feedback capacitance C_F .
- ENC includes the charge gain component factor.
- ENC still depends, to some extent, on C_F ($\tau_R - C_F$ dependency).
- Low rise time moves CSA's low-pass pole (s_{p1}) to higher frequencies.
- Both ENC and timing response of CSA depend on detector capacitance C_D.
- Mitigation of high C_D through input transistor's transconductance g_m (scales up with power consumption).

Analog Front-End Circuitry and Analysis

Technology node →	180 nm	130 nm SiGe BiCMOS		65 nm	22 nm FD-SOI
CSA metric ↓	CMOS[a]	HBT[b]	CMOS[a]	CMOS[a]	CMOS[a]
Peaking Time $\tau_r = \frac{(C_D + C_{in} + C_o)}{g_m}$ $+ \frac{(C_D + C_{in})C_o}{g_m C_F}$	$g_m \approx 5$ mS $C_{in}^{c} \approx 19.4$ fF $\tau_r \geq 203.9$ ps	$g_m \approx 101$ mS $C_{in}^{c} \approx 4.1$ fF $\tau_r \geq 9.94$ ps	$g_m \approx 9.5$ mS $C_{in}^{c} \approx 12.1$ fF $\tau_r \geq 106.5$ ps	$g_m \approx 13.3$ mS $C_{in}^{c} \approx 4.9$ fF $\tau_r \geq 75.55$ ps	$g_m \approx 21.5$ mS $C_{in}^{c} \approx 4.8$ fF $\tau_r \geq 46.73$ ps
Charge Gain $A_Q = -\frac{\tau_f \left(\frac{\tau_f + \tau_r}{\tau_r} \right)^{-\frac{\tau_r}{\tau_f}}}{C_F (\tau_f + \tau_r)}$	$\tau_f = 1$ ns $\|A_Q\| = \frac{0.5572}{C_F}$	$\tau_f = 1$ ns $\|A_Q\| = \frac{0.9447}{C_F}$	$\tau_f = 1$ ns $\|A_Q\| = \frac{0.6933}{C_F}$	$\tau_f = 1$ ns $\|A_Q\| = \frac{0.7568}{C_F}$	$\tau_f = 1$ ns $\|A_Q\| = \frac{0.8232}{C_F}$
Equivalent Noise Charge $ENC^2 = eI_0 \cdot \tau_r + \frac{K_f \cdot C_D^2}{C_{ox}^2 WL}$ $+ \frac{4kT \cdot C_D^2}{3 g_m \cdot \tau_r}$	*Reference*	*Shot* ↓ 95.5% *Thermal* ↑ 9.8%	*Shot* ↓ 49.7% *Thermal* ↑ 4.6%	*Shot* ↓ 65.6% *Thermal* ↑ 9.3%	*Shot* ↓ 78.7% *Thermal* ↑ 9.4%
Figure of Merit[d] $FoM_1 = \frac{C_{in}^{(fF)} \cdot \tau_{r_{min}}^{(ps)}}{g_m^{(mS)} \cdot \|A_Q\| \cdot C_F}$	1.419×10^3	4.271×10^{-1}	1.956×10^2	3.678×10^1	1.267×10^1

[a] g_m extracted @ $V_{gs} = V_{ds} = V_{DD}$ for $W_{in} = 10$ μm, $L_{in} = L_{min}$.

[b] g_m extracted @ $V_{be} = V_{ce} = V_{DD}$ for *Emitter Area* $= 0.07 \times 0.9$ μm^2.

[c] C_{in} calculated using S-parameter analysis as $C_{in} = \frac{1}{2\pi} \left(\frac{\partial}{\partial f} Im(Y_{11}) \right)$.

[d] The lower the better.

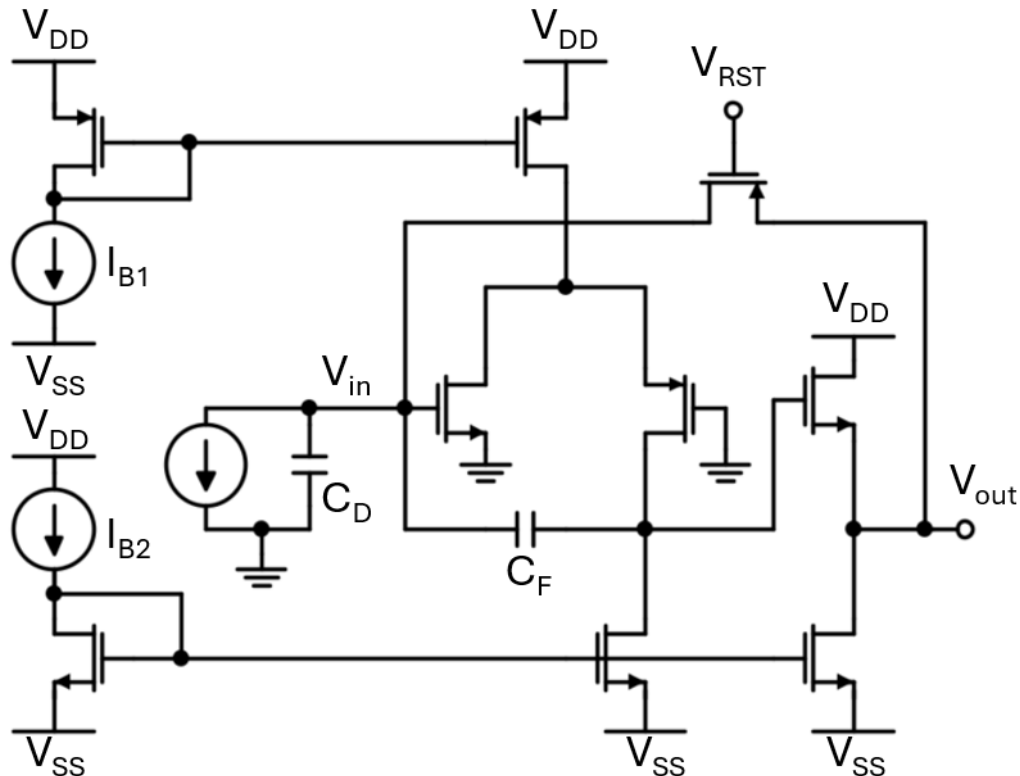*CSA performance overview versus Technology Scaling (taken from: [9])*

Analog Front-End Circuitry and Analysis

- To evaluate the real CSA performance across all selected process nodes, four topologies were designed.

- In all topologies, the detector capacitance and the feedback components were set constant :
  C_D = 1 pF, C_F = 10 fF and R_F = 200 kΩ.

- For a fair comparison, a power dissipation limit was set for all topologies, keeping the overall current of each topology to be **< 1.5 mA @ V_{DD}.**
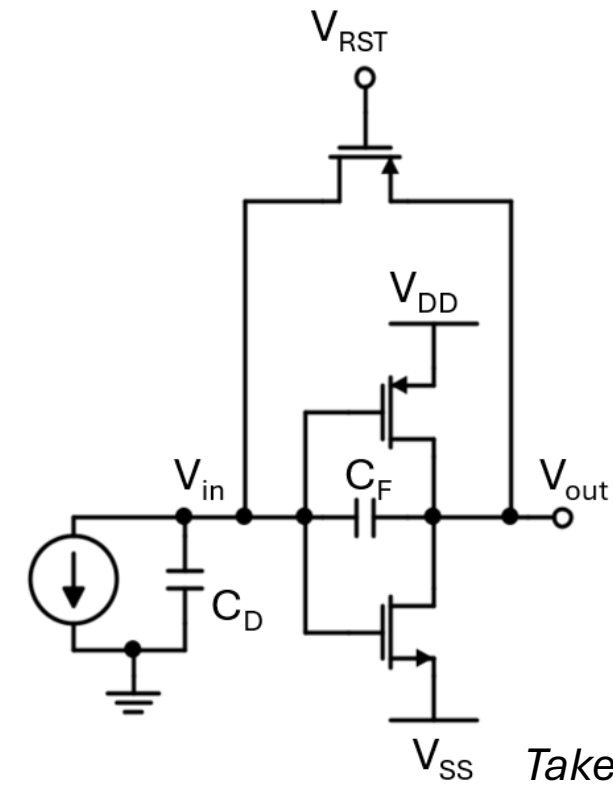
CMOS Node

Folded-Cascode CSA

Inverter-based CSA

BiCMOS Node

Common-Source CSA
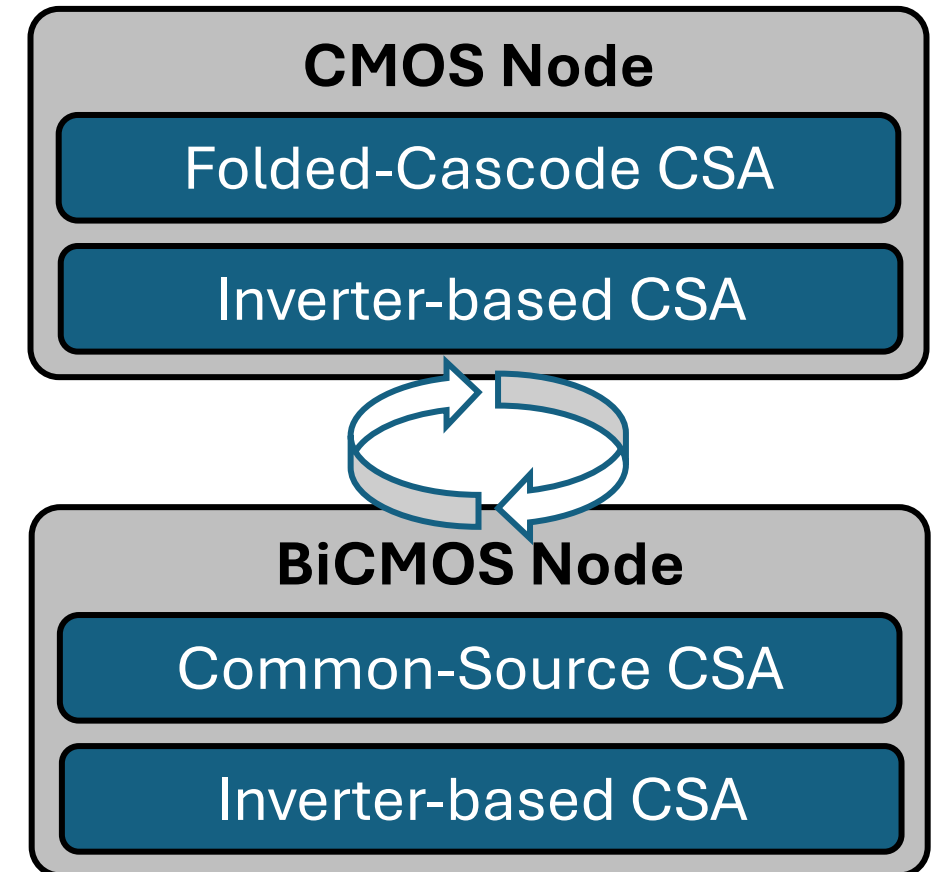
Inverter-based CSA

Analog Front-End Circuitry and Analysis

Folded-Cascode CSA
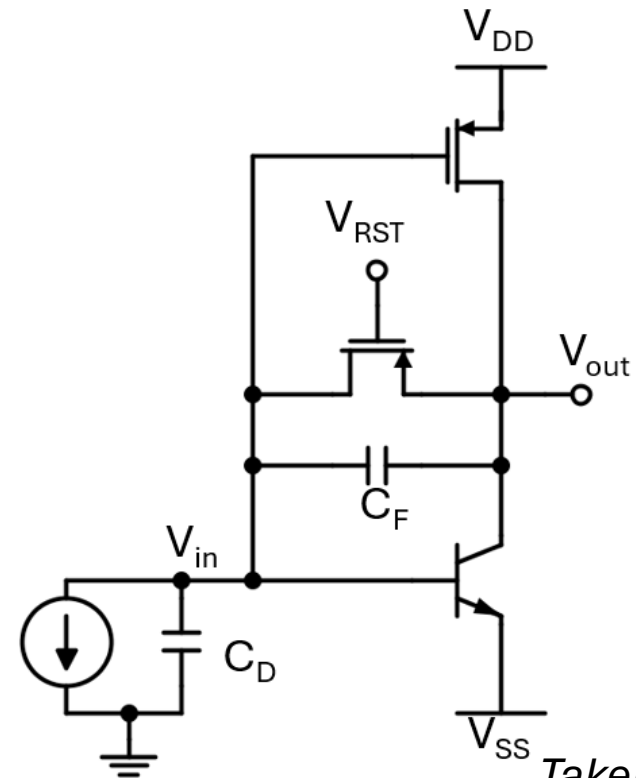

CMOS Inverter-based CSA

Taken From: [9]

Analog Front-End Circuitry and Analysis
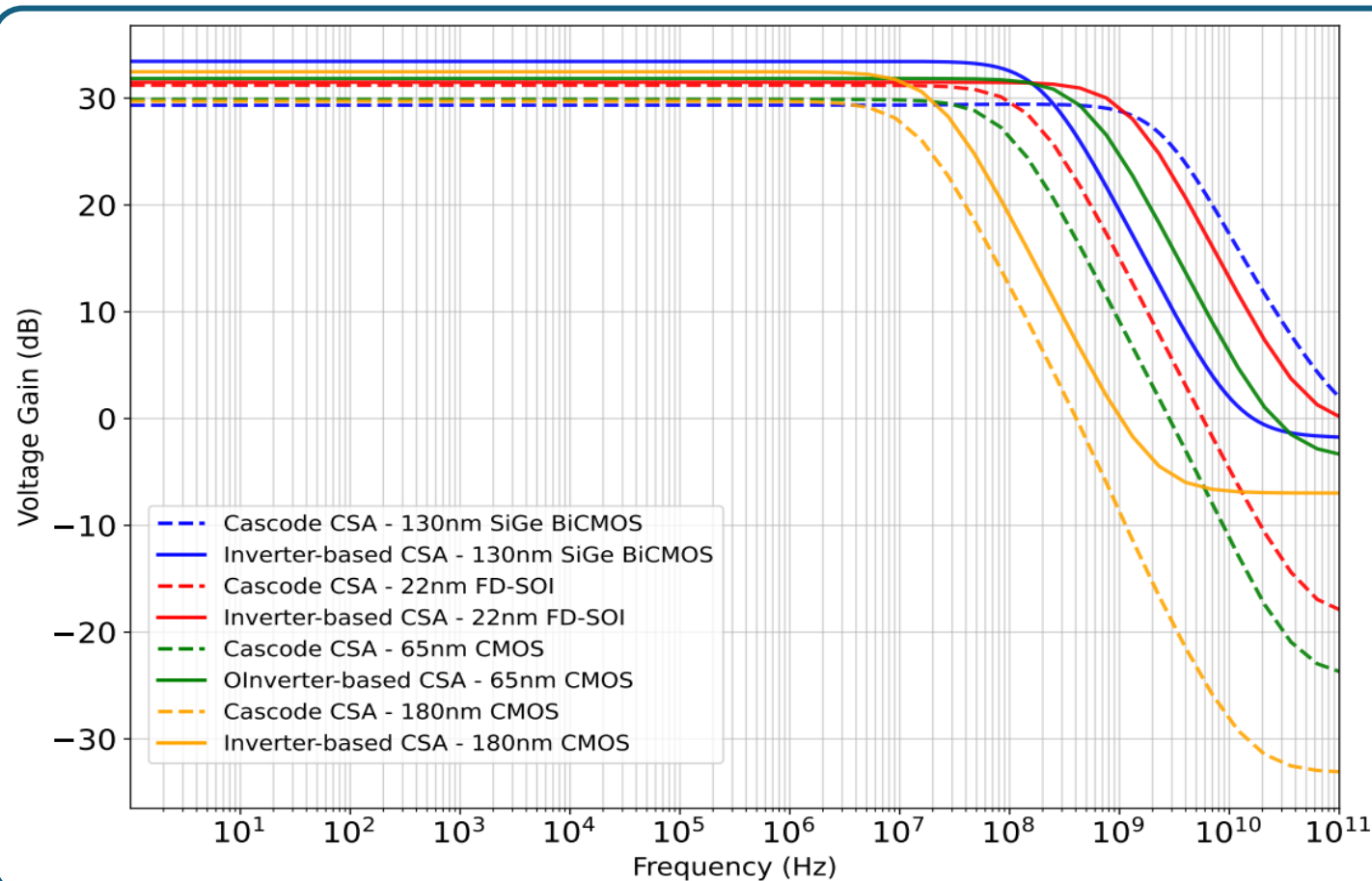

HBT-based Common-Source CSA
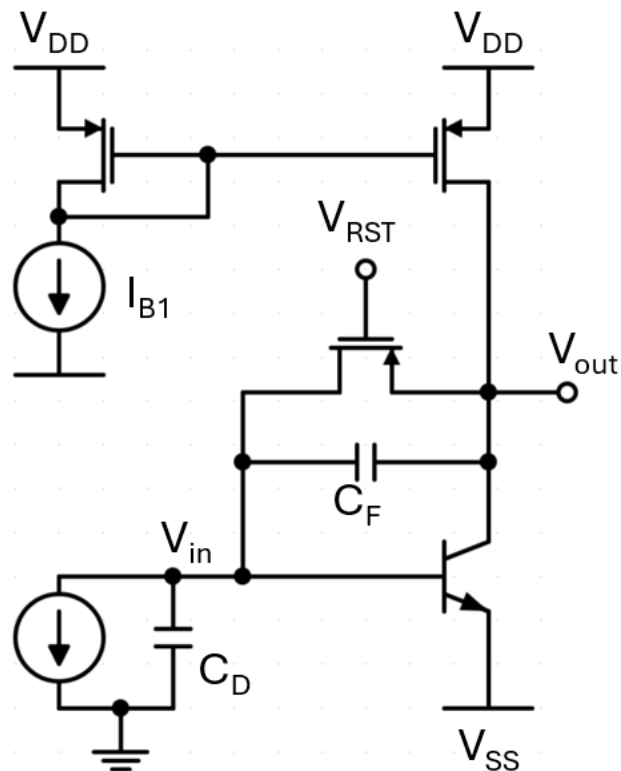
BiCMOS Inverter-based CSA

Taken From: [9]

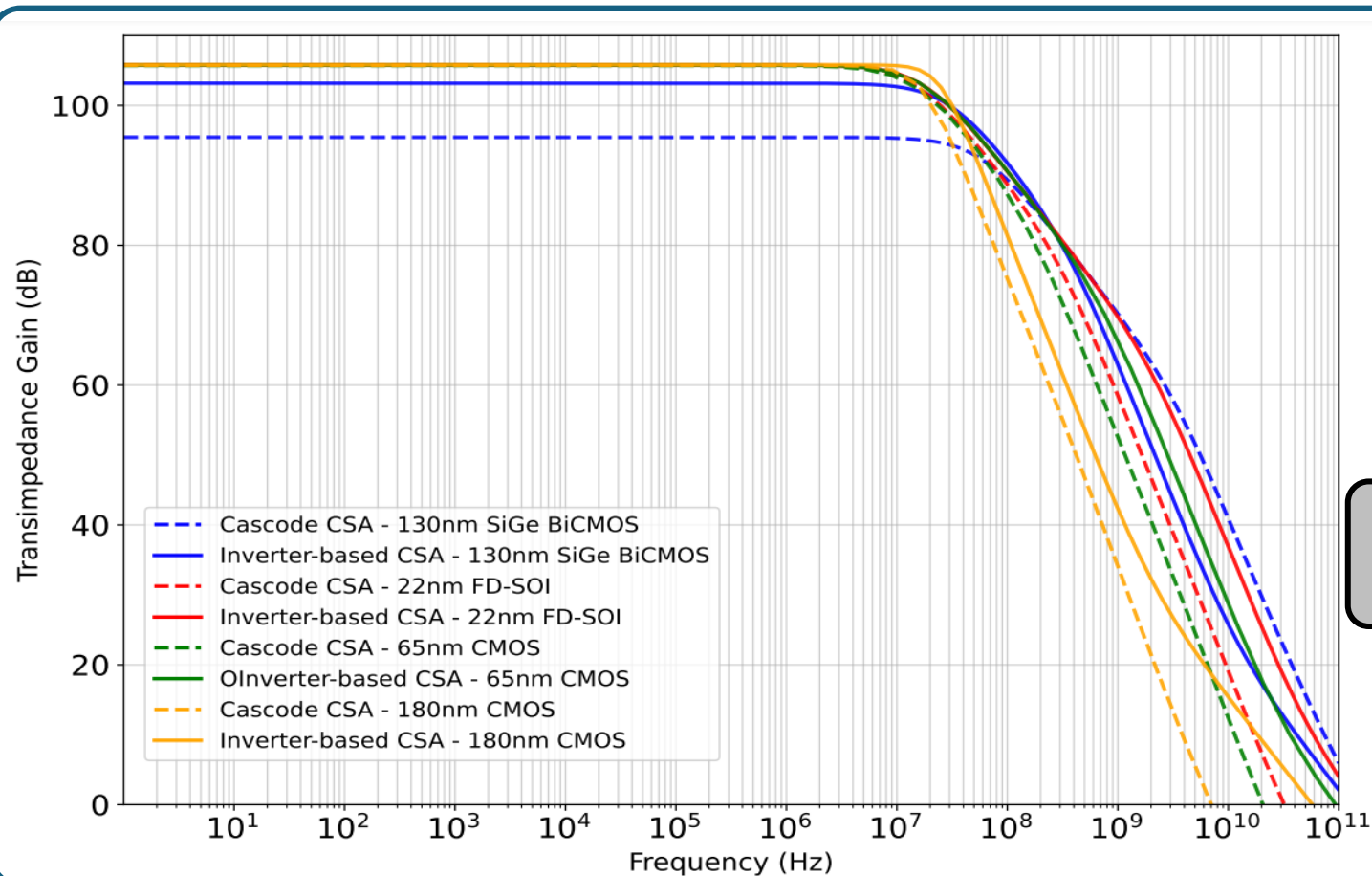# Analog Front-End Circuitry and Analysis

CSA Voltage Gain
(Frequency Response)
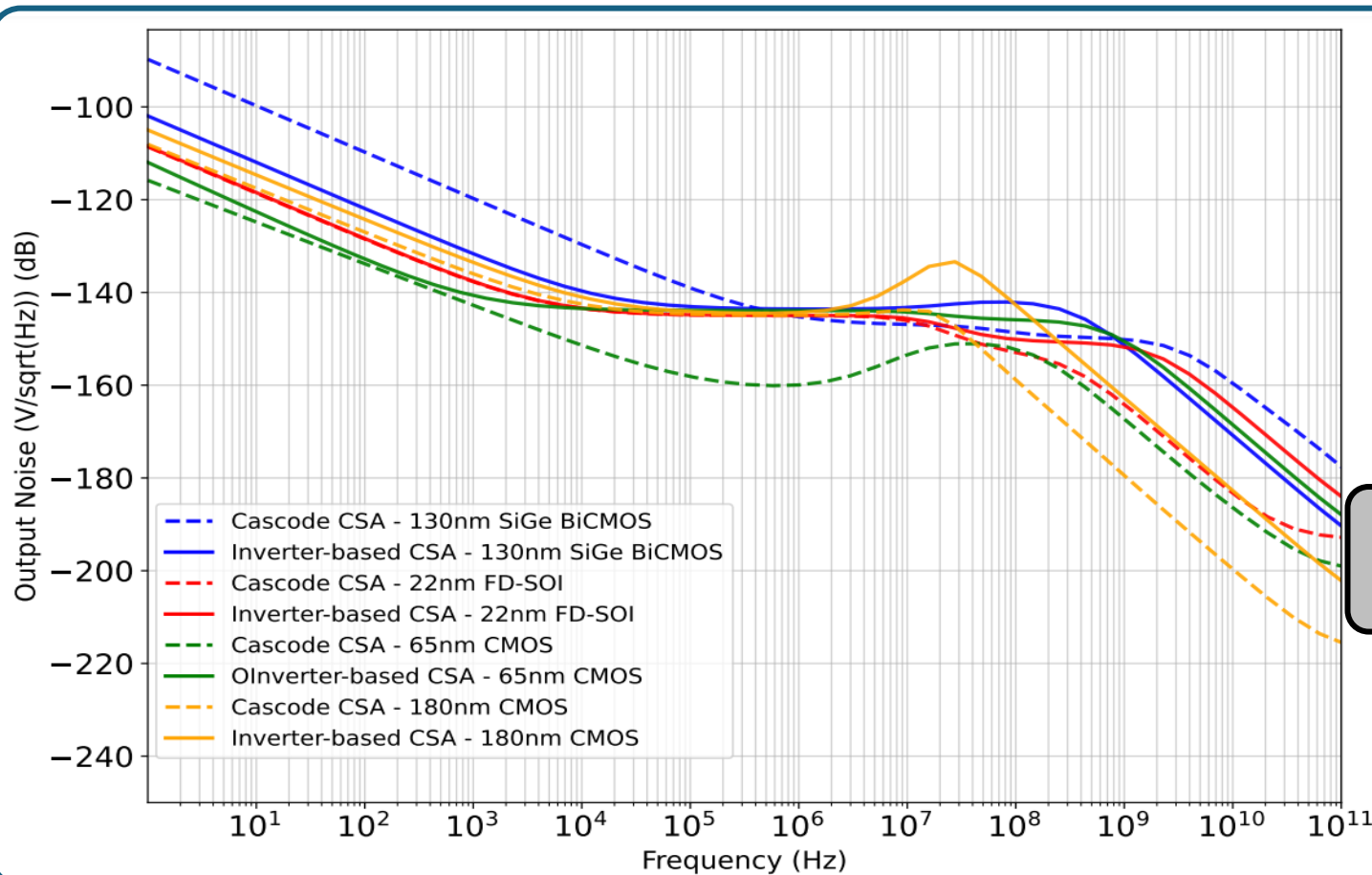
Small-signal Analysis

Taken From: [9]

Analog Front-End Circuitry and Analysis

CSA Transimpedance Gain (Frequency Response)

Small-signal Analysis

Taken From: [9]

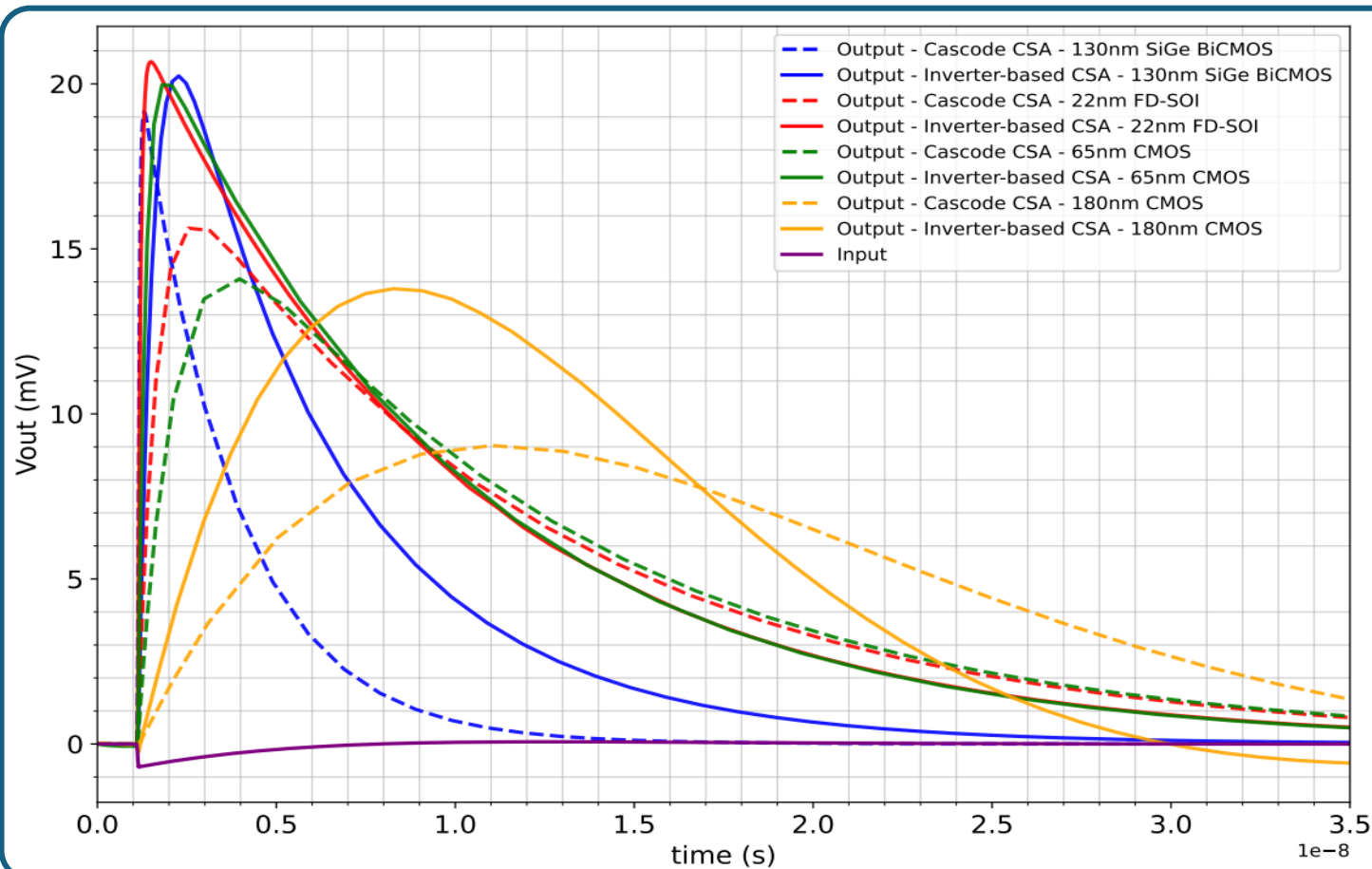# Analog Front-End Circuitry and Analysis

Taken From: [9]

CSA Noise Behavior
(AC Noise Analysis)

Small-signal Analysis

Analog Front-End Circuitry and Analysis
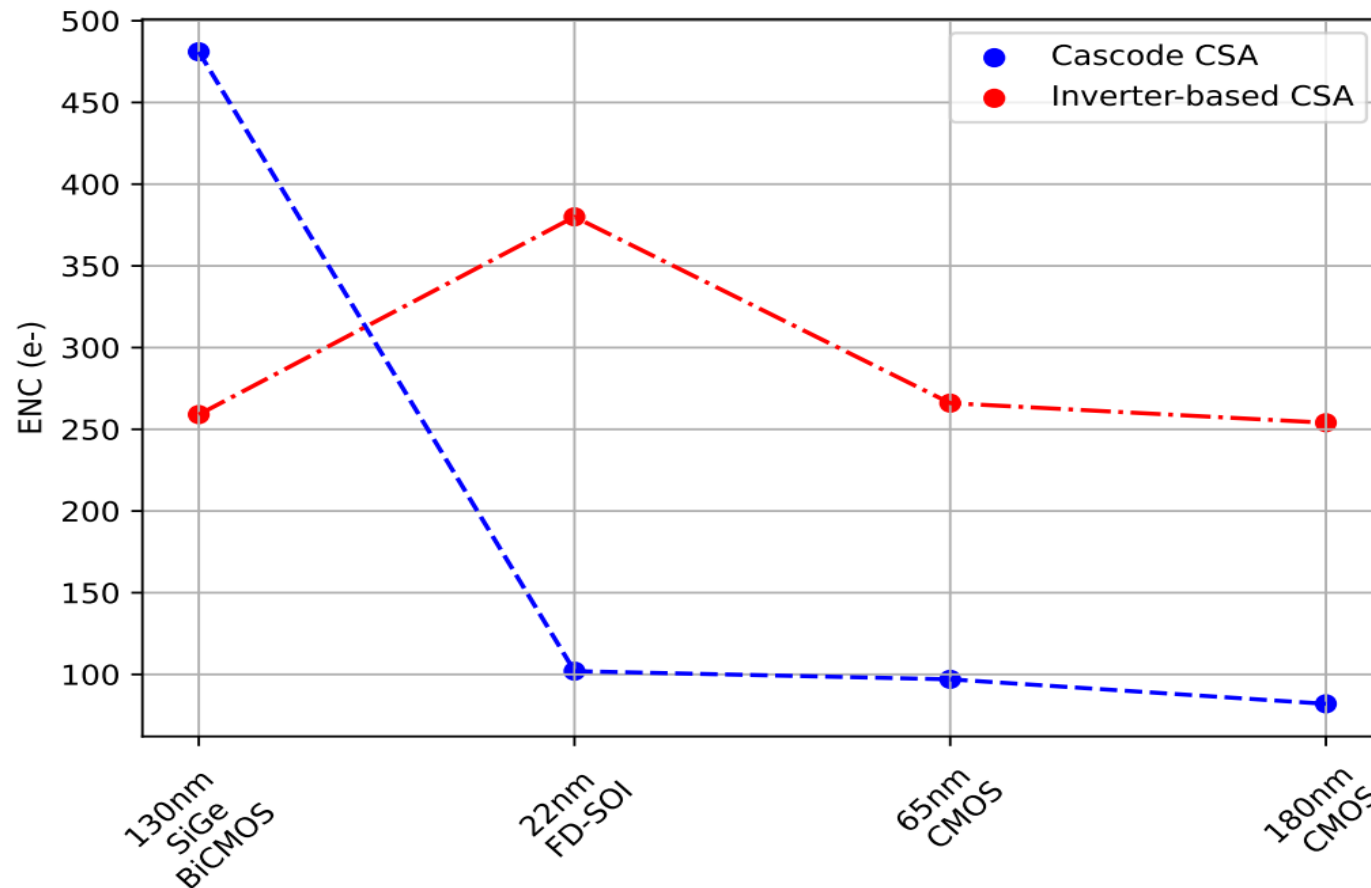

CSA Transient Response
(input charge Q_{in} = 1 fC)

Large-signal Analysis

Taken From: [9]

Analog Front-End Circuitry and Analysis

CSA ENC performance
(derived from AC noise)

Taken From: [9]

Analog Front-End Circuitry and Analysis

Technology node →	180 nm CMOS		130 nm SiGe BiCMOS		65 nm CMOS		22 nm FD-SOI CMOS	
Performance metric ↓	FC[a]	INV[b]	CS[c]	INV[b]	FC[a]	INV[b]	FC[a]	INV[b]
Peaking time – τ_r (ns)	11	8.3	0.2	1.14	4	1.8	2.5	1.5
Fall time – τ_f (ns)	16.9	10.8	1.8	5.2	11.6	5.5	11.5	9
Voltage gain – A_V (dB)	29.7	32.5	30	33.5	29.9	31.8	31.2	31.5
Transimpedance gain – A_{XF} (dBΩ)	105.7	106	92.7	103.2	105.7	105.7	105.8	105.9
Bandwidth – BW (GHz)	0.014	0.022	2.3	0.205	0.092	0.55	0.16	1.2
RMS noise – $V_{noise(rms)}$ (mV)	0.39	1.32	2.5	1.95	0.46	1.35	0.51	1.91
Equivalent Noise Charge – ENC (e^-)	82	255	481	259	97	266	102	380
Power dissipation – P_{diss} (mW)	2.34	0.324	1.29	0.035	1.44	0.24	0.96	0.141
$FoM_2{}^{d} = \dfrac{A_V^{(dB)} \cdot BW^{(GHz)}}{\tau_r^{(ns)} \cdot ENC^{(e^-)} \cdot P_{diss}^{(mW)}}$	0.0002	0.001	0.556	0.664	0.0049	0.1522	0.0204	0.4703

[a] Folded-Cascode Configuration.
[b] Inverter-based Configuration.
[c] Common-Source Configuration.
[d] The higher the better.

Simulation Results of all implemented CSAs versus Technology Scaling (taken from: [9])
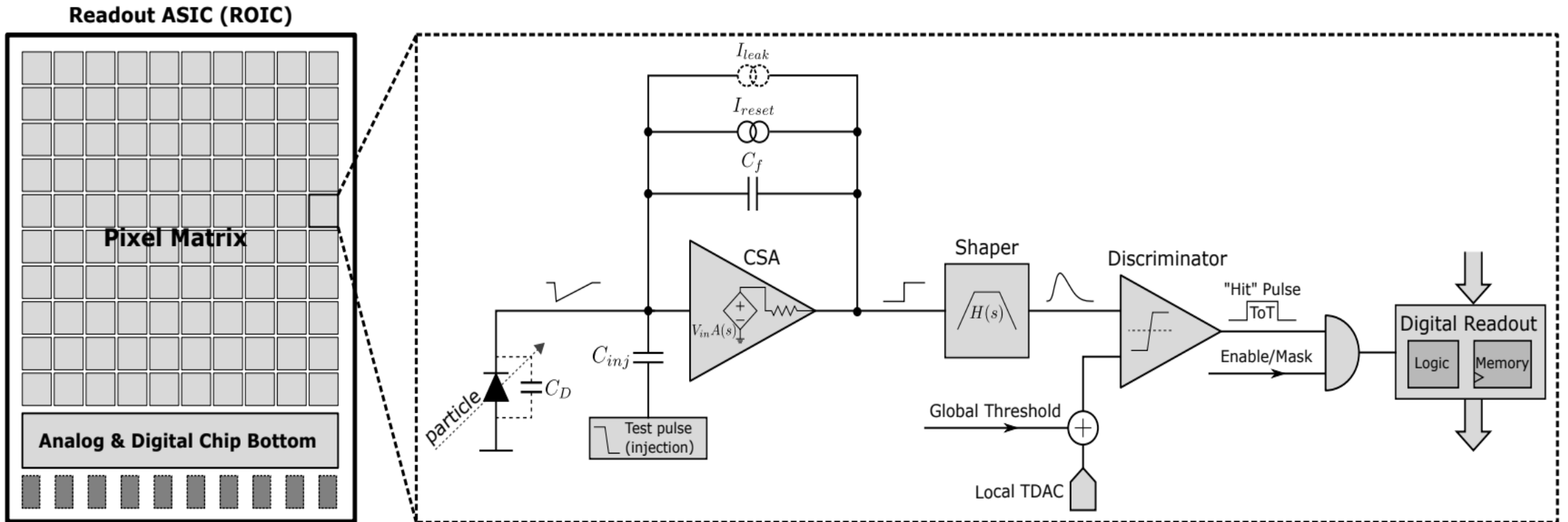
1. Introduction to Readout Electronics

2. Planar and 3D Pixel Detectors

3. Analog Front-End Circuitry and Analysis
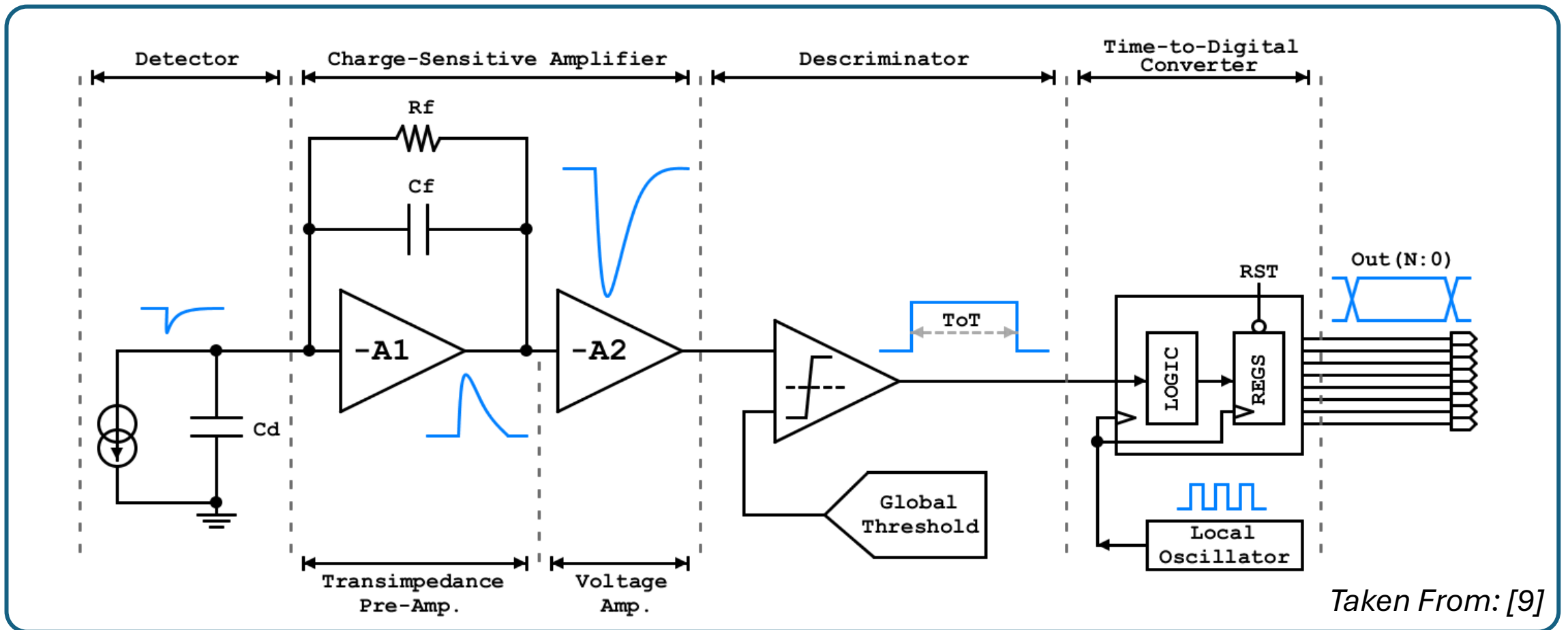
4. Readout Front-End ASIC Design

5. Conclusion and Discussion

Readout Front-End ASIC Design

Typical front-end readout scheme often used in a detector readout ASIC.
(taken from: [11])

Readout Front-End ASIC Design

Taken From: [9]

Readout Front-End ASIC Design

Particle Interaction with the Sensor:
- Particle induces a short current signal.

Active Integration:
- Preamplifier with feedback loop.
- Generates a voltage proportional to charge.

Pulse Shaping:
- Band-pass filter with a tuned time constant.
- Optimizes signal shape and bandwidth.
- Reduces noise and pile-up effects.

Discrimination:
- Compares pre-amplifier output signal to a reference voltage (threshold).


Taken From: [9]
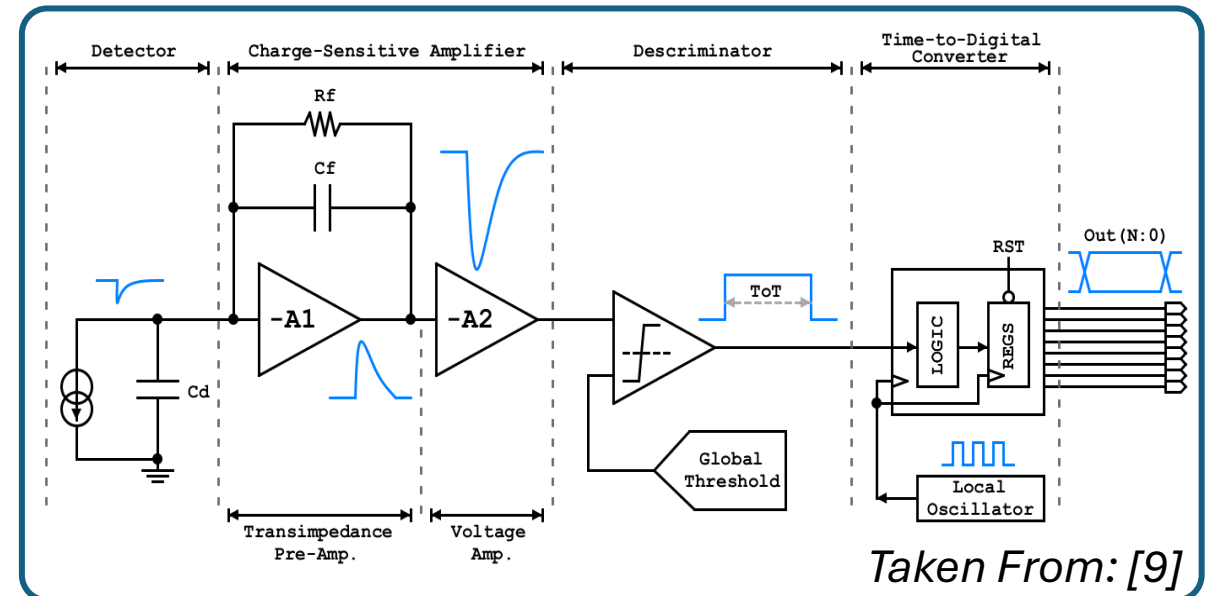
Digital Pulse Readout:
- Pulse width is proportional to the collected charge (Time-over-Threshold (ToT)), converted into a digital bit-stream (TDC).

Readout Front-End ASIC Design

Operating Threshold and Threshold Variations:

- Detection threshold should be set **as low as possible**, maximizing detector's efficiency **but not too low** as to suppress hits from noise fluctuations.

- Threshold of individual pixels experience random variations due to **component mismatches** and possible **systematic variations** due to voltage drops across the power delivery network of the array.
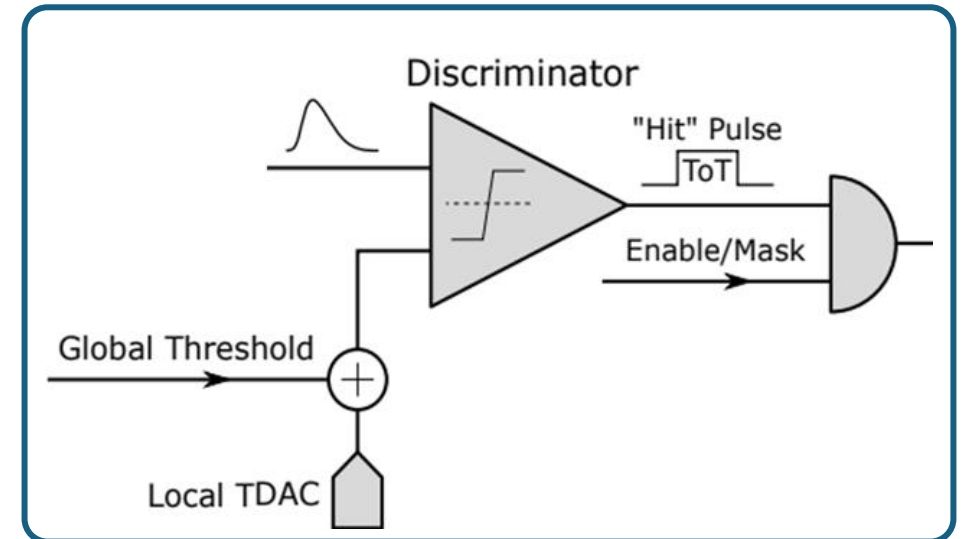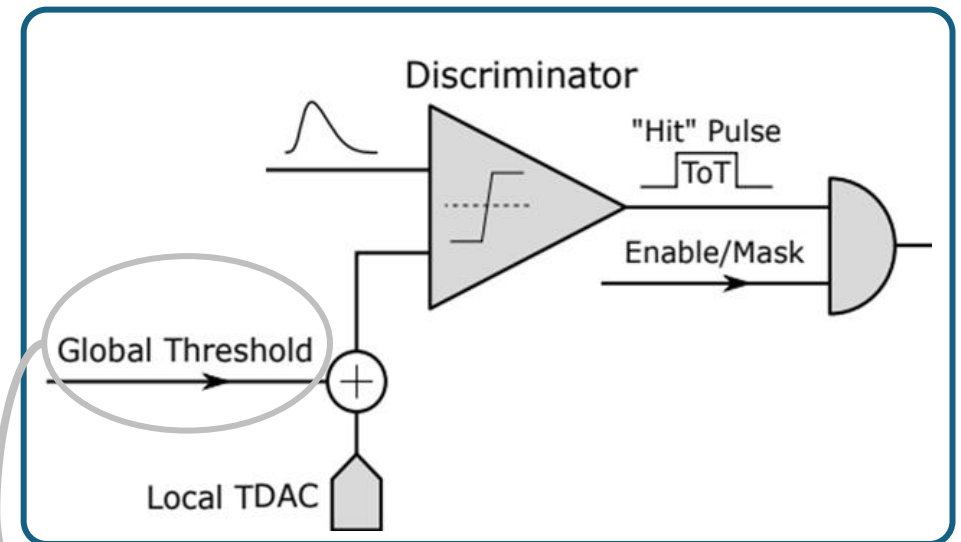
Readout Front-End ASIC Design

Operating Threshold and Threshold Variations:

- Threshold is tuned via a **Tuning Digital-to-Analog Converter (TDAC)** → Dispersion inversely proportional to TDAC bits.

$$\sigma_{THR_{\text{tuned}}} \approx \frac{\sigma_{THR}}{2^{n_{\text{TDAC}}}}$$

> *Threshold dispersion before tuning*

- FE noise sets the lower bound to threshold. The charge threshold should be at least **6 times greater** than the combined threshold deviation and the FE noise.


$$Q_{THR} = 6 \cdot \sqrt{\sigma_{THR}^2 + ENC^2}$$

Readout Front-End ASIC Design

## *Timing Response and In-Time Threshold:*

- Timing response is a **function of input charge**. Hits with high amplitude results to a faster response than the low-amplitude hits.

- Apart from charge collection time, the time response also depends on **the pre-amplifier peaking time**, the shaper bandwidth and the **discrimination speed**.
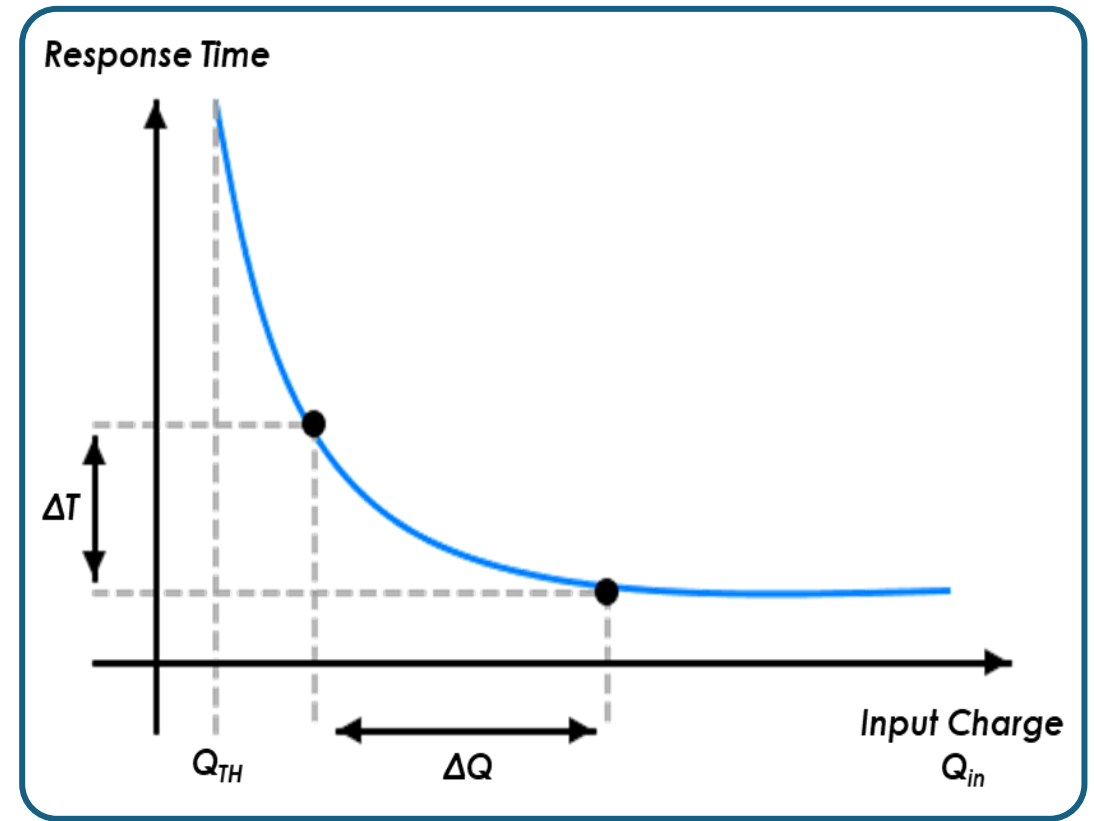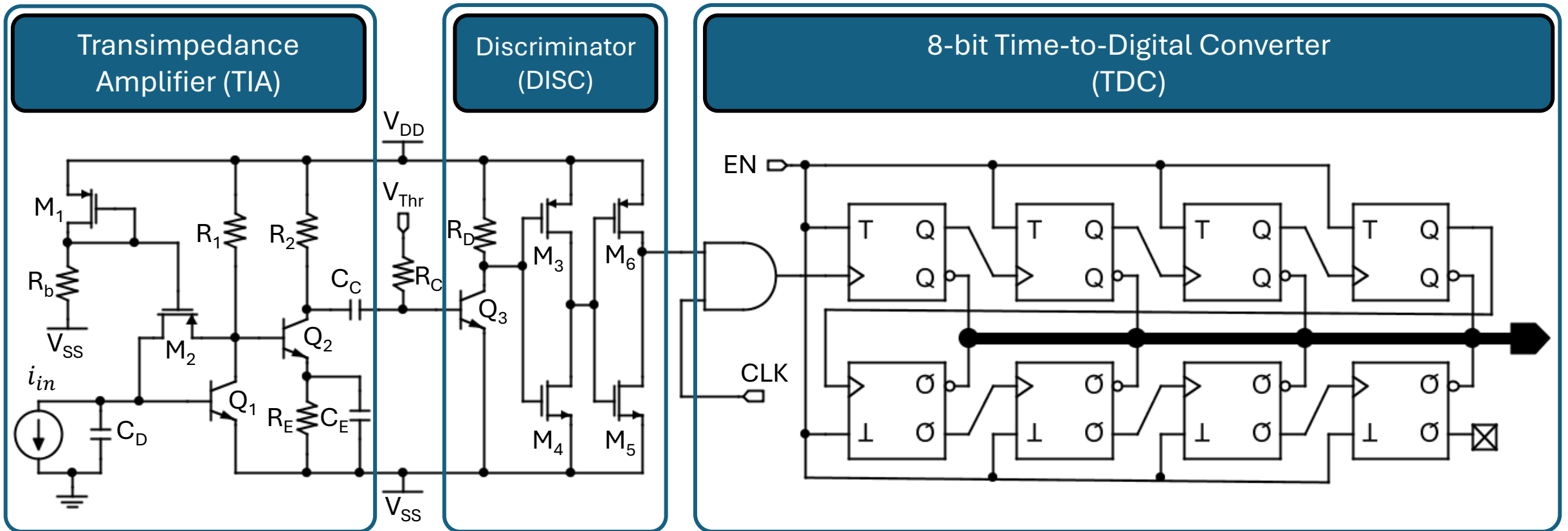
Readout Front-End ASIC Design

Input Charge Measurement:

- The duration of discriminator's output is proportional to the input charge into the chip's pixel. This duration is also referred as **Time-over-Threshold (ToT)**.

- The charge measurement is a **time-to-digital conversion (TDC)**. Measuring the clock cycles during which discriminator's output is higher than charge threshold, the ToT is obtained.

$Q_1 > Q_2$

Threshold

$ToT_1 > ToT_2$
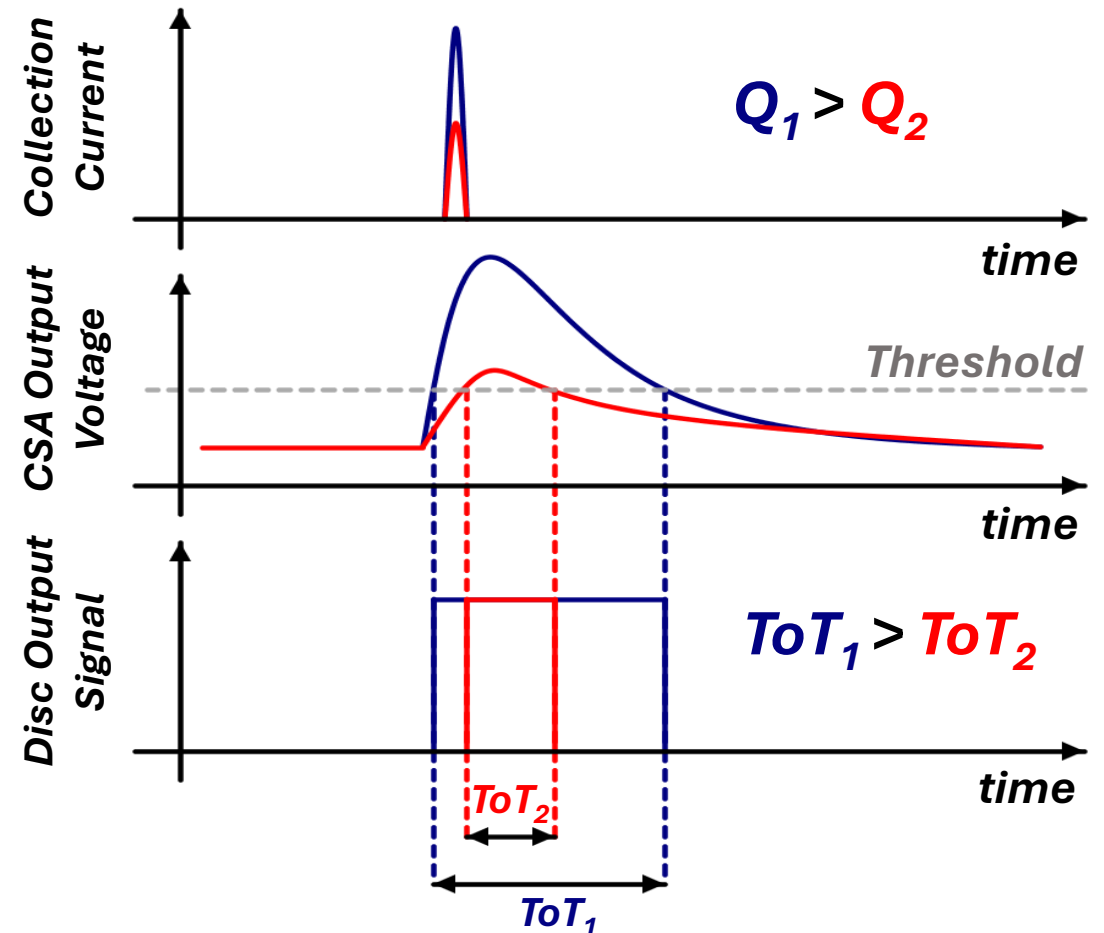
Readout Front-End ASIC Design

Top-level readout front-end ASIC schematic using the 130 nm BiCMOS process node (taken from: [9]).

Readout Front-End ASIC Design

Transimpedance Amplifier (TIA):

- The front-end readout consists of **two amplification stages** (TIA and voltage amplifier).

- TIA is equivalent to a CSA **if feedback parasitics** are considered.

- CSA analysis can also be applied in the TIA topology.
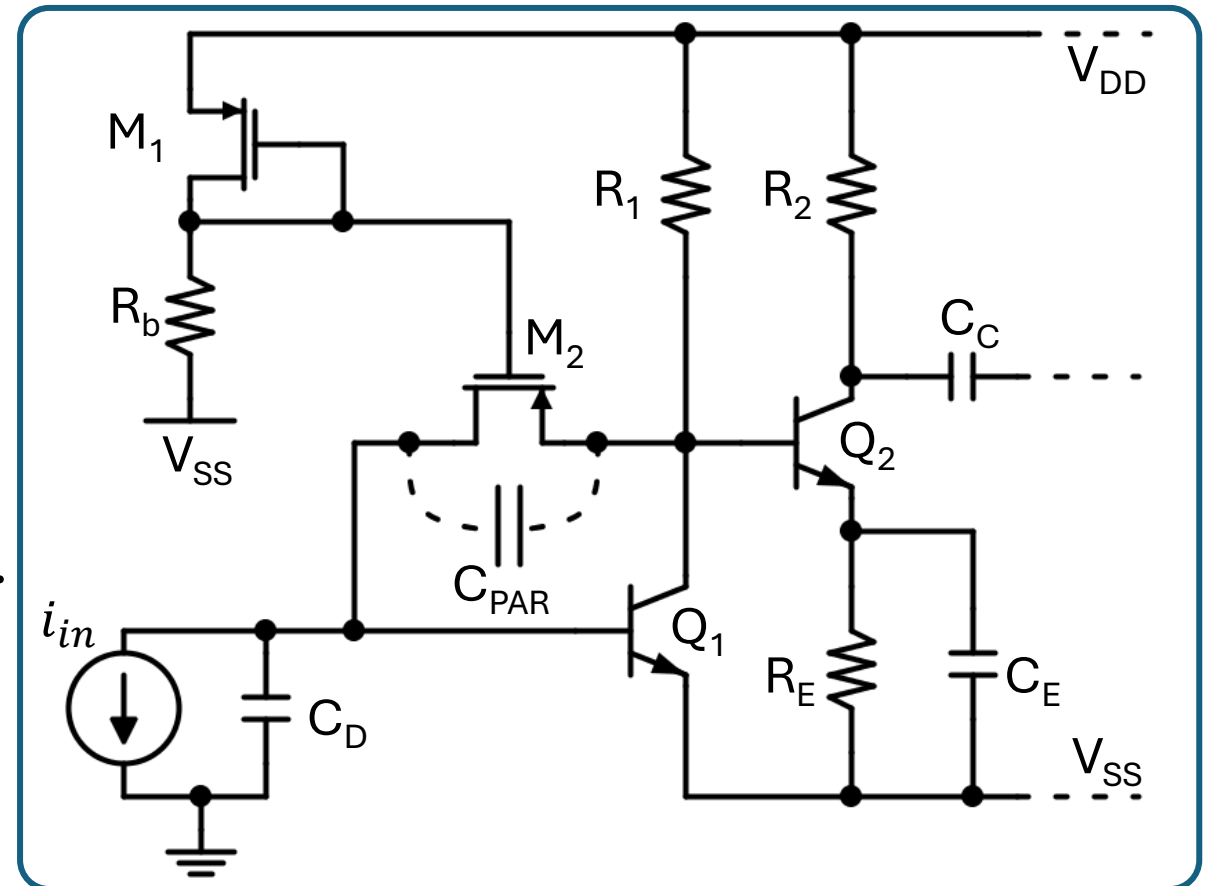
Readout Front-End ASIC Design
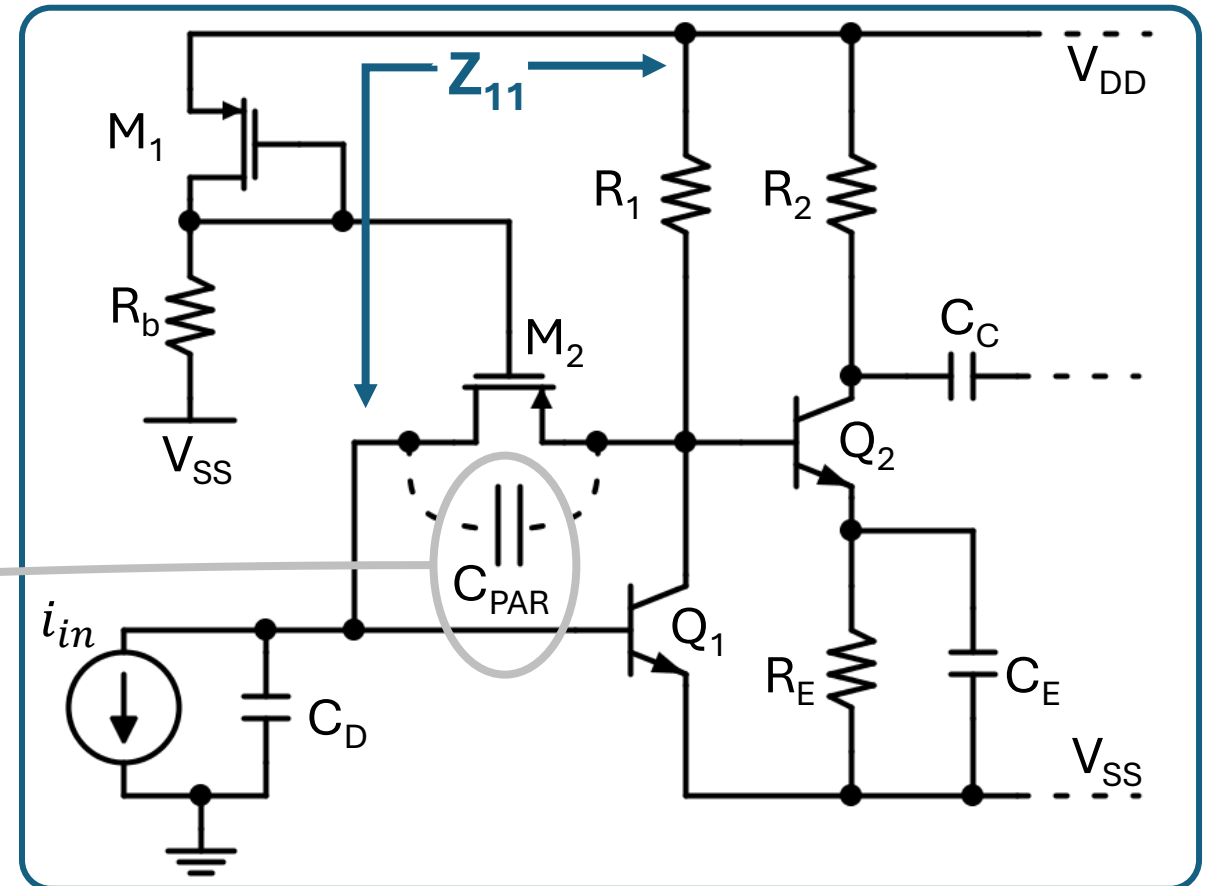
Feedback Parasitic Capacitance:

- S-parameter analysis and monitoring **Im(Y$_{11}$)** and having V$_{DD}$ as reference:

$$Z_{11} = R + Xc = R + 1/sC$$
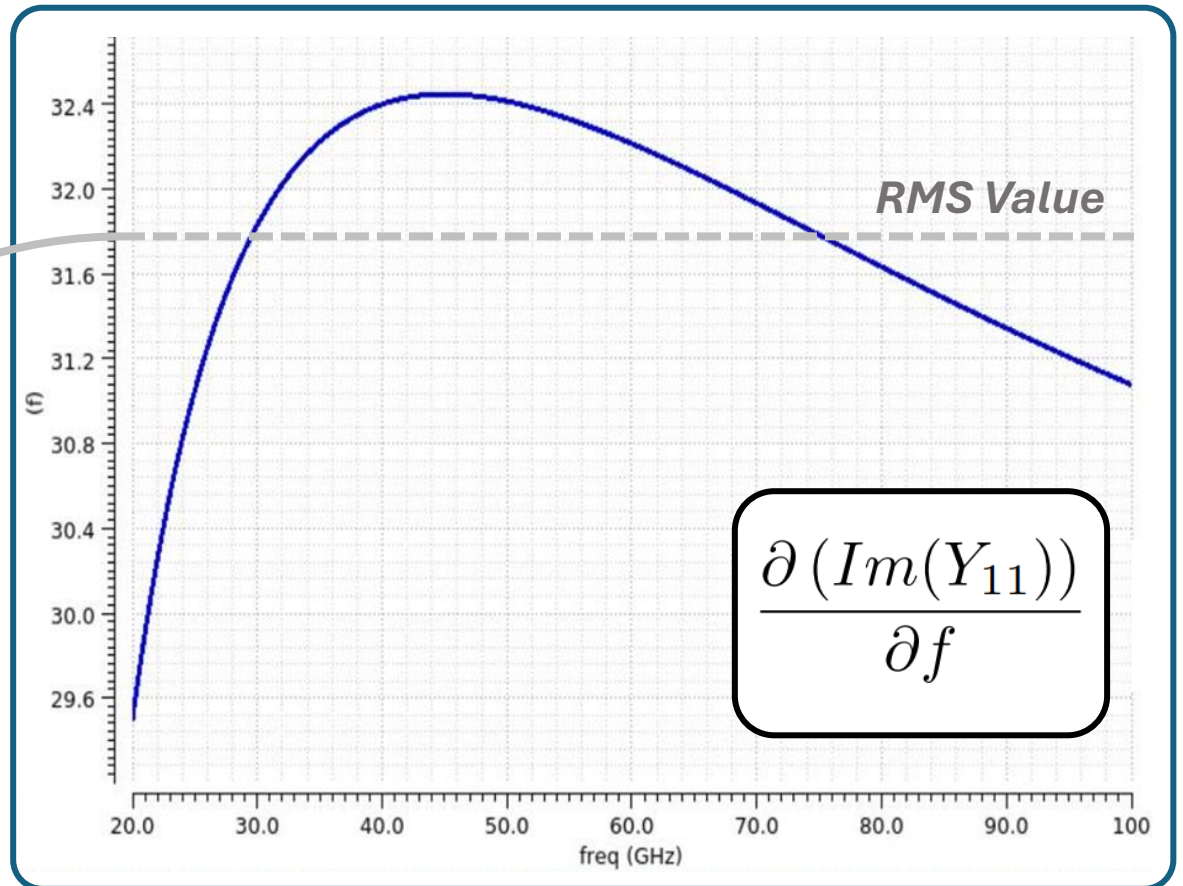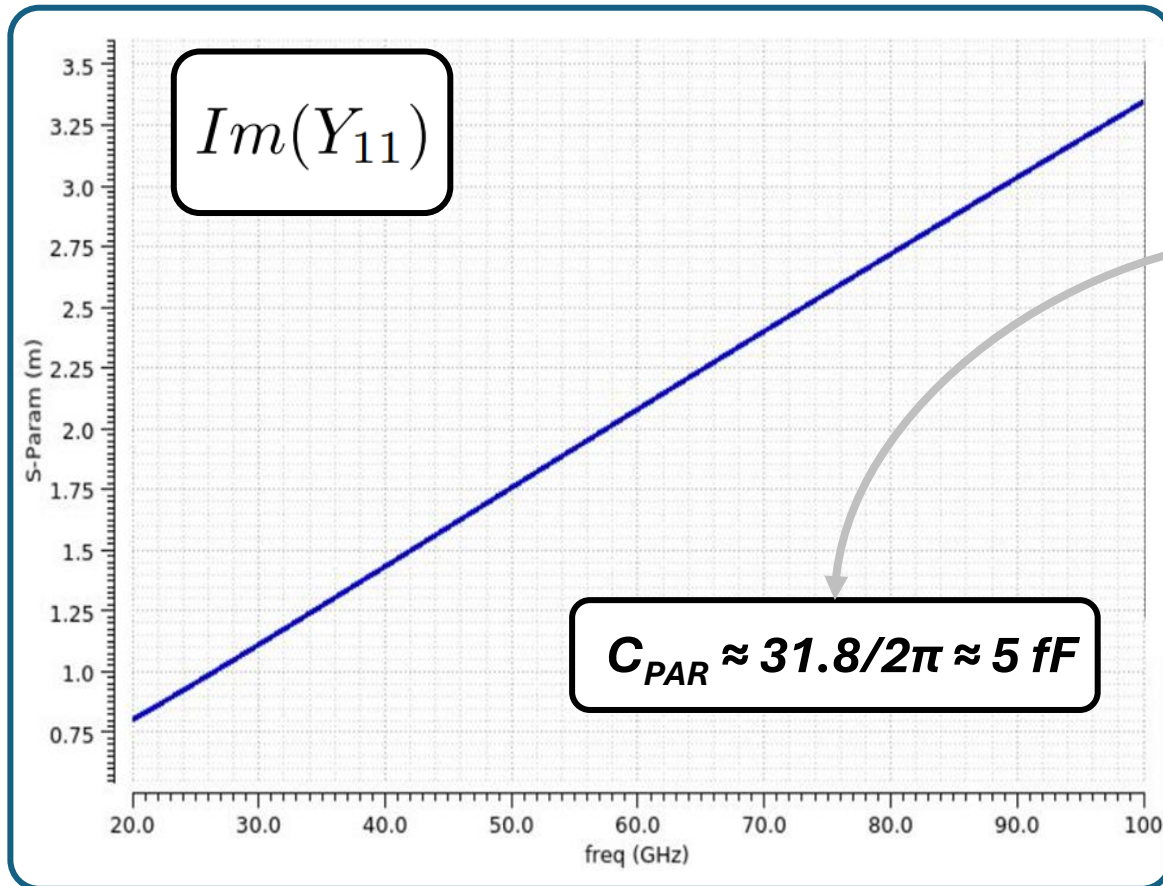
$$Y_{11} = 1/R + sC$$

$$Im(Y_{11}) = sC = 2\pi f C$$

$$C = \left(\frac{1}{2\pi}\right) \times \left(\frac{\partial (Im(Y_{11}))}{\partial f}\right)$$
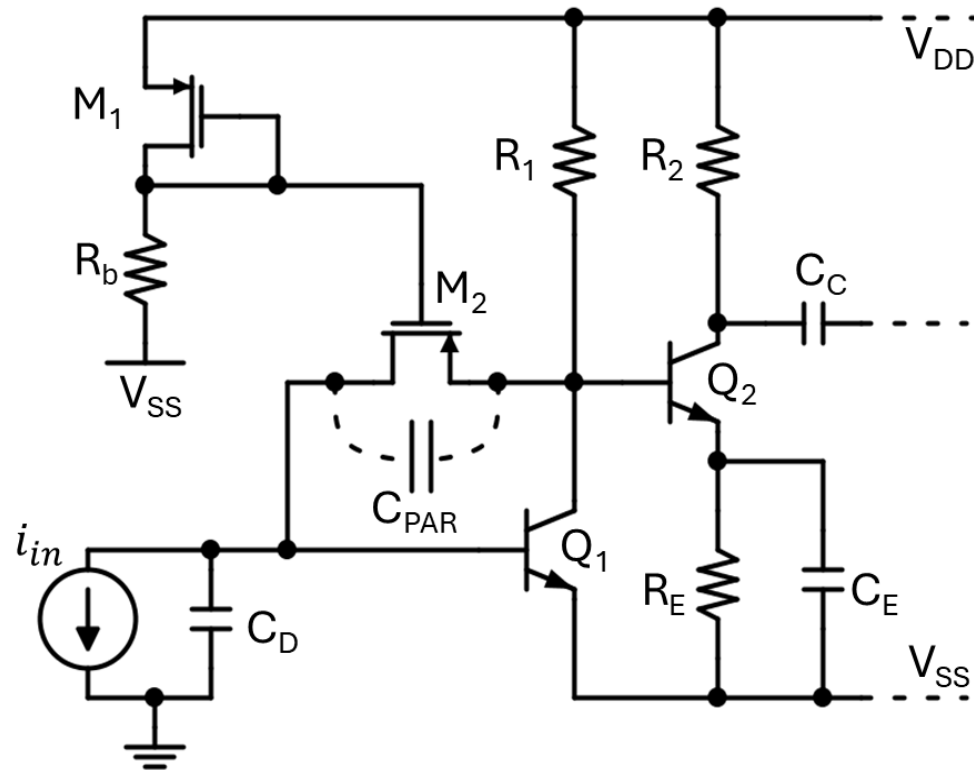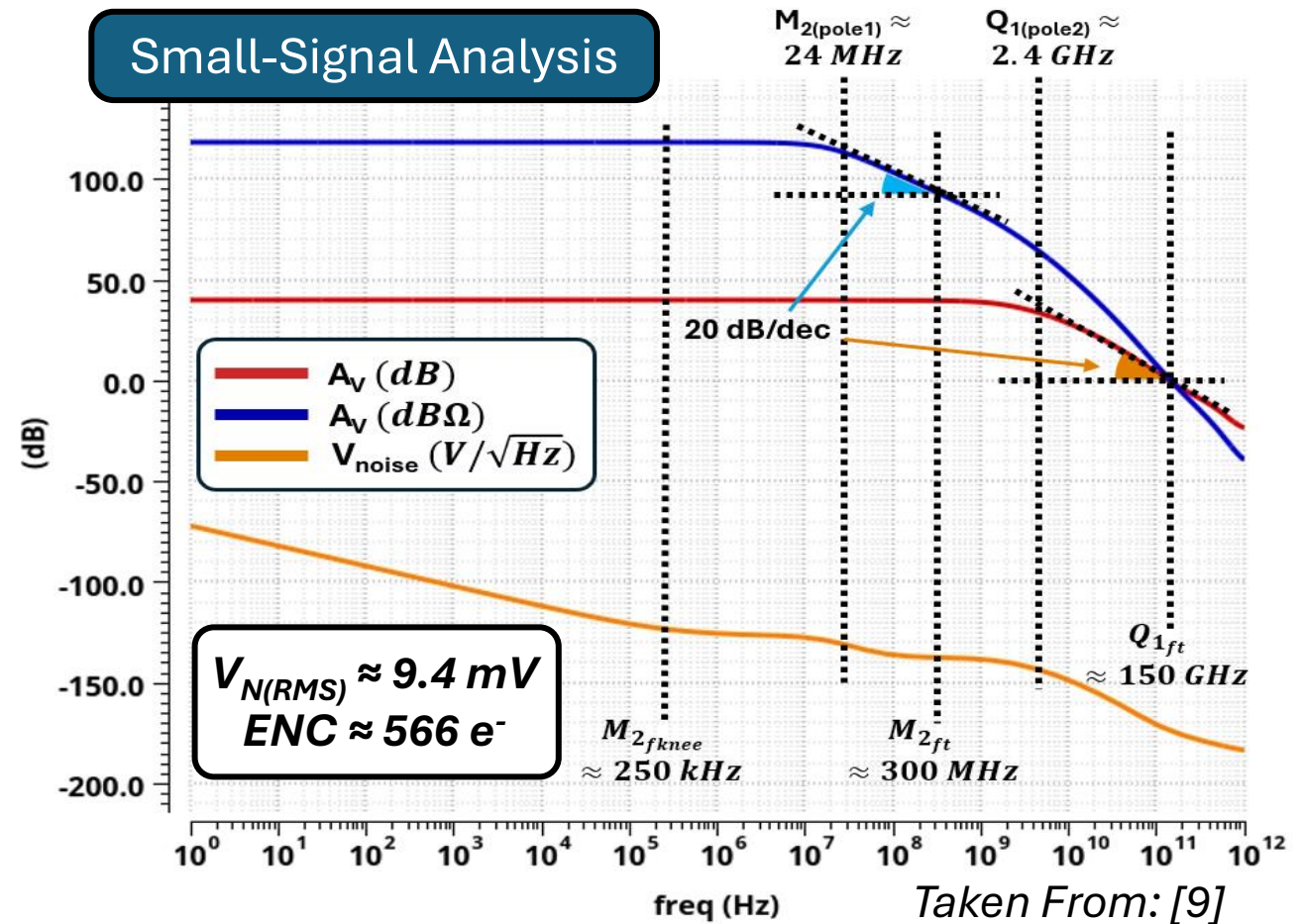
Readout Front-End ASIC Design

Readout Front-End ASIC Design

Transimpedance Amplifier (TIA)

Small-Signal Analysis

$V_{N(RMS)} \approx 9.4\ mV$
$ENC \approx 566\ e^-$

$M_{2(pole1)} \approx 24\ MHz$

$Q_{1(pole2)} \approx 2.4\ GHz$

- $A_V\ (dB)$
- $A_V\ (dB\Omega)$
- $V_{noise}\ (V/\sqrt{Hz})$

20 dB/dec

$Q_{1_{ft}} \approx 150\ GHz$

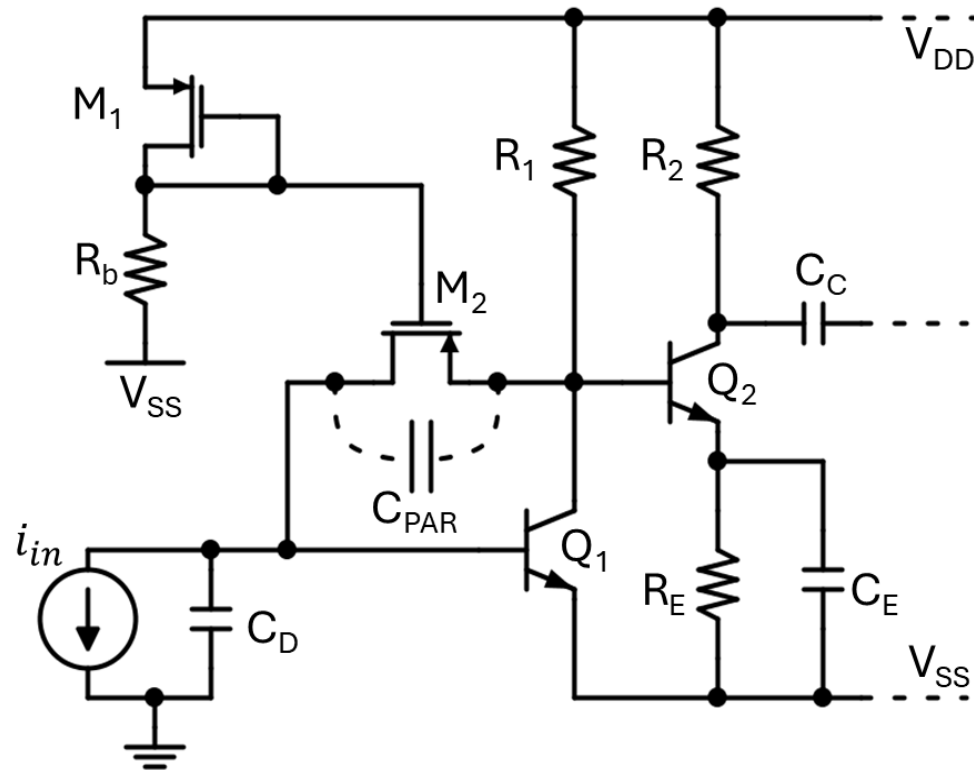$M_{2_{fknee}} \approx 250\ kHz$

$M_{2_{ft}} \approx 300\ MHz$

Taken From: [9]

Readout Front-End ASIC Design

Transimpedance Amplifier (TIA)

Large-Signal Analysis
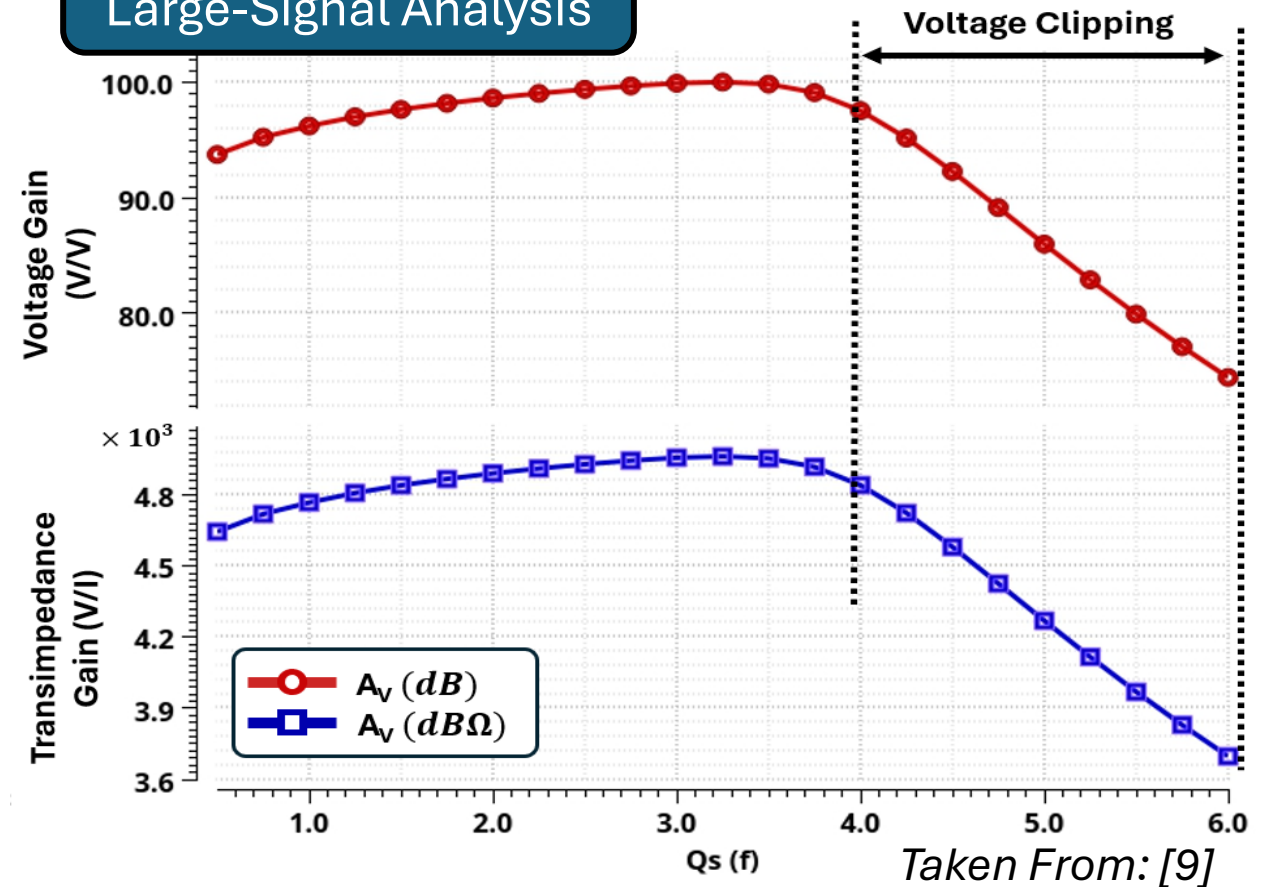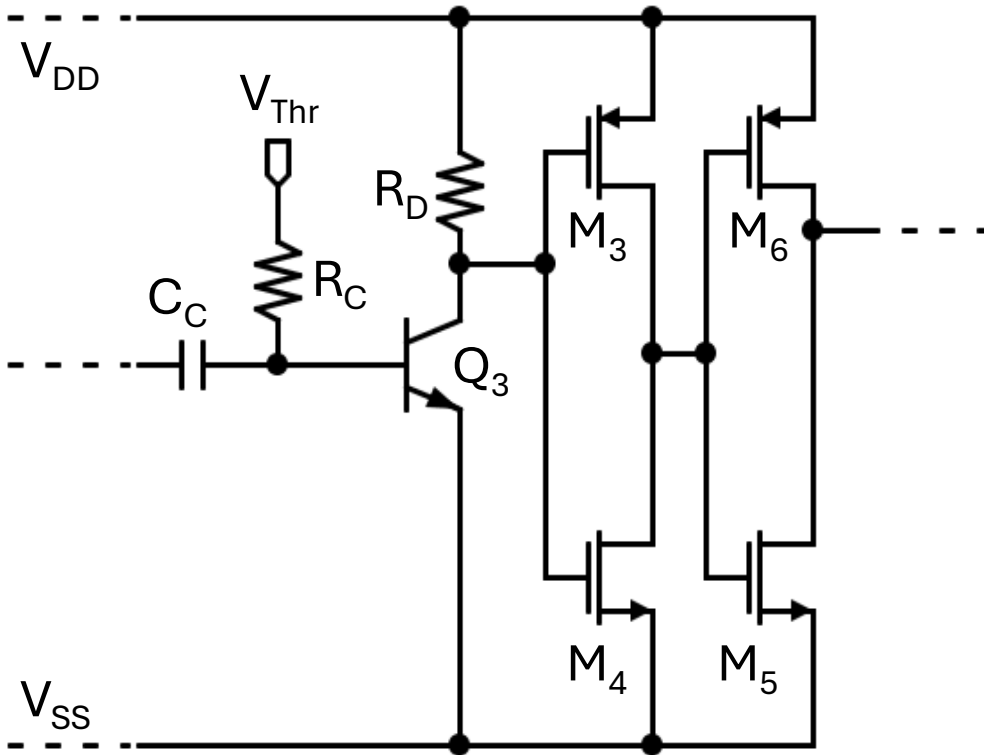
Taken From: [9]

Readout Front-End ASIC Design
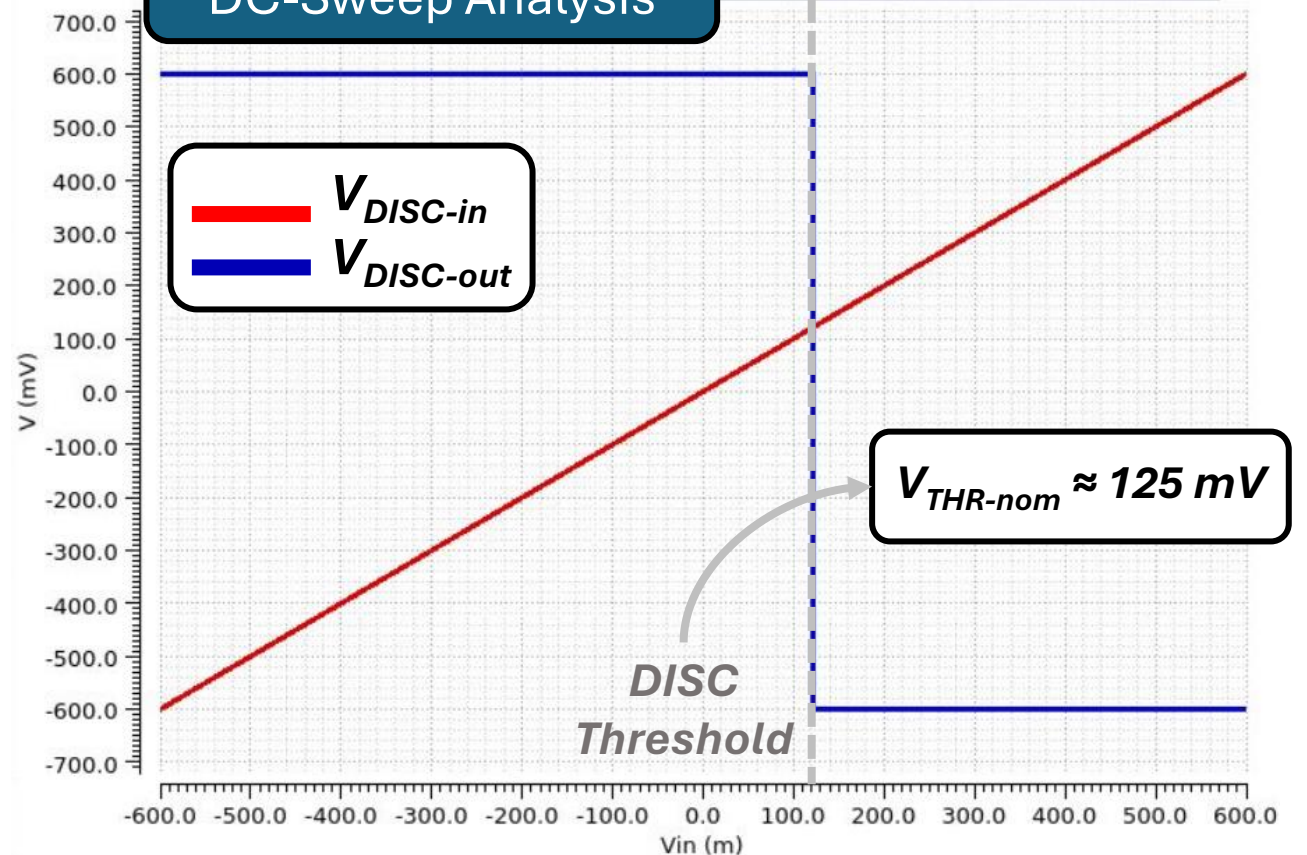
Readout Front-End ASIC Design

Discriminator (DISC)

Discriminator's Threshold Variations
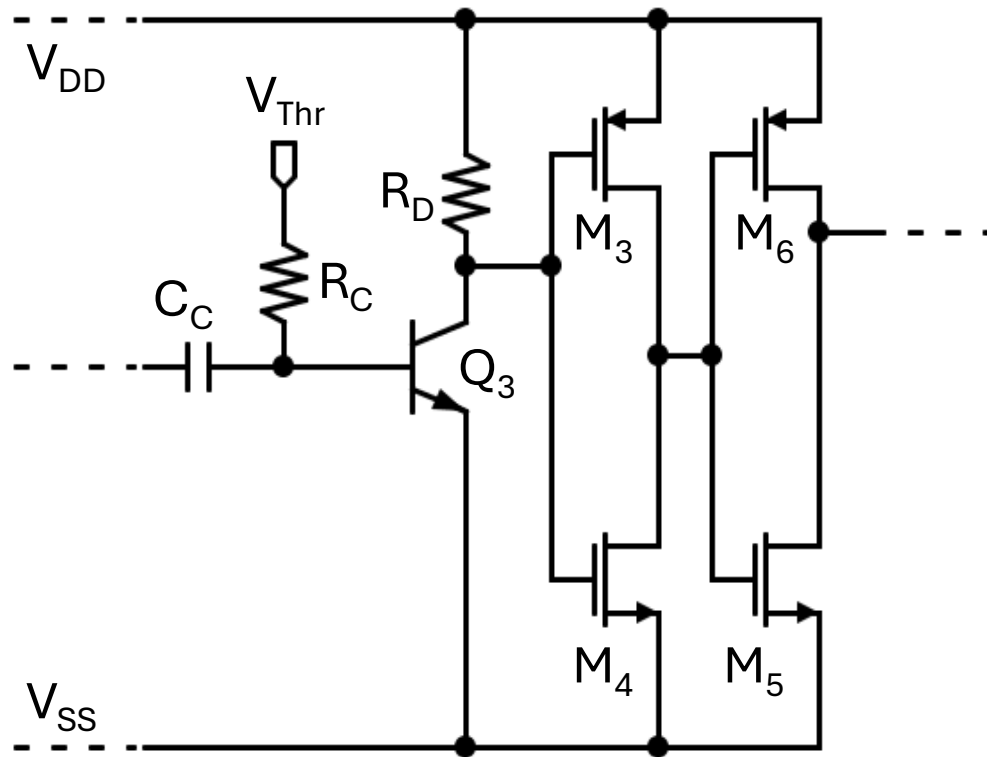(Monte Carlo Analysis)
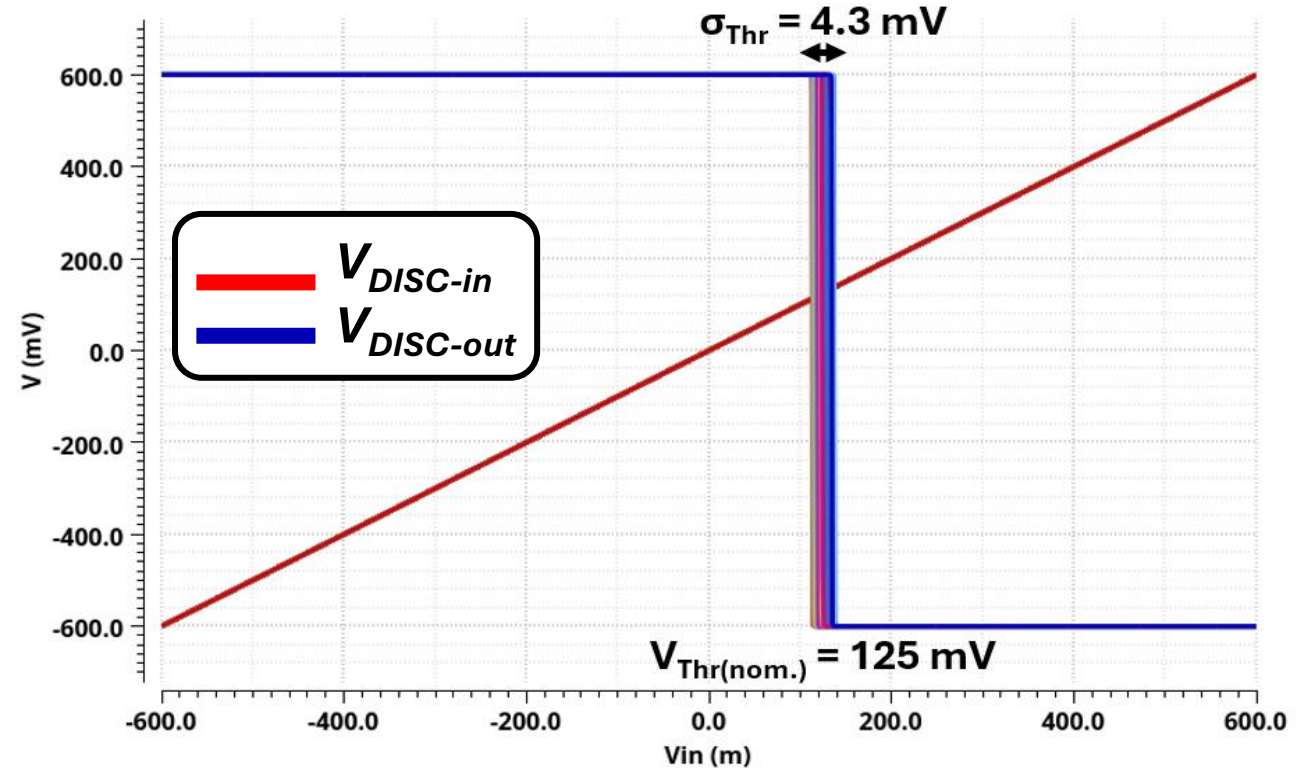
Readout Front-End ASIC Design

Discriminator (DISC)
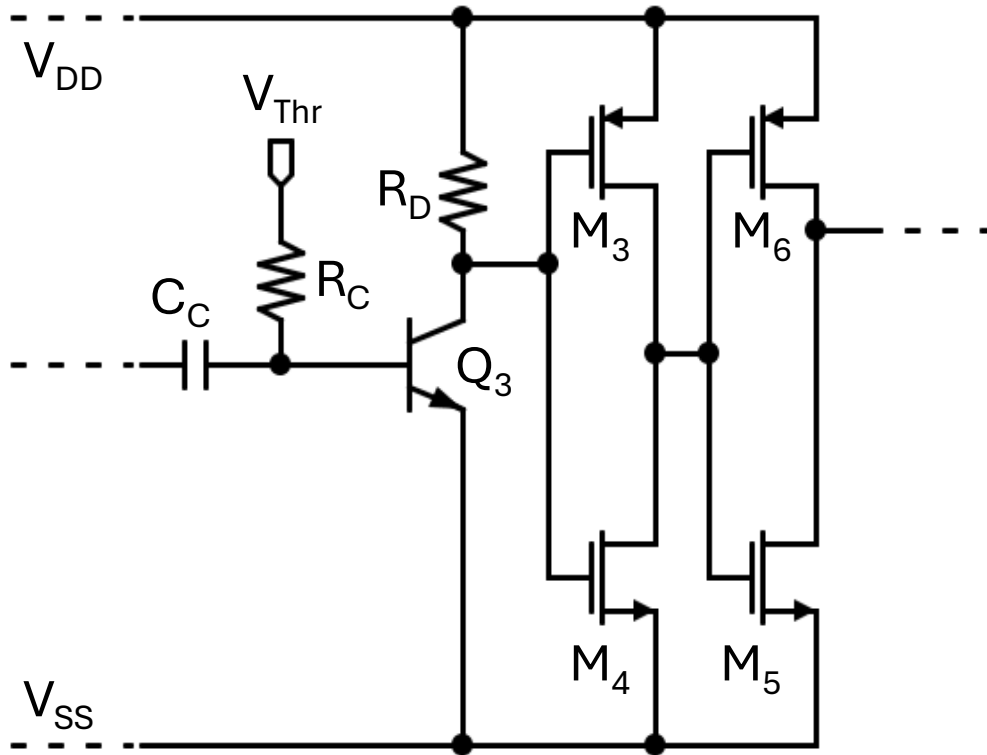
Discriminator's Threshold Variations (Monte Carlo Analysis)
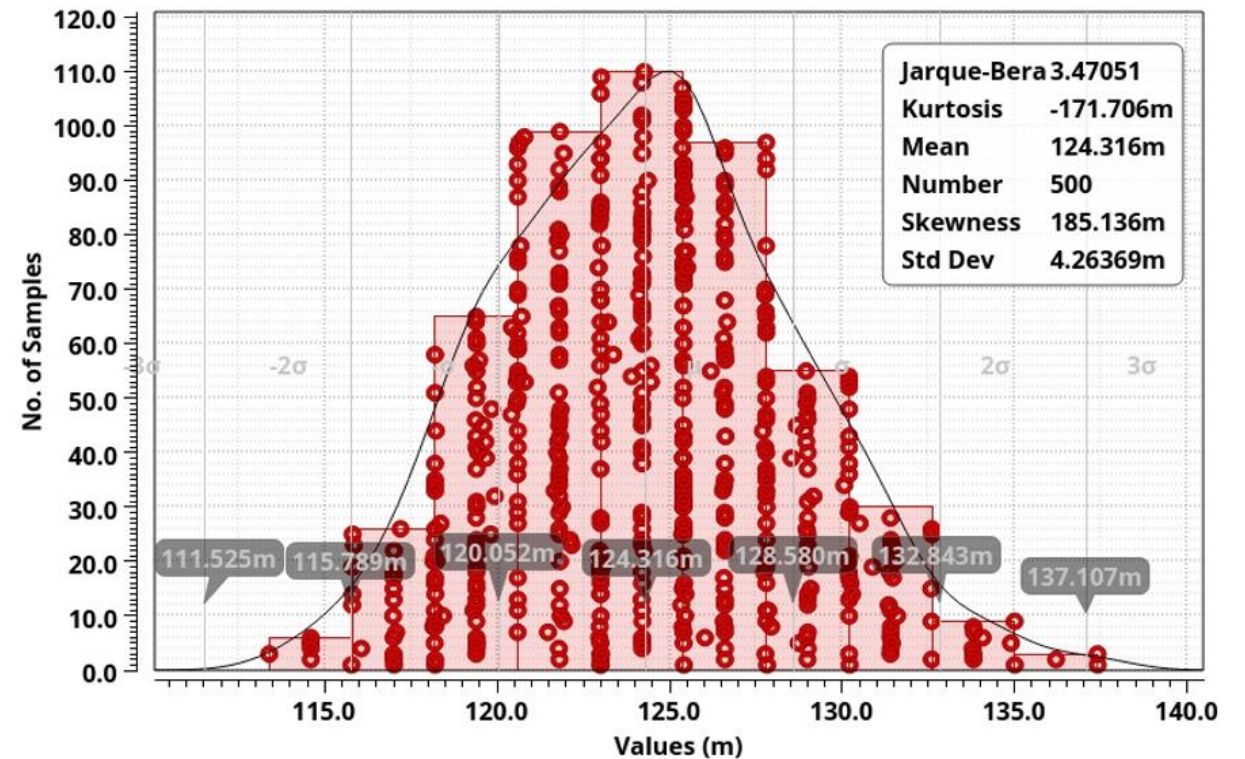
Readout Front-End ASIC Design

- Nominal threshold of this discriminator topology is practically the **V_{BE} of Q_3**.

- On top of nominal threshold, **ENC and threshold dispersion** should be considered as to suppress noise hits.

$$V_{Thr} = V_{Thr(nom.)} + 6 \times \sqrt{V^2_{noise(RMS)} + \sigma^2_{Thr}} \approx 190 \text{ mV}$$

$$Q_{Thr_{min}} \approx 3.9 \text{ ke}^-$$

Discriminator (DISC)
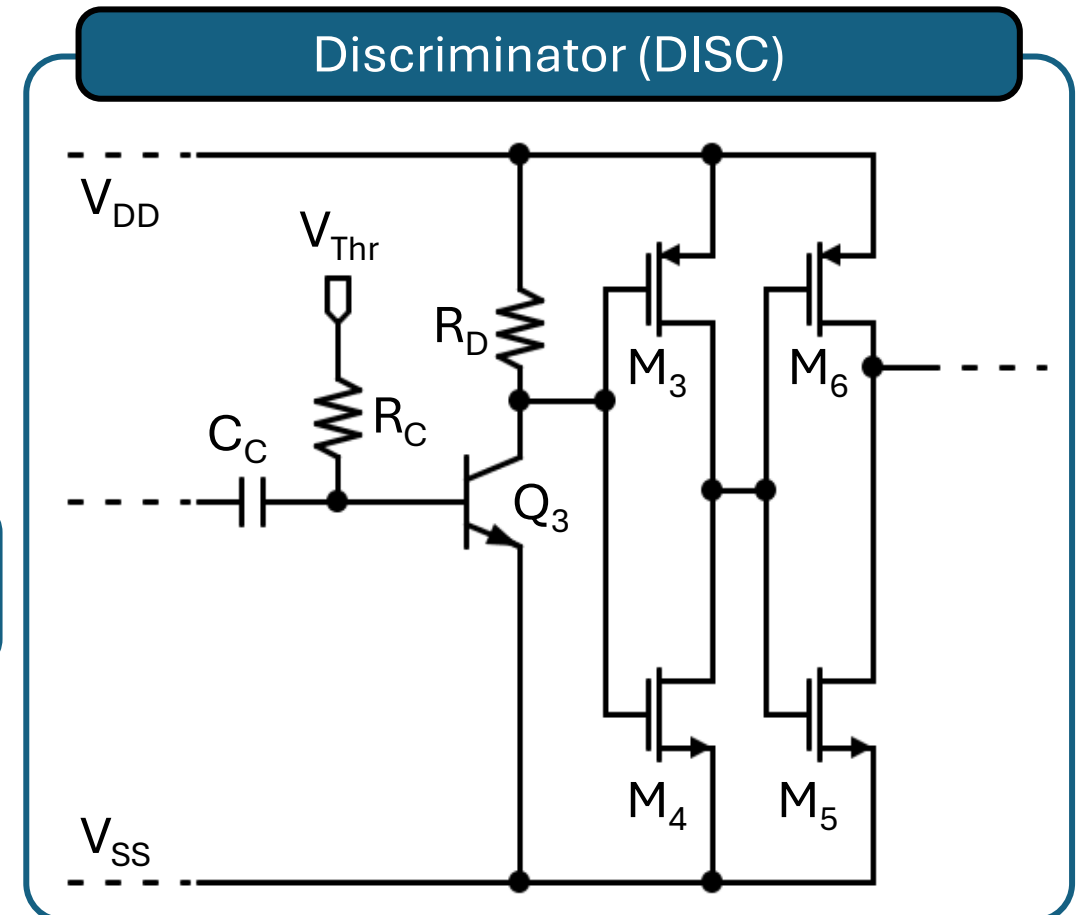
Readout Front-End ASIC Design
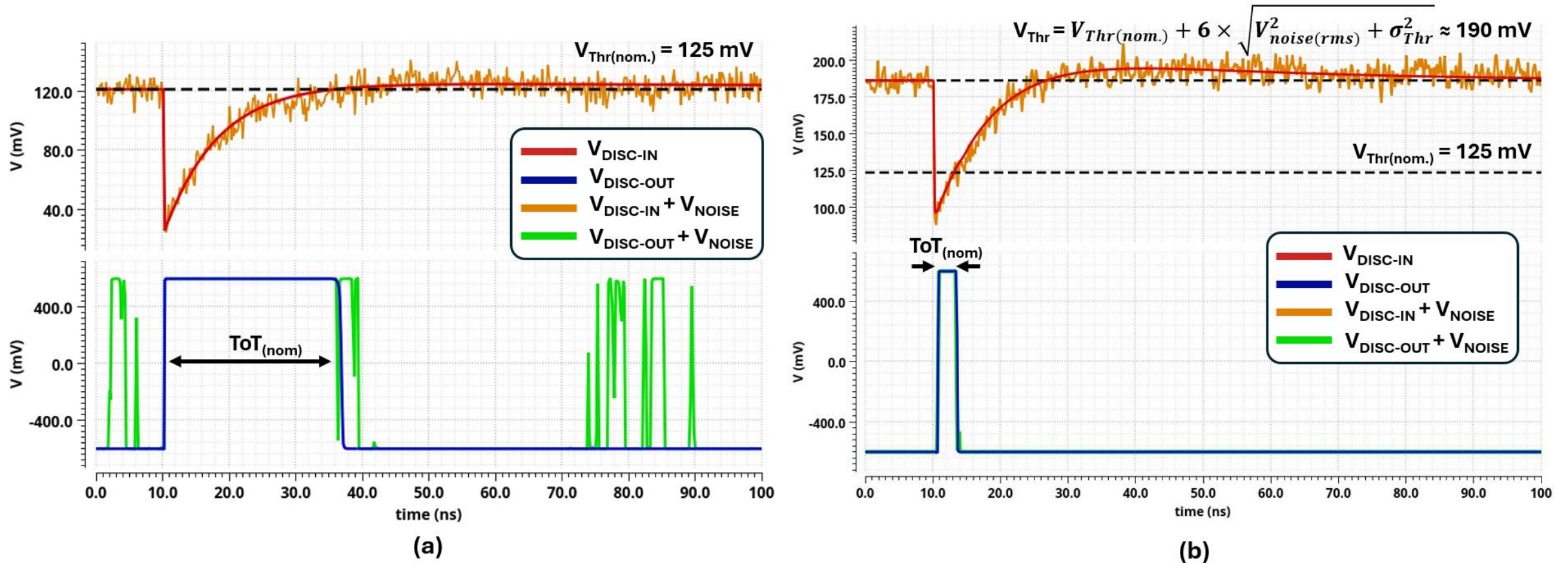
Simulations results of the discriminator's output hit-pulse signal (a) before and (b) after noise suppression (taken from: [9]).

Readout Front-End ASIC Design

- TDC clock is selected by simulating (as standalone) the TFF based on **True Single-Phase Clocked – TSPC** topology.

- High data fidelity is preserved for **clock frequencies < 5 GHz**, resulting in a TDC with **0.2 ns time resolution.**

$$0.2 \ \text{ns} \ \le \ t_{hit-pulse} \ \le \ 51.2 \ \text{ns}$$

Time-to-Digital Converter (TDC)
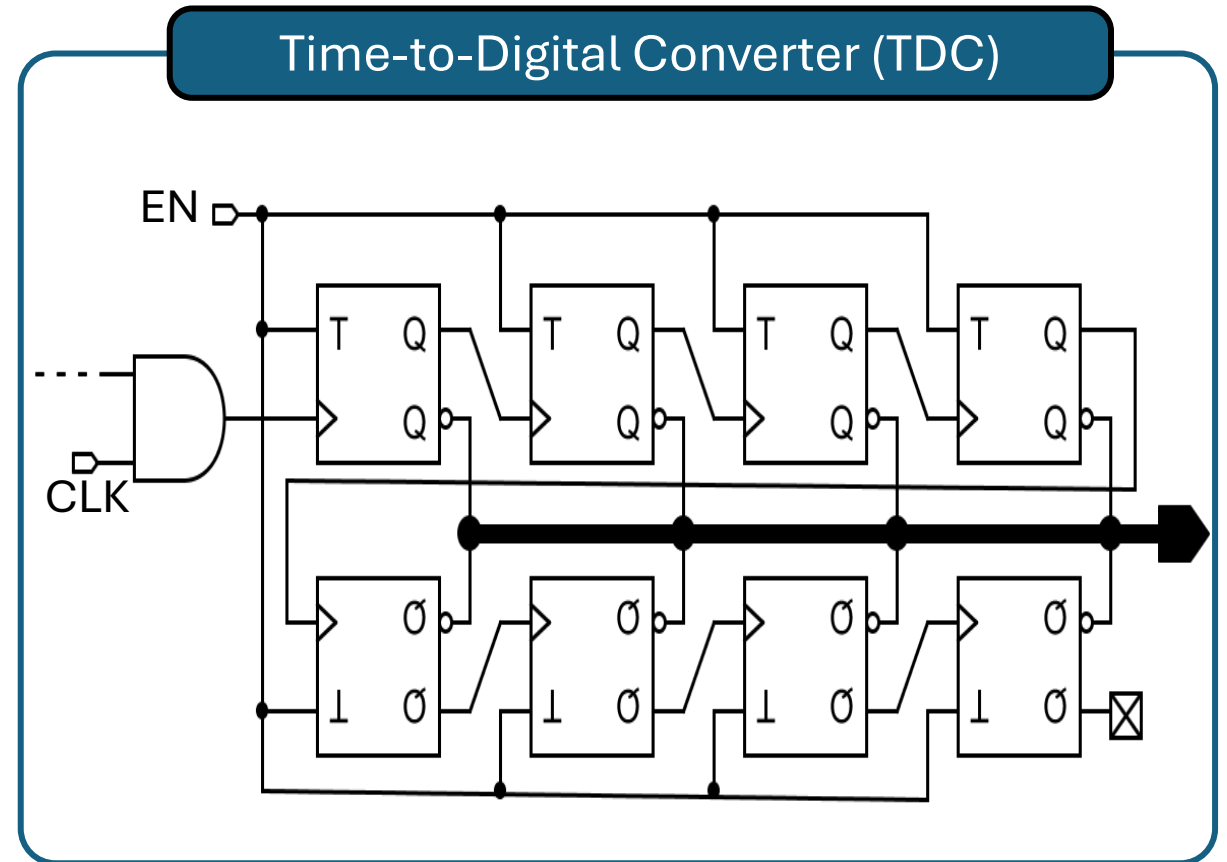
Readout Front-End ASIC Design

T Flip-Flop (TFF)

True Single-Phase Clocked TFF (TSPC-TFF)
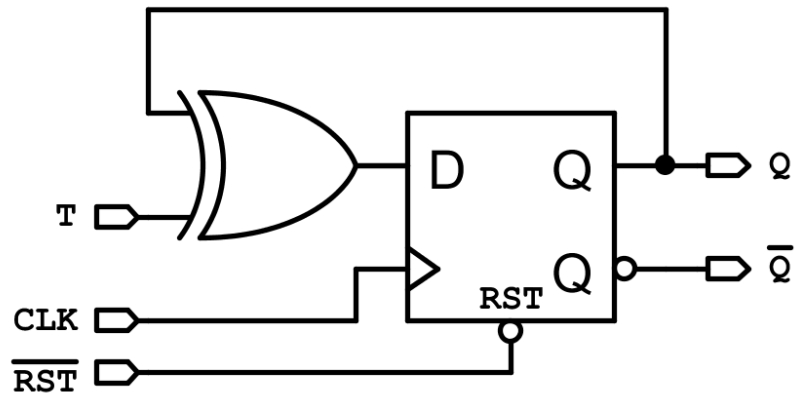
TFF Truth-Table

CLK	T	Q_{N+1}
↑	0	Q_N
↑	1	$\overline{Q_N}$
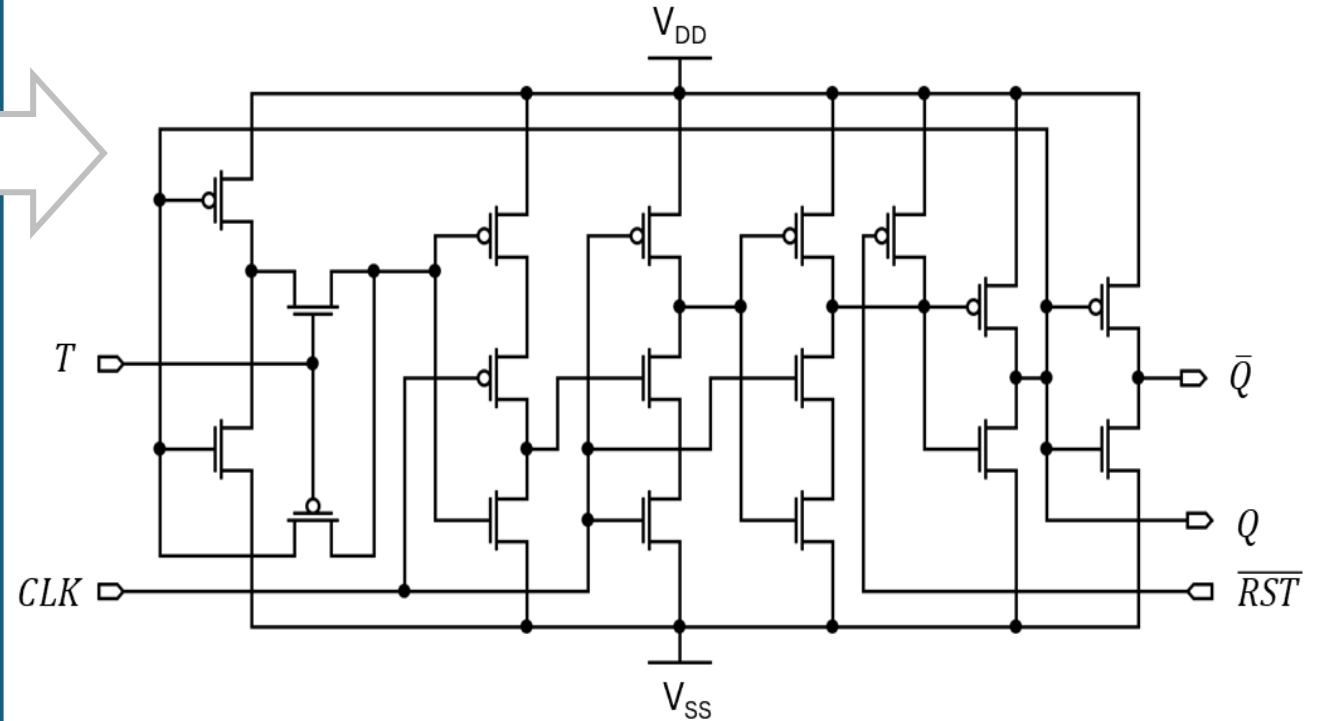
Readout Front-End ASIC Design
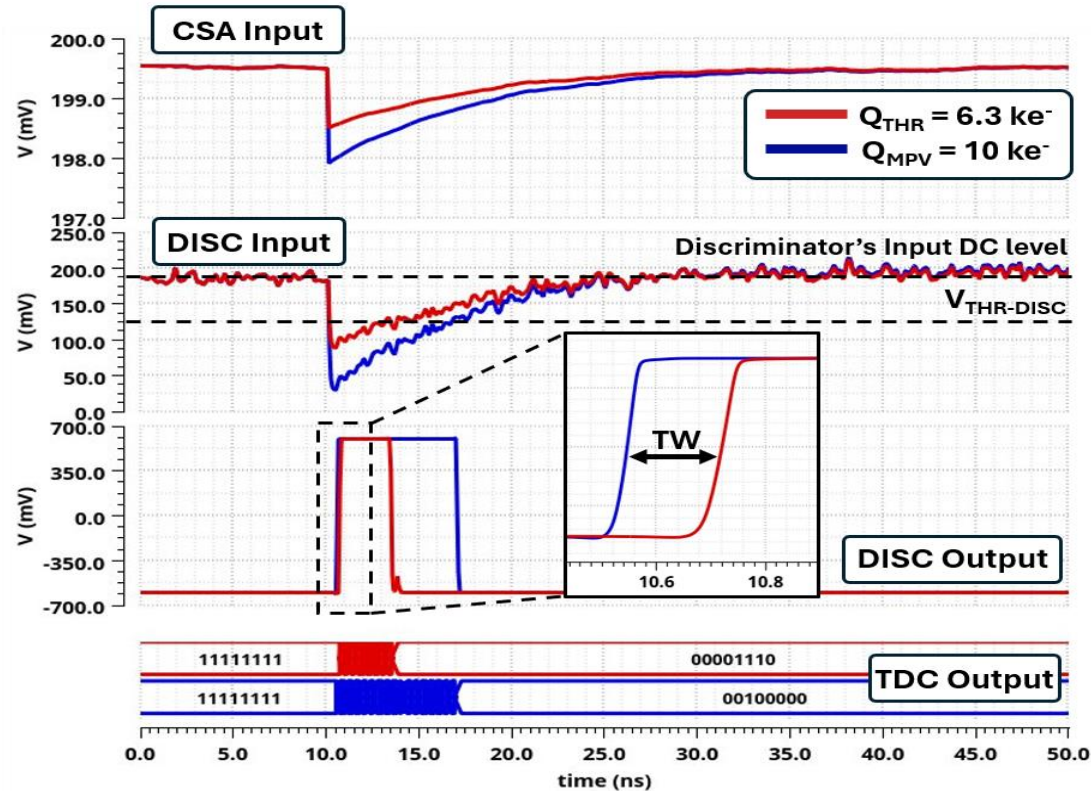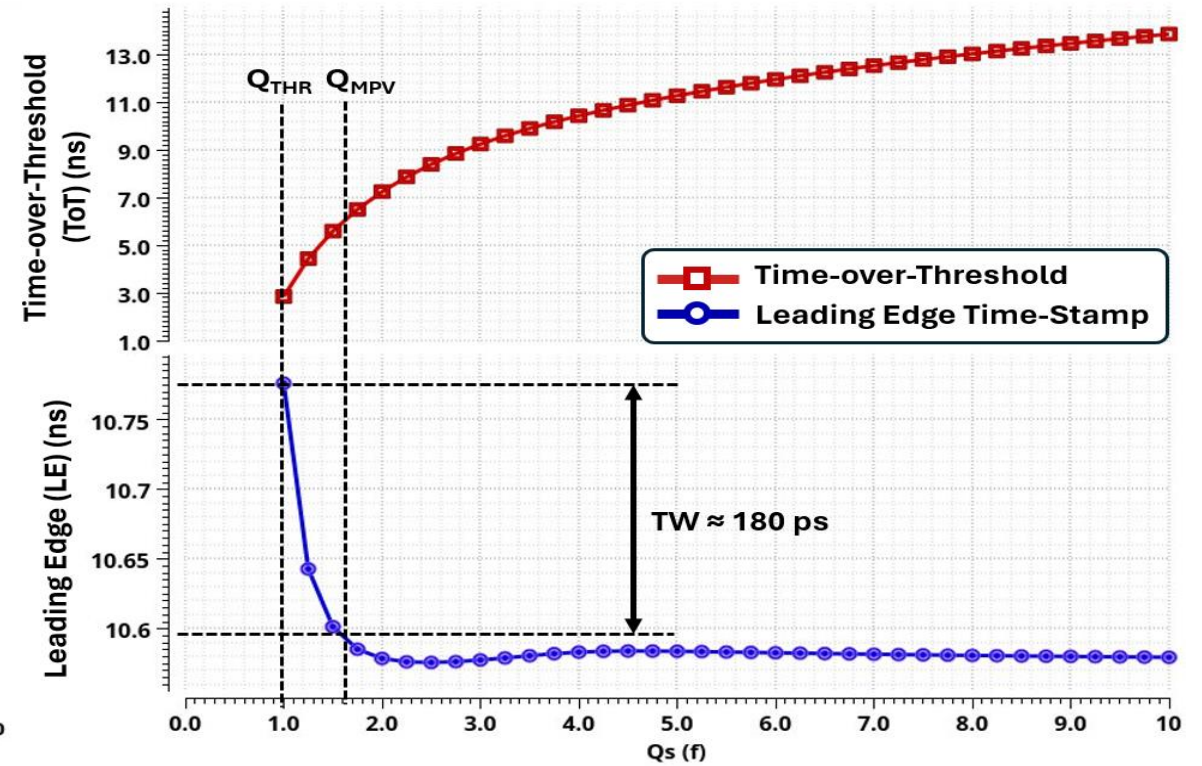
Simulations results in (a) the time-domain and (b) the timing-performance of the implemented front-end readout ASIC for detector capacitance of C_D = 1 pF (taken from: [9]).

Readout Front-End ASIC Design

Detector Capacitance (pf)	ENC (e-)	Discriminator's σ_{THR} (e-)	Q_{THR} (e-)	V_{THR} (mV)
0.5	294.5	271	2401.3	201.23
1	581.8	271	3850.9	186.13
1.5	868.9	271	5461.1	182.79
2	1156	271	7124.0	181.54
2.5	1443	271	8809.4	180.93
3	1729	271	10500.7	180.56
3.5	2016	271	12204.8	180.35
4	2303	271	13913.3	180.21

Detector Capacitance (pf)	$Q_{THR\ (In\text{-}Time)}$ (fC)	Time-Walk (MPV = 23 ke-)	Time-Walk (MPV = 10 ke-)
0.5	0.75	0.0674	0.0711
1	1.00	0.195	0.183
1.5	1.25	0.404	0.29
2	1.45	0.811	0.437
2.5	1.80	0.749	MPV below Q_{THR}
3	2.15	0.694	MPV below Q_{THR}
3.5	2.45	0.805	MPV below Q_{THR}
4	2.75	0.922	MPV below Q_{THR}
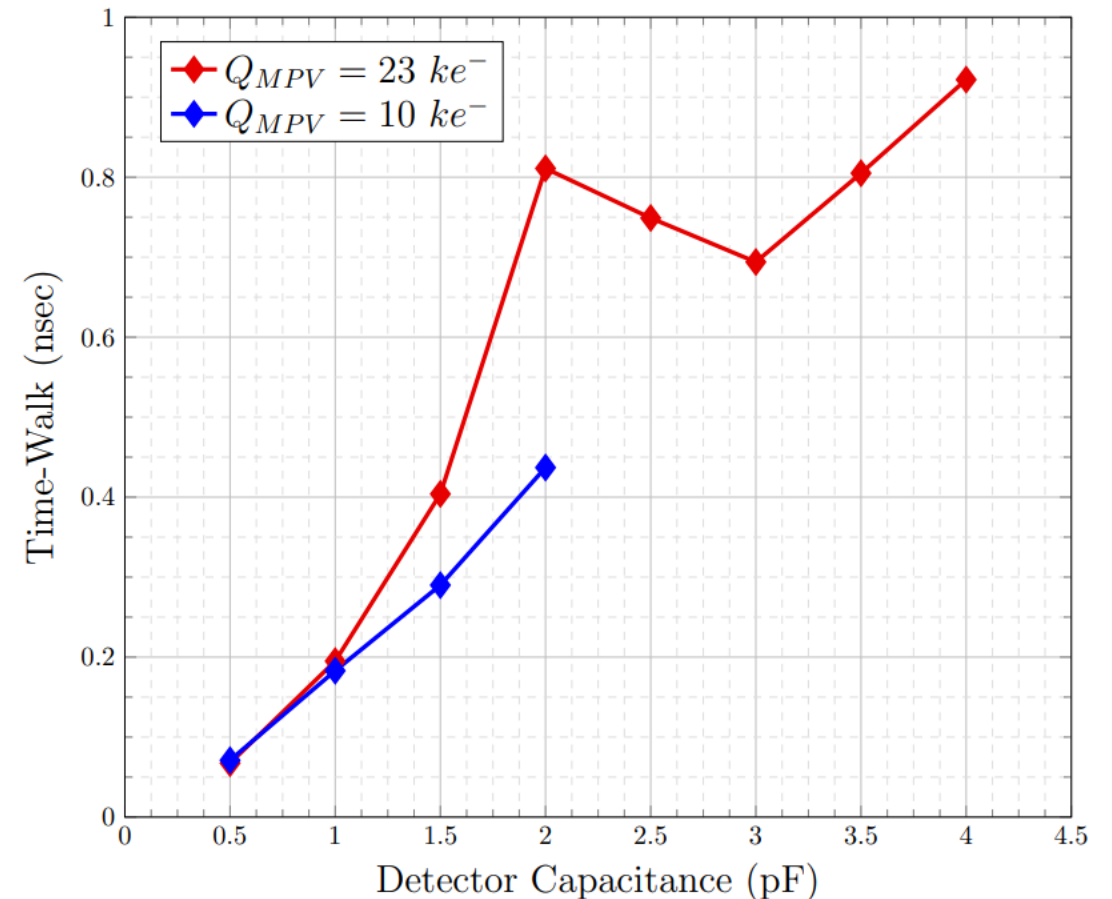
1. Introduction to Readout Electronics

2. Planar and 3D Pixel Detectors

3. Analog Front-End Circuitry and Analysis

4. Readout Front-End ASIC Design

5. **Conclusion and Discussion**

Conclusion and Discussion

- The designed front-end readout ASIC exhibit low **Time-Walk < 180 ps**, despite the large detector capacitance **C_D = 1 pF** of a 3D-pixel detector scheme.

- The observed **high noise is correlated to the high detector capacitance** used for the FE readout ASIC simulation.

- To achieve high timing-precision (low TW overhead), the **power consumption per pixel significantly increased**, reaching a power dissipation of **1 mW/pixel**.

- The **estimated pixel area** of the full readout ASIC design (TDC is included), was estimated close to **40×40 µm^2** via the properly sized PCELLs of the ASIC.

Conclusion and Discussion

Reference →		FE-I3	FE-I4	TDCpix	VFAT3	This
Specification ↓	Units	[17]	[29]	[30]	[31]	Work[c]
Process node	–	250 nm CMOS	130 nm CMOS	130 nm CMOS	130 nm CMOS	130 nm BiCMOS
Analog supply voltage	V	1.6	1.4	1.5	1.2	1.2
Charge Threshold – Q_{Thr}	ke⁻	4	3	3.6	18.9	3.2
Most Probable Value – Q_{MPV}	ke⁻	8–12	19.4	15.1	NR[a]	10
Equivalent Noise Charge – ENC	e⁻	200	300	180	653	566
Threshold dispersion – σ_{Thr}	e⁻	49	100	NR[a]	155	271
Charge gain – A_Q	mV/e⁻	NR[a]	0.055	0.011	0.008	0.017
Detector Capacitance – C_D	pF	0.4	0.5	0.25	1	1
Time-Walk – TW	ns	20	25	2	0.4	0.18
ToT resolution	bits	8	4	NR[a]	NR[a]	8
Power Dissipation – P_{Diss}	mW/pixel	0.042	0.014	0.28	1.3[b]	1
Pixel size – $Area_{pixel}$	μm²	50 × 400	50 × 250	300 × 300	NR[a]	40 × 40[d]

[a] Not Recorded.
[b] Estimated $P_{total}/channels$.
[c] Pre-layout results.
[d] Estimated.

Comparison of the implemented Front-End Readout ASIC performance (taken from: [9])

References

[1]:   ATLAS Collaboration, "The ATLAS Experiment at the CERN Large Hadron Collider", JINST 3 (2008).

[2]:   M. Garcia-Sciveres and N. Wermes, "A review of advances in pixel detectors for experiments with high rate and radiation", Rept. Prog. Phys. 81 (2018).

[3]:   Minwoong Lee et al. "Radiation-tolerance analysis of I-gate n-MOSFET according to isolation oxide module in the CMOS bulk process", Microelectronic Engineering 200 (2018).

[4]:   W. Snoeys et al., "Layout techniques to enhance the radiation tolerance of standard CMOS technologies demonstrated on a pixel detector readout chip", Nuclear Instruments and Methods in Physics Research A 439 (2000).

[5]:   H. Puchner et al., "Elimination of Single Event Latchup in 90nm SRAM Technologies," 2006 IEEE International Reliability Physics Symposium Proceedings (2006).

[6]:   A. Karagounis, "Analog integrated CMOS circuits for the readout and powering of highly segmented detectors in particle physics applications" (2010).

[7]:   F. Hartmann, "Evolution of Silicon Sensor Technology in Particle Physics", Springer, Berlin, Heidelberg (2009).

References

[8]: F. Hartmann & J. Kaminski, "Advances in Tracking Detectors", Annual Review of Nuclear and Particle Science, 61(1) (2011).

[9]: A. Michailidis, V. Gogolou, T. Noulis & J. Dingfelder, "Charge-sensitive amplifier design for high-speed interface readout front-end ASICs", AEU - International Journal of Electronics and Communications (2024).

[10]: G.T. Forcolin, M. Boscardin, F. Ficorella, A. Lai, A. Loi, R. Mendicino, S. Ronchin, G.-F. Dalla Betta, "3D trenched-electrode pixel sensors: Design, technology and initial results", Nuclear Instruments and Methods in Physics Research Section A (2020).

[11]: K. Moustakas, "Design and development of depleted monolithic active pixel sensors with small collection electrode for high- radiation applications", Rheinische Friedrich-Wilhelms-Universität Bonn (2021).

[12]: A. Michailidis, T. Noulis and K. Siozios, "CMOS Noise Analysis and Simulation From Low Frequency and Baseband to RF and Millimeter Wave," in IEEE Access (2023).

[13]: C. Leyris et. al., "Impact of Random Telegraph Signal in CMOS Image Sensors for Low-Light Levels," 32nd European Solid-State Circuits Conference, Montreaux, Switzerland (2006).

Thank You!

Any Questions?