The Future Beauty

LHCb Upgrade II with the **Mighty-Tracker**

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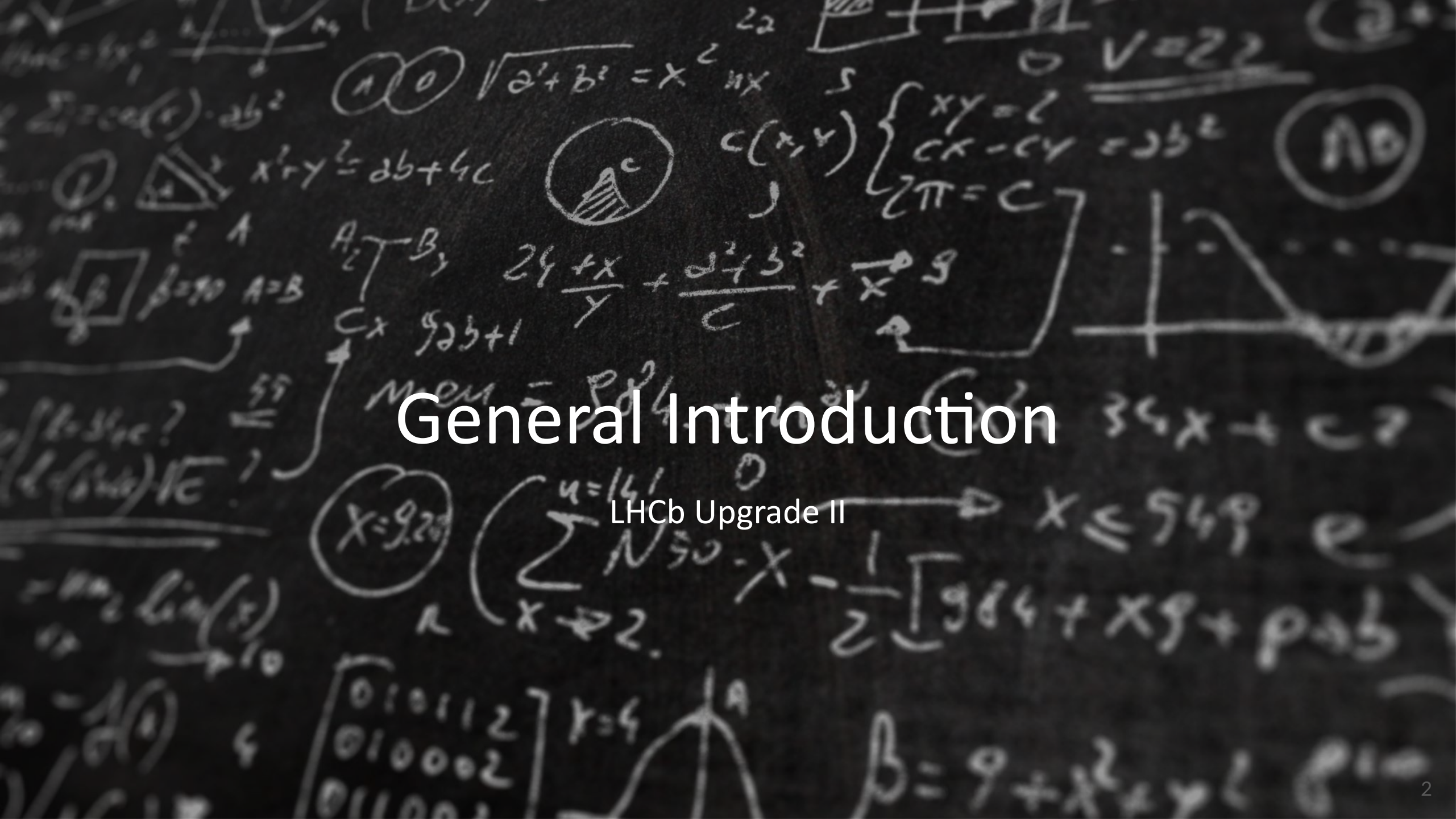
UNIVERSITÄT BONN

HISKP

LHCb

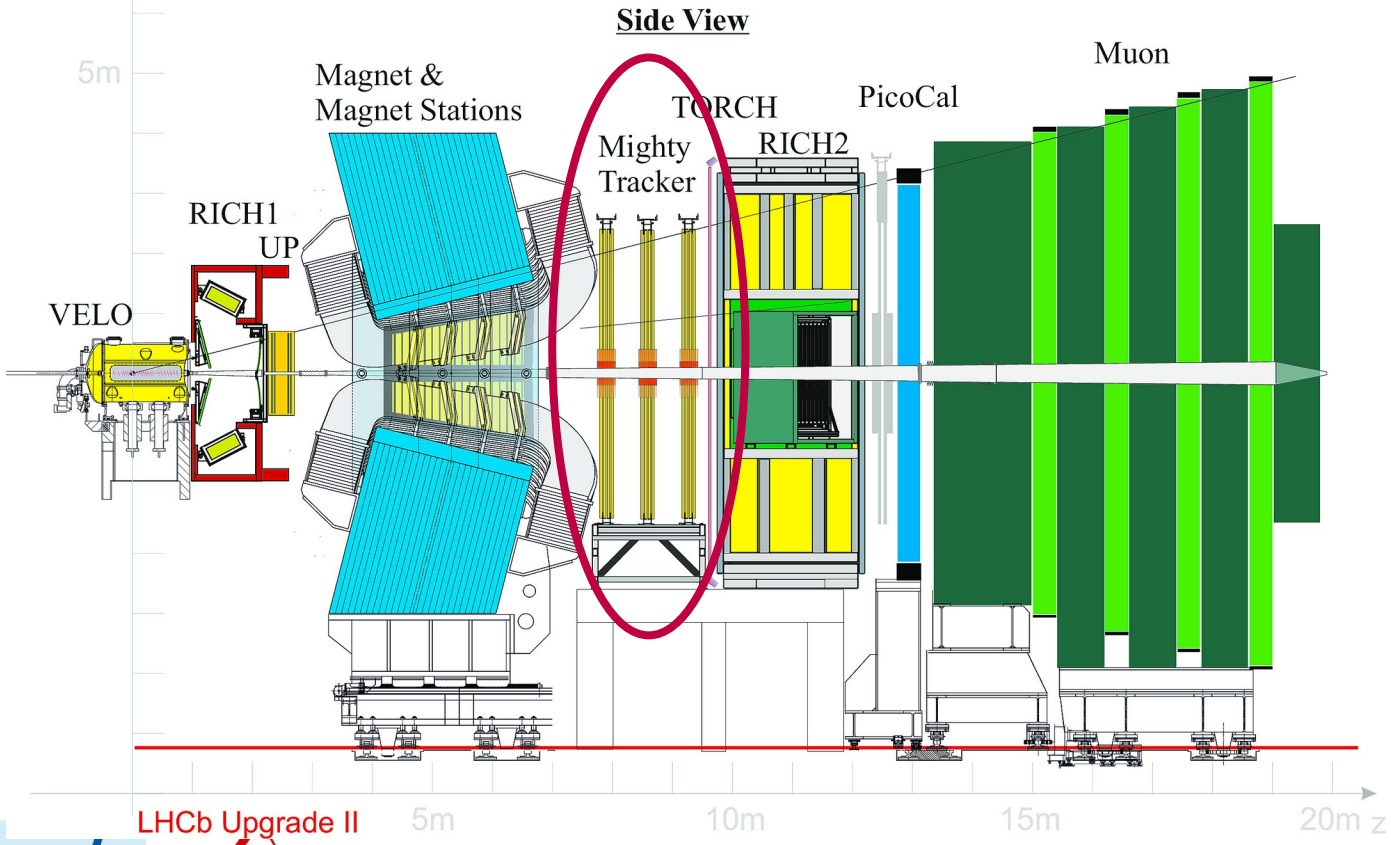


General Introduction

LHCb Upgrade II

The Upgrade II Detector (2034)

Without a major upgrade to all detectors LHCb will not be able to run at these high luminosities.



LHCB-TDR-026

Velo
- 4D tracks with <20 ps
- 1.2 × 10^{12} tracks/cm^2 at r=1cm

UT
- HVCMOS
- 9.0 Gbps

Magnet Stations
- new

MT/SciFi
- next slides

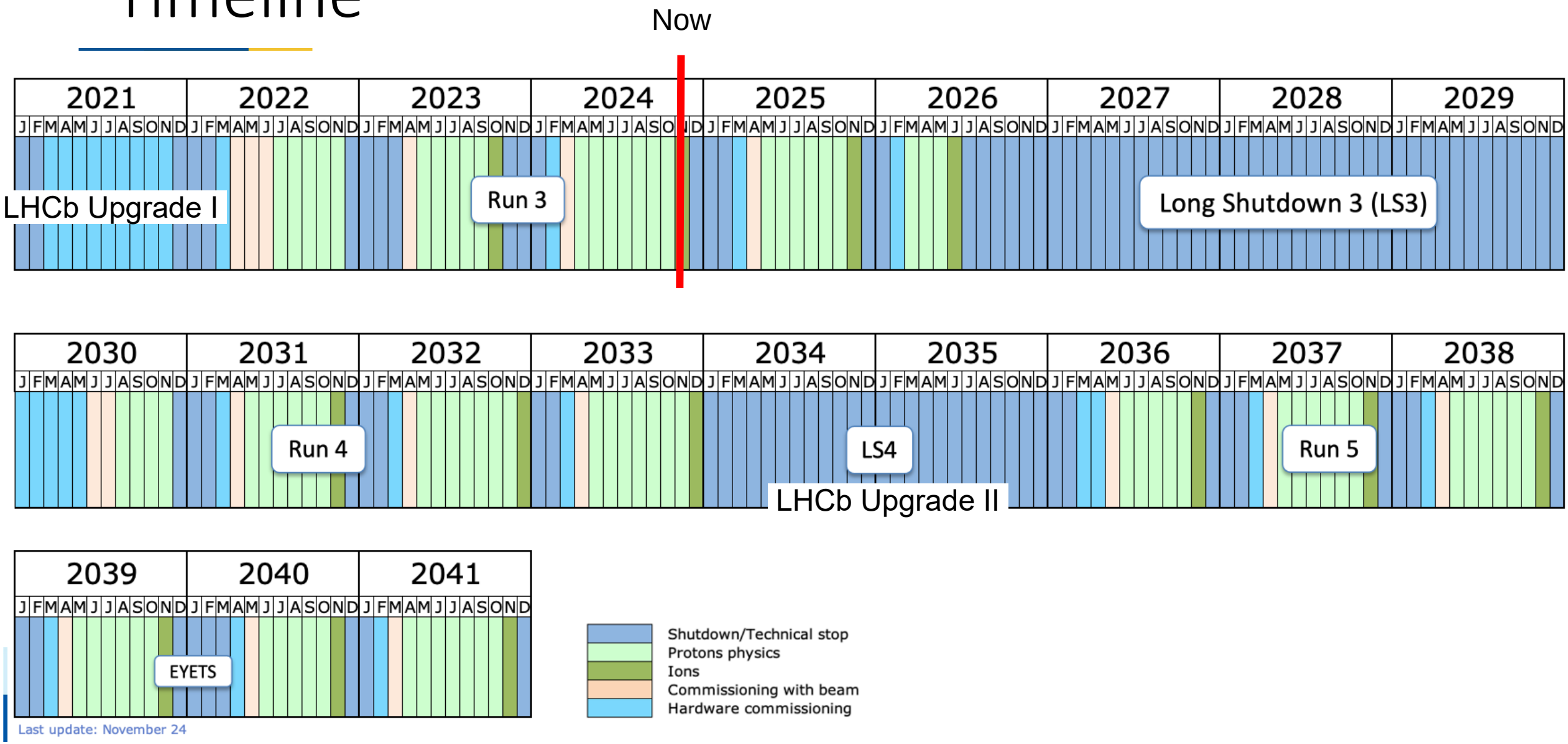
RICH
- 50ps timing
- SiPM (higher resolution)

TORCH
- new (20ps timing layer)

ECAL, HCAL
- SpaCal+Shashlik
- time + space resolution

MUON Stations
- higher granularity
- maybe shielding

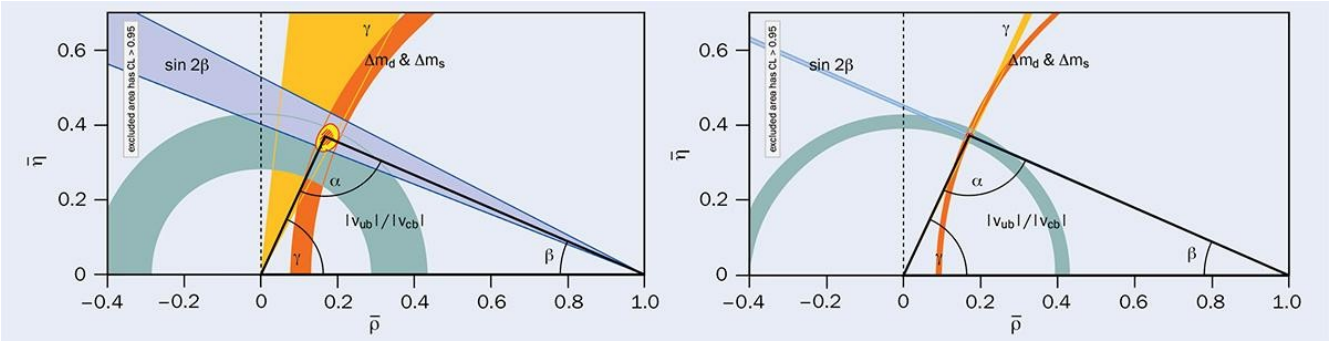
Timeline

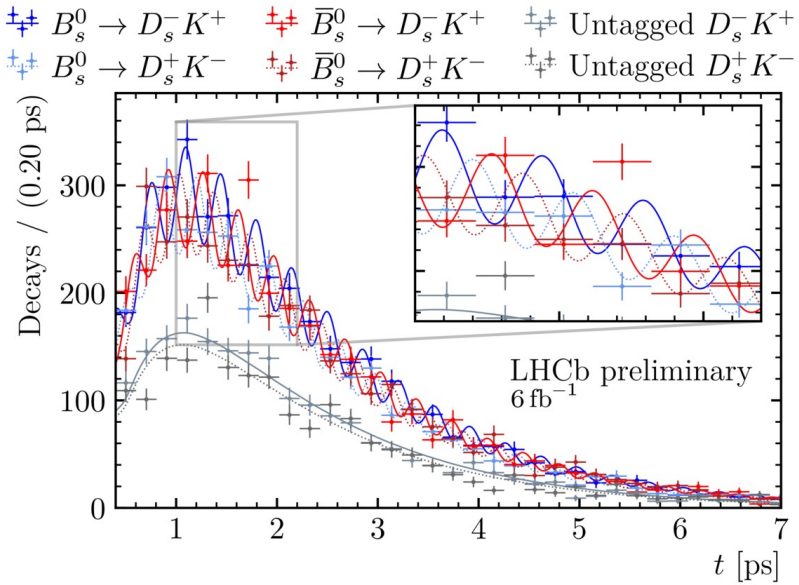

Now
2021
2022
2023
2024
2025
2026
2027
2028
2029
LHCb Upgrade I
Run 3
Long Shutdown 3 (LS3)
2030
2031
2032
2033
2034
2035
2036
2037
2038
Run 4
LS4
Run 5
LHCb Upgrade II
2039
2040
2041
EYETS
Shutdown/Technical stop
Protons physics
Ions
Commissioning with beam
Hardware commissioning
Last update: November 24

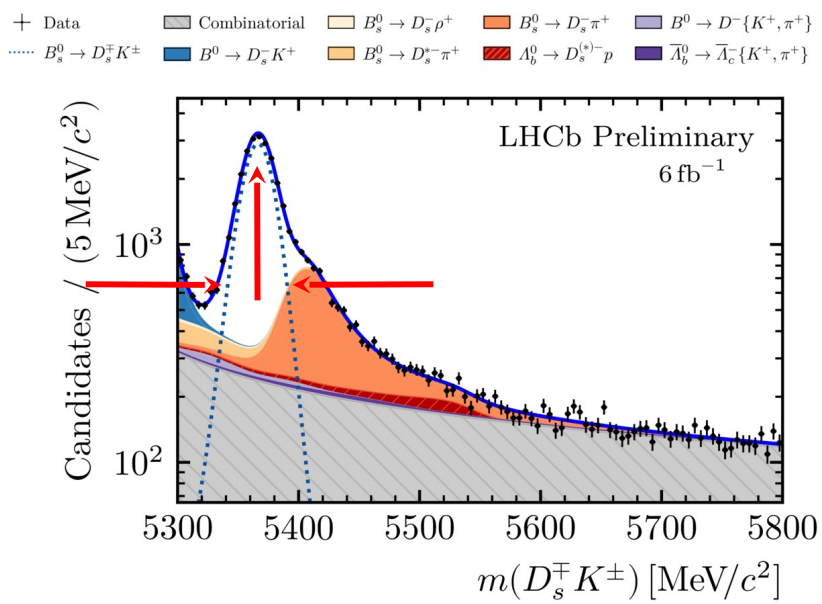
Goal of the Upgrade

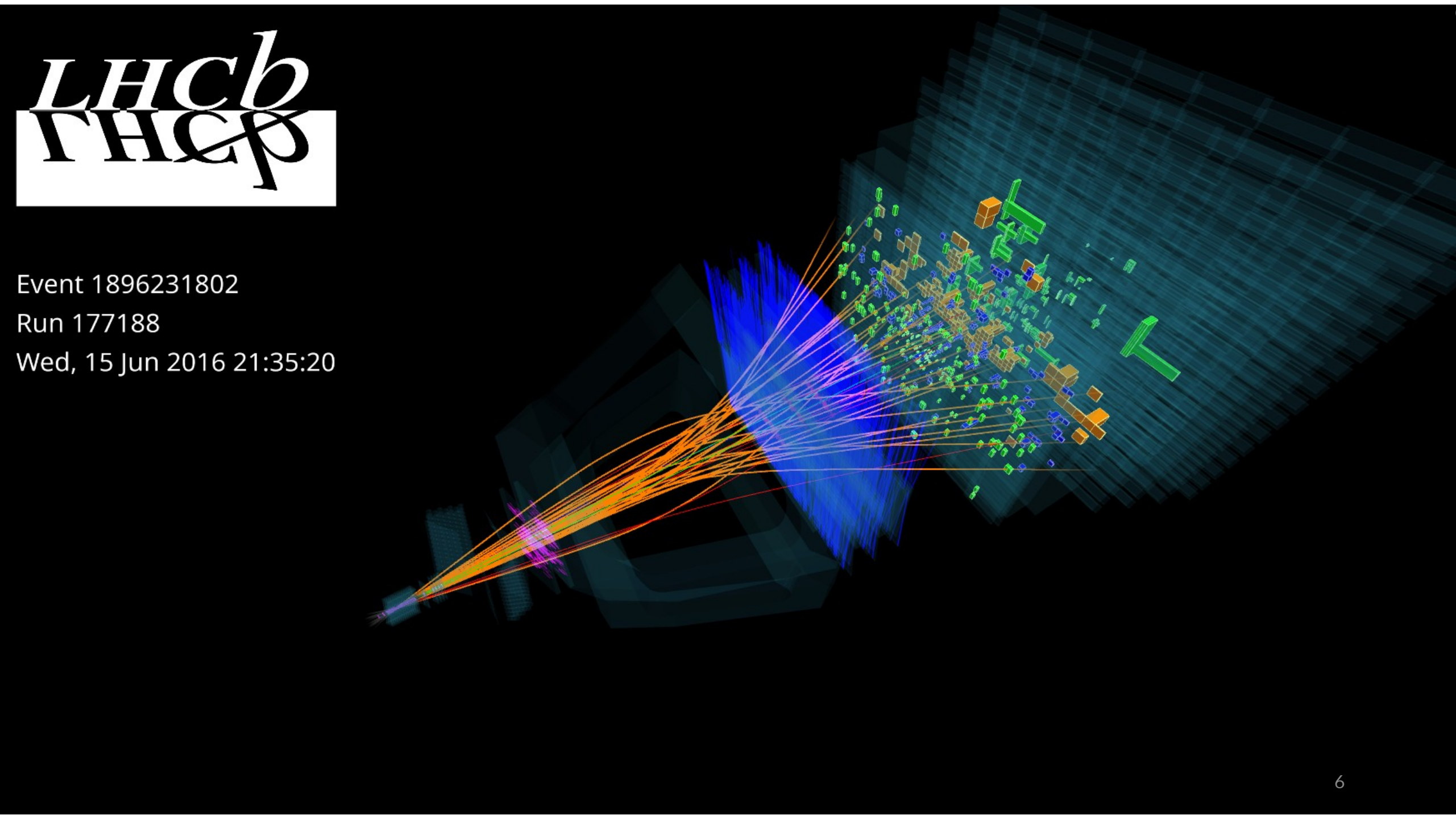
- More statistics
- Higher Precision

→ Better Physics Results







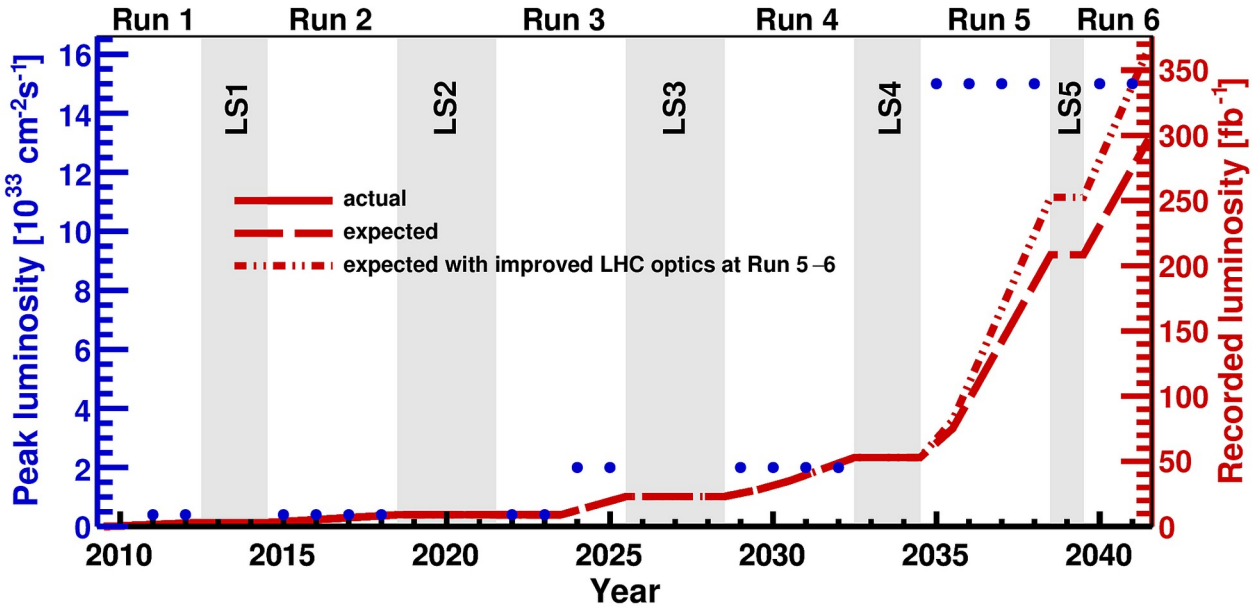

LHCb
Event 1896231802
Run 177188
Wed, 15 Jun 2016 21:35:20

The Upgrade II Conditions (2034)

Run 3-4	Run 5-6
2×10^{33} cm^{-2} s^{-1}	1.5×10^{34} cm^{-2} s^{-1}
50 fb^{-1}	250 fb^{-1}
<μ>=7	<μ>=50
radiation hard	Current detectors will not work in this radiation enviroment

Streamless Readout

acceptance η=1.9 to 5



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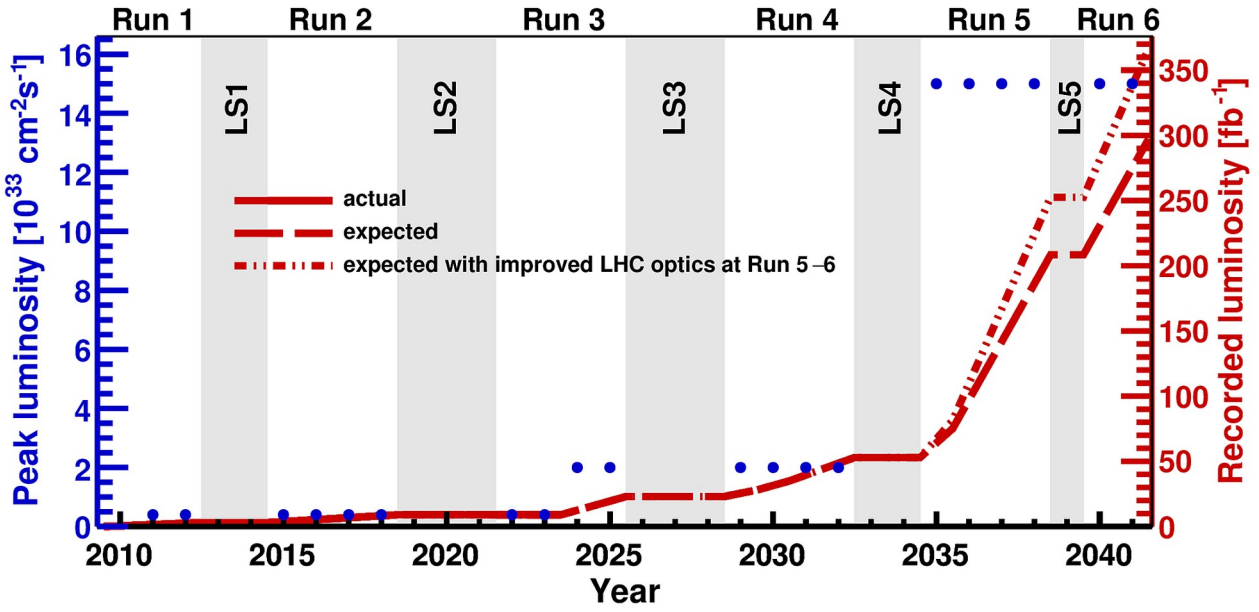


Untriggered readout @40MHz

Streaming Readout

LHCb uses no Hardware Trigger

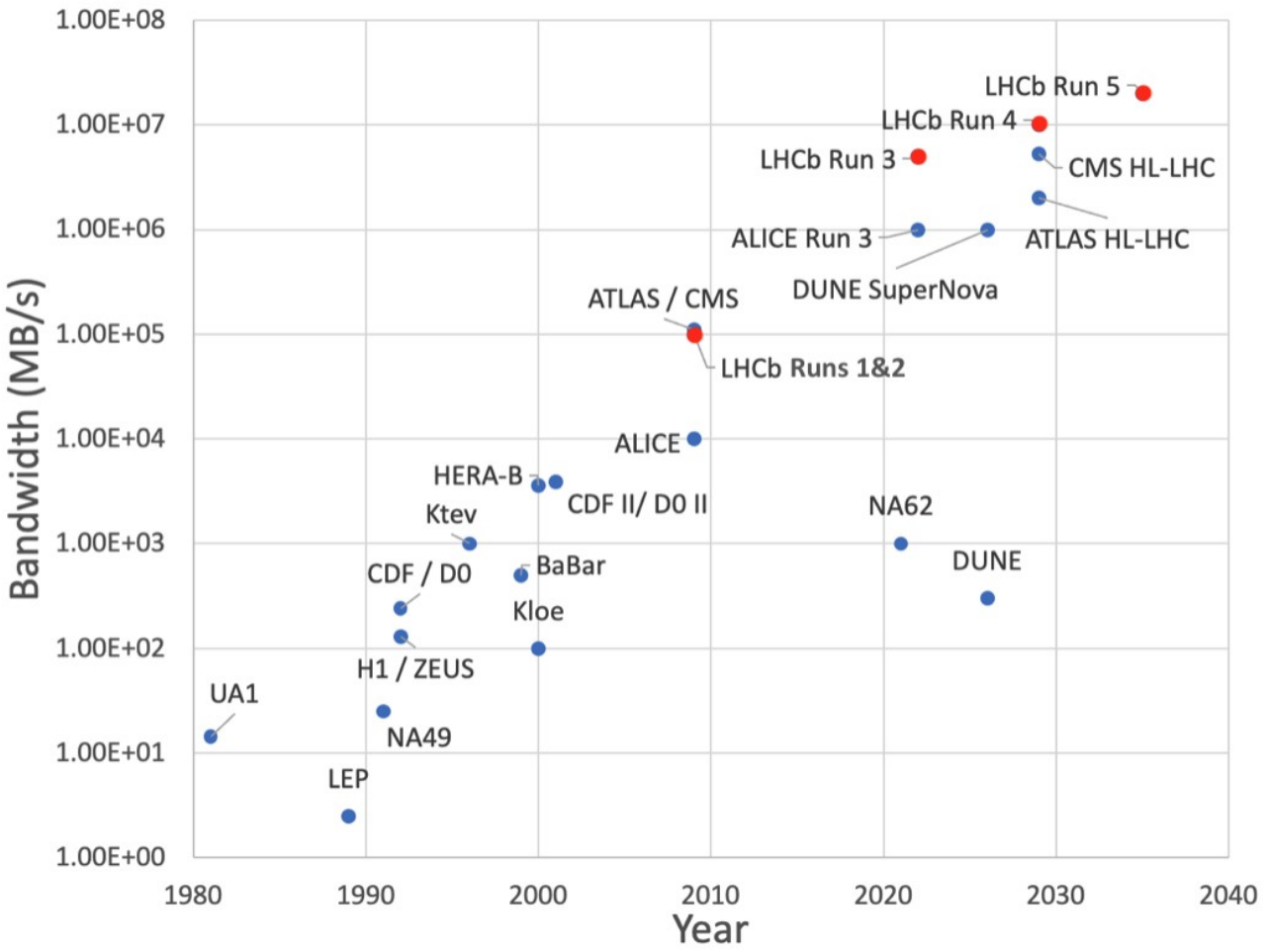
All data is processed and reconstructed

LHCb is the experiment with the worlds highest bandwidth output!

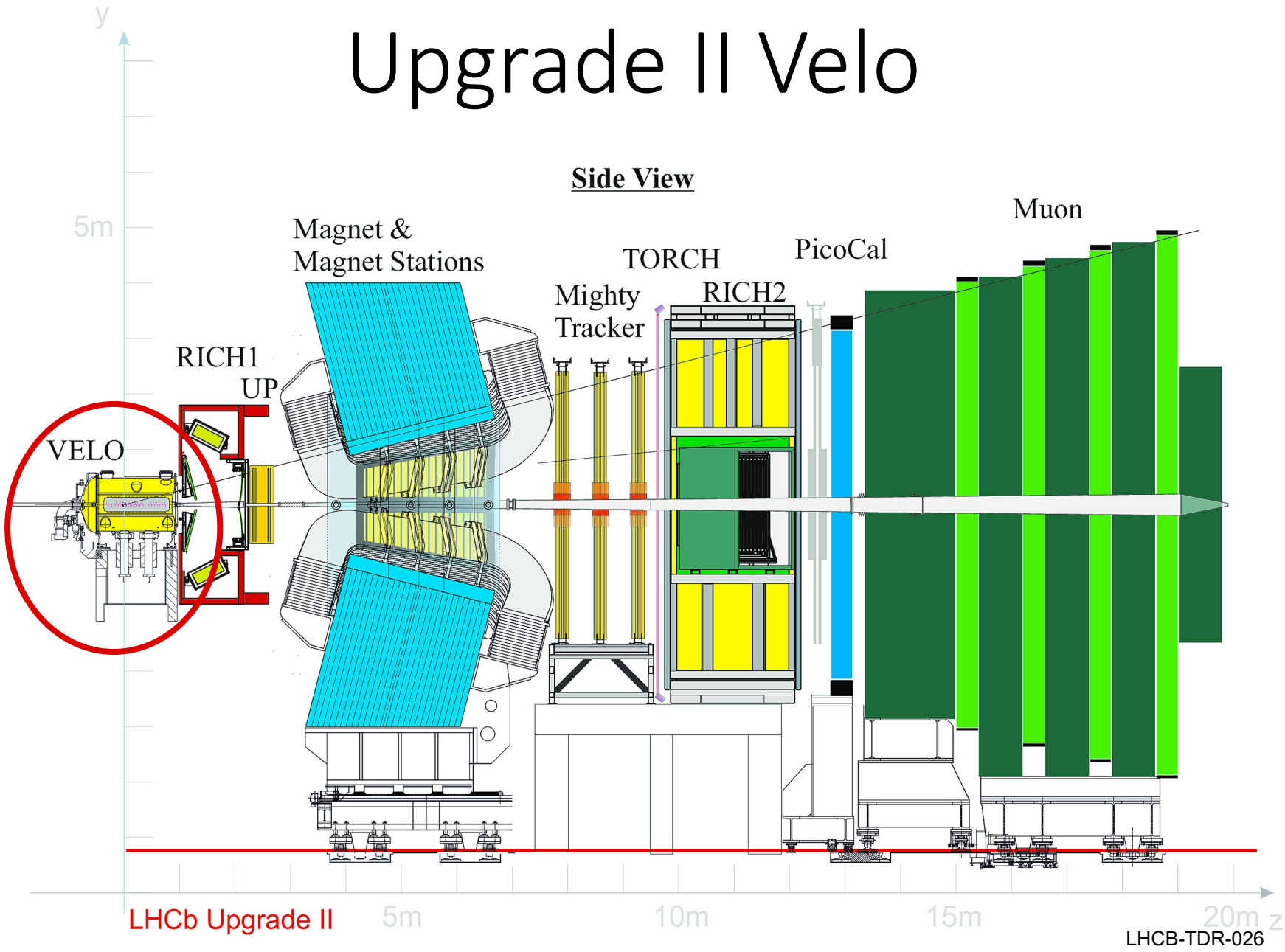
LHCb now is at the level of the coming ATLAS and CMS upgrades ~O(TB/s)

We will have to 10TB/s in LS3 (new RICH and ECAL

For Upgrade II in LS4 we expect a Bandwidth requirement of 25TB/s



Upgrade II Velo



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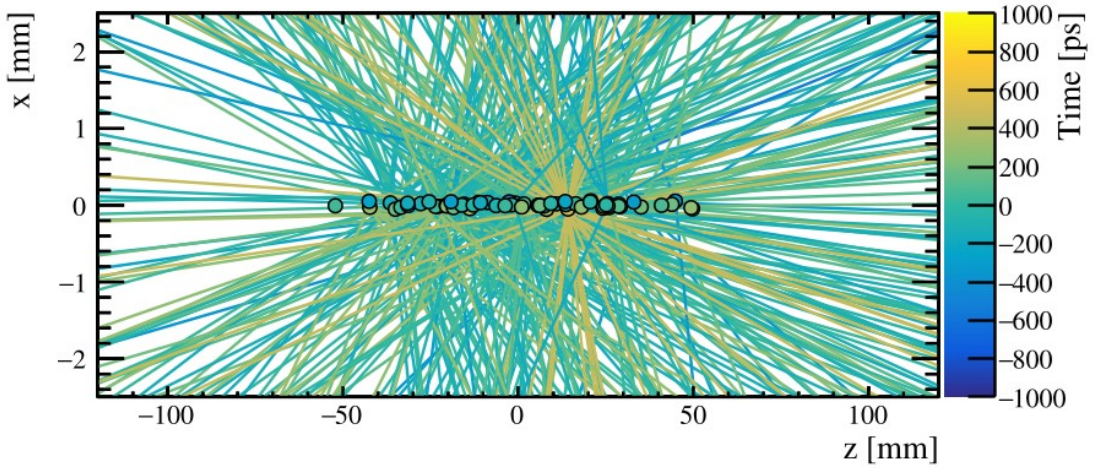
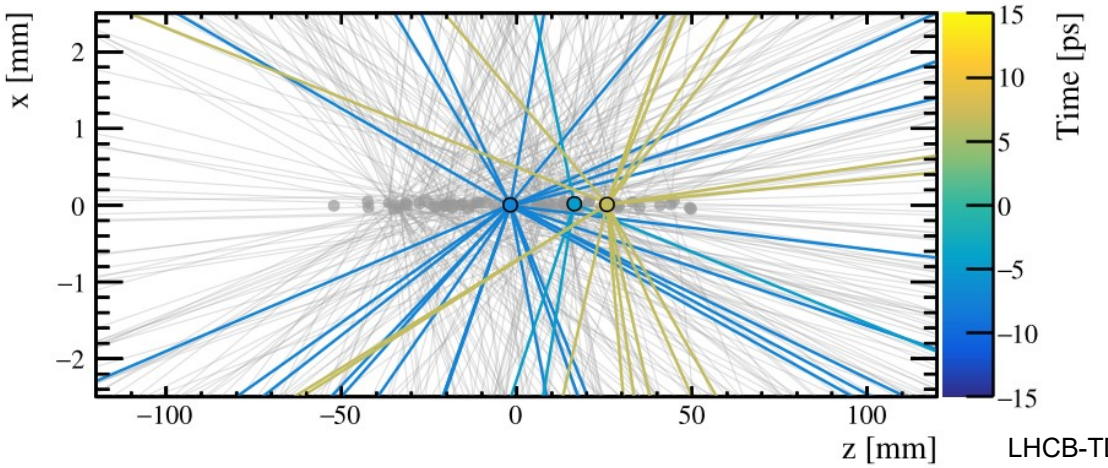
Velo Upgrade

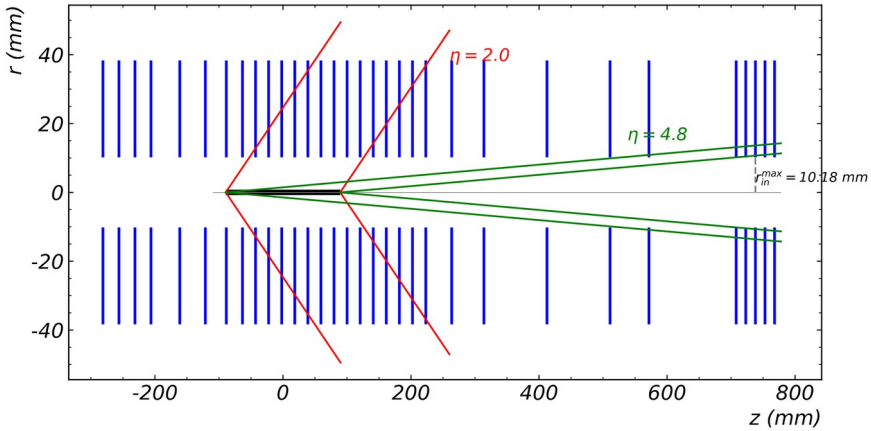




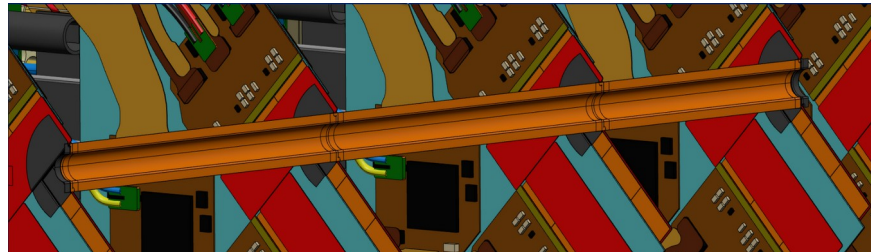
LHCB-TDR-026

Keep 10µm impact parameter resolution:

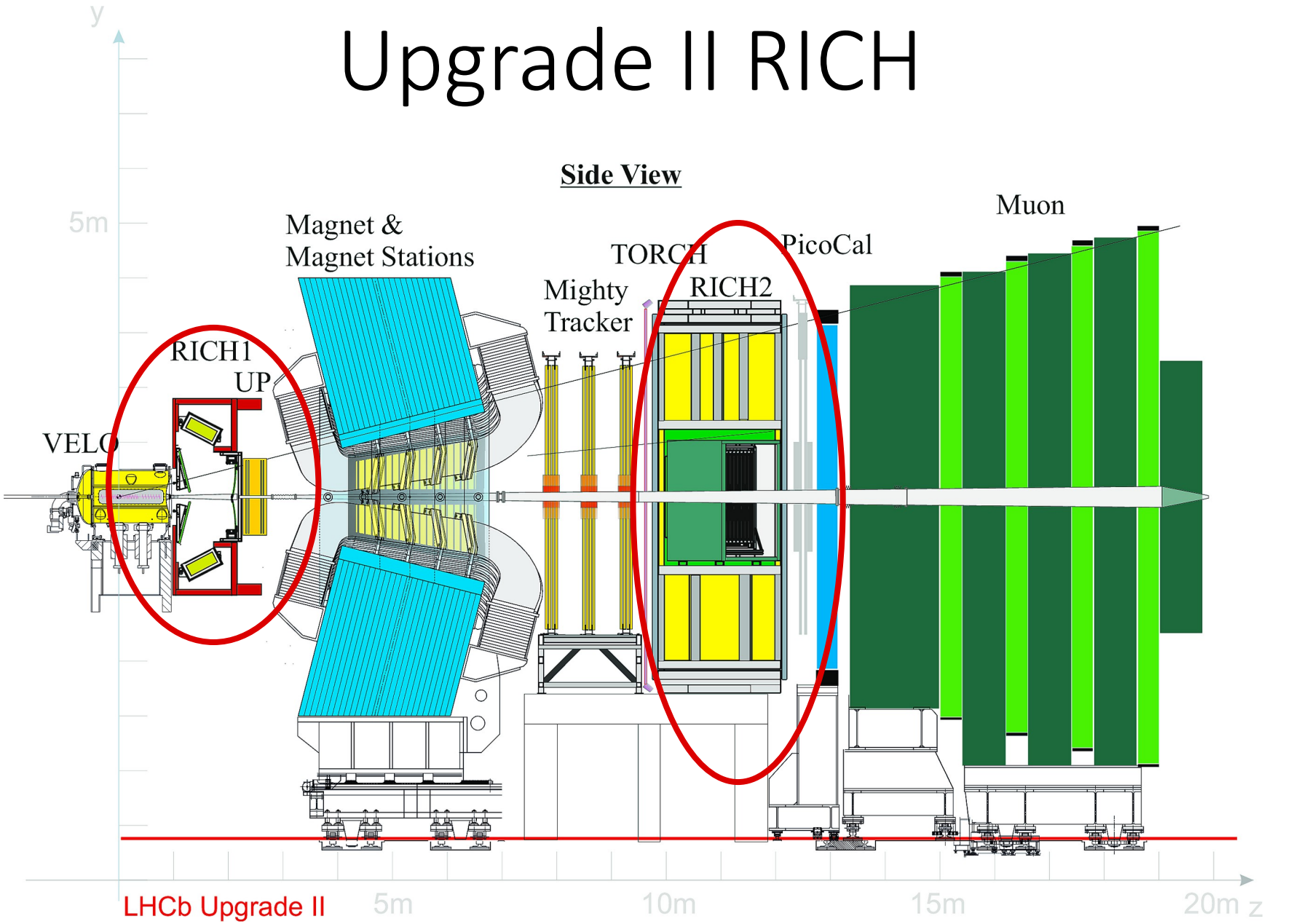
- 28 nm Hybrid ASIC
- 50 ps time timestamps per hit
- 50µm pixel pitch 3D sensor
- 170Gbit/s output for the hottest ASIC (direct to VTRx+)
- NIEL: 10^{16} 1MeV n_{eq}/cm^2
- TID: 400 MRad



- Reduced RF shield (75µm w.r.t. 250µm Al)
- CO_2 cooling with µ-channels or 3D printed Ti



Upgrade II RICH



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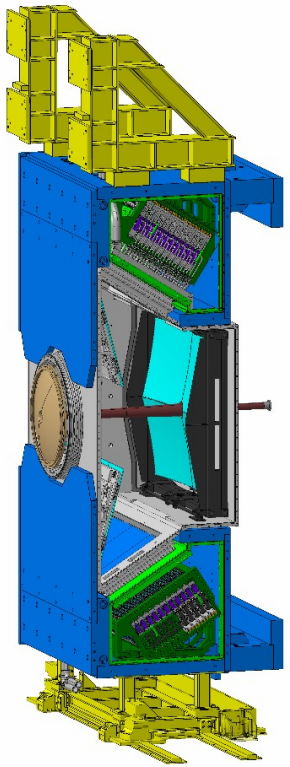
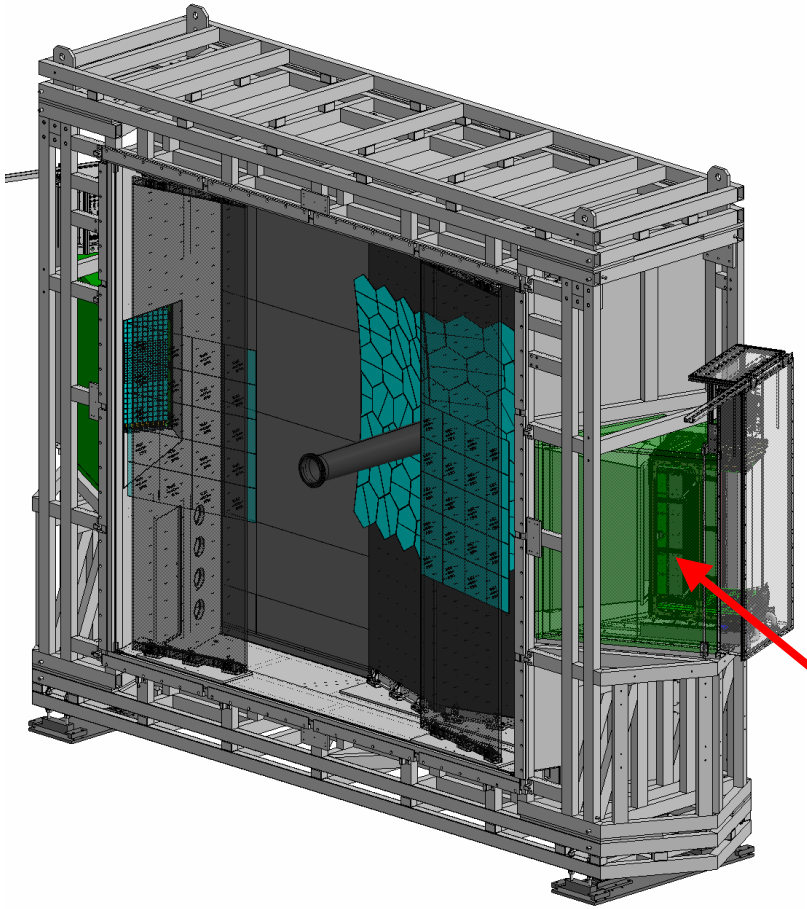
RICH Upgrade



RICH 1
3- 65 GeV PID



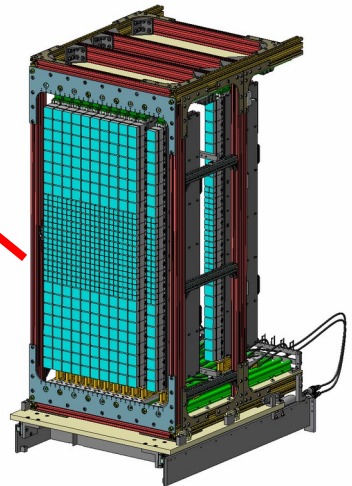
RICH 2
15-10 GeV PID

Main upgrade: Readout and Sensors

LHC Run 3	**Sensor** MAPMT		**FE ASIC** CLARO		**FPGA** Kintex 7	NDC	**Optical link** GBT Versatile Link	NDC	**Back-end** PCIe40
LHC Run 4	**Sensor** MAPMT		**FastRICH**			DC	**Optical link** lpGBT / VL+	DC	**Back-end** PCIe40(0)
HL-LHC Run 5	**Sensor** SiPM / MAPMT / MCP		**FastRICH**			DC	**Optical link** lpGBT / VL+	DC	**Back-end** PCIe400

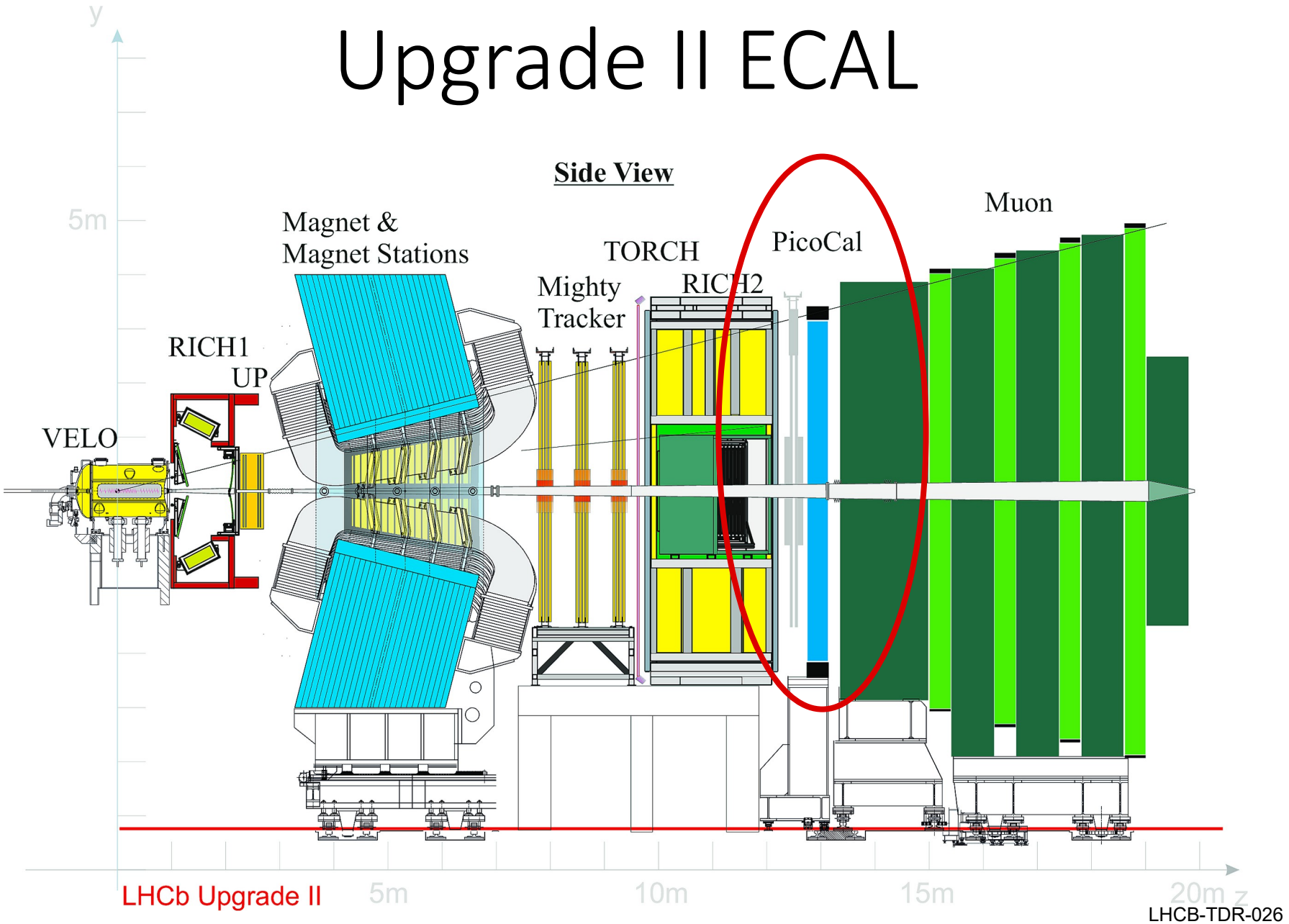
LHCB-TDR-026

- 100 ps photon resolution (FastRICH electronics)
- PMT → SiPM or MCP-PMT (higher granularity)



Planned Rich2 readout

Upgrade II ECAL



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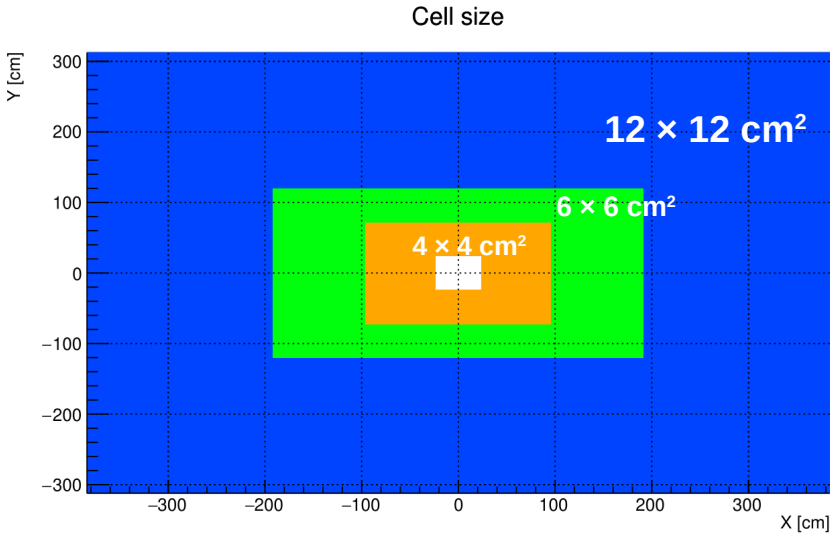
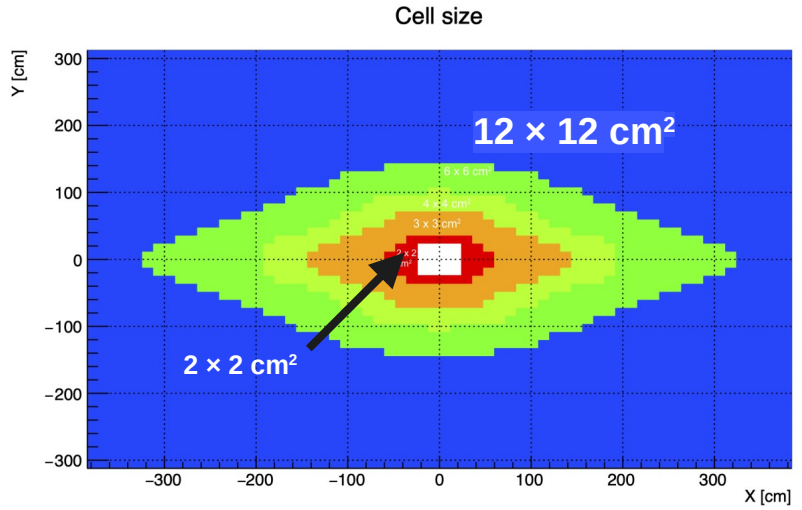
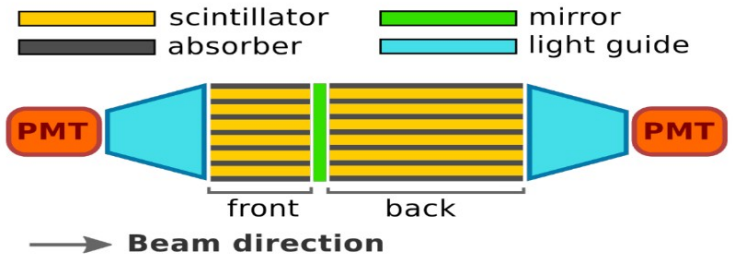
PicoCal

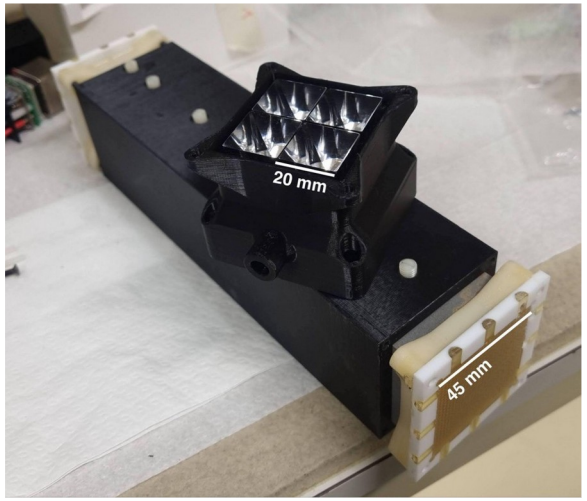
$$\sigma(E)/E = 10\%/\sqrt{E} \oplus 1\%$$

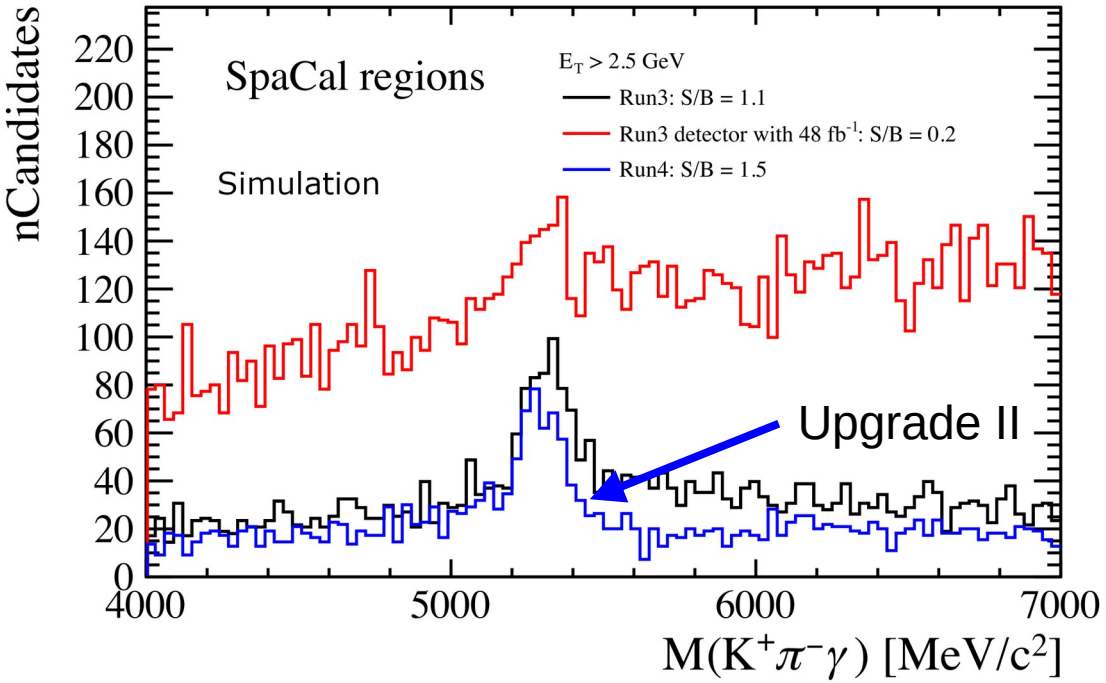
- O(10ps) timing
- Higher Granularity
- Spaghetti Calorimeter (SpaCal)
  - Absorber (inside to outside):
  - Tungsten
  - Gadolinium Aluminum Gallium Garnet
  - Lead



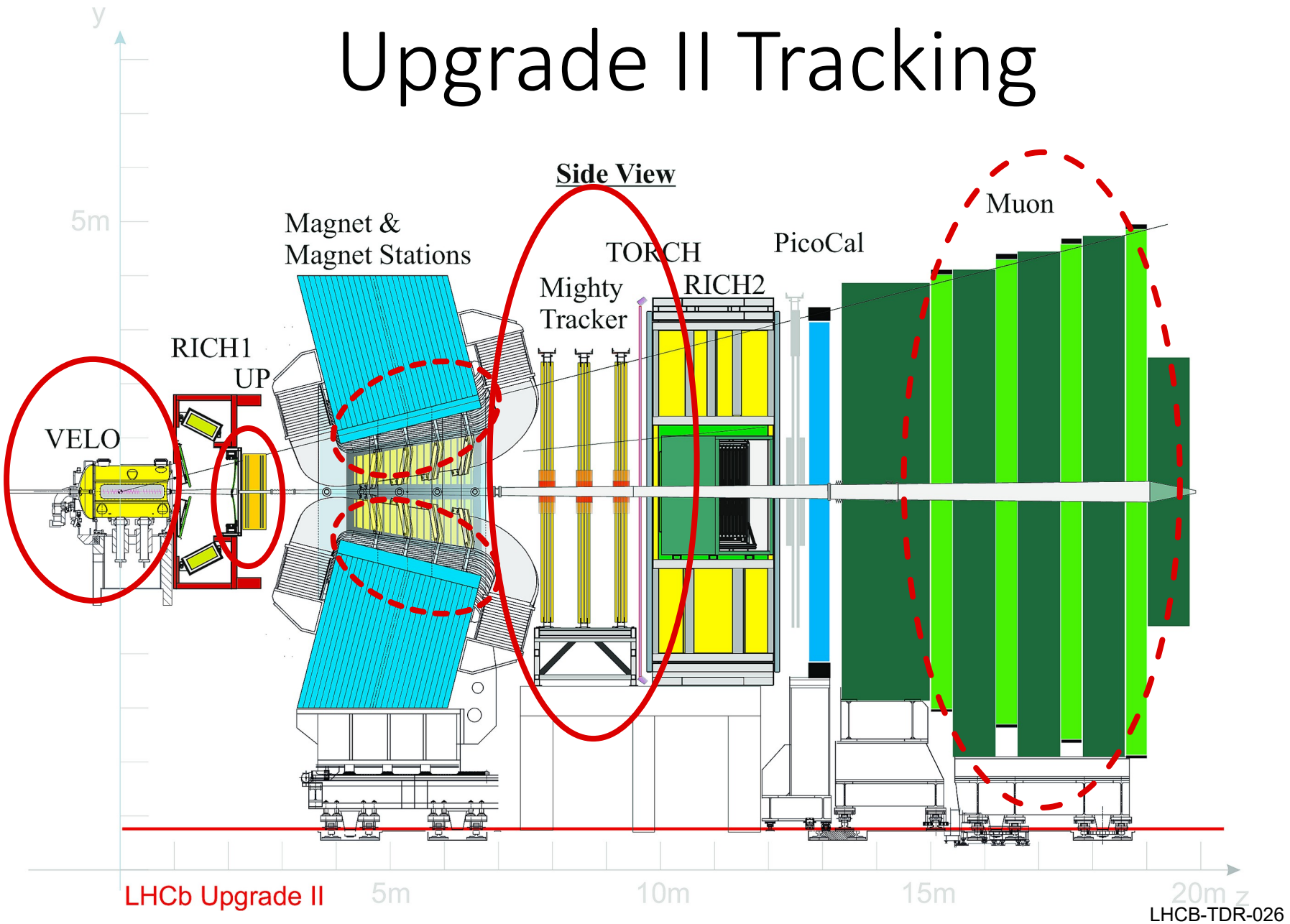








Upgrade II Tracking



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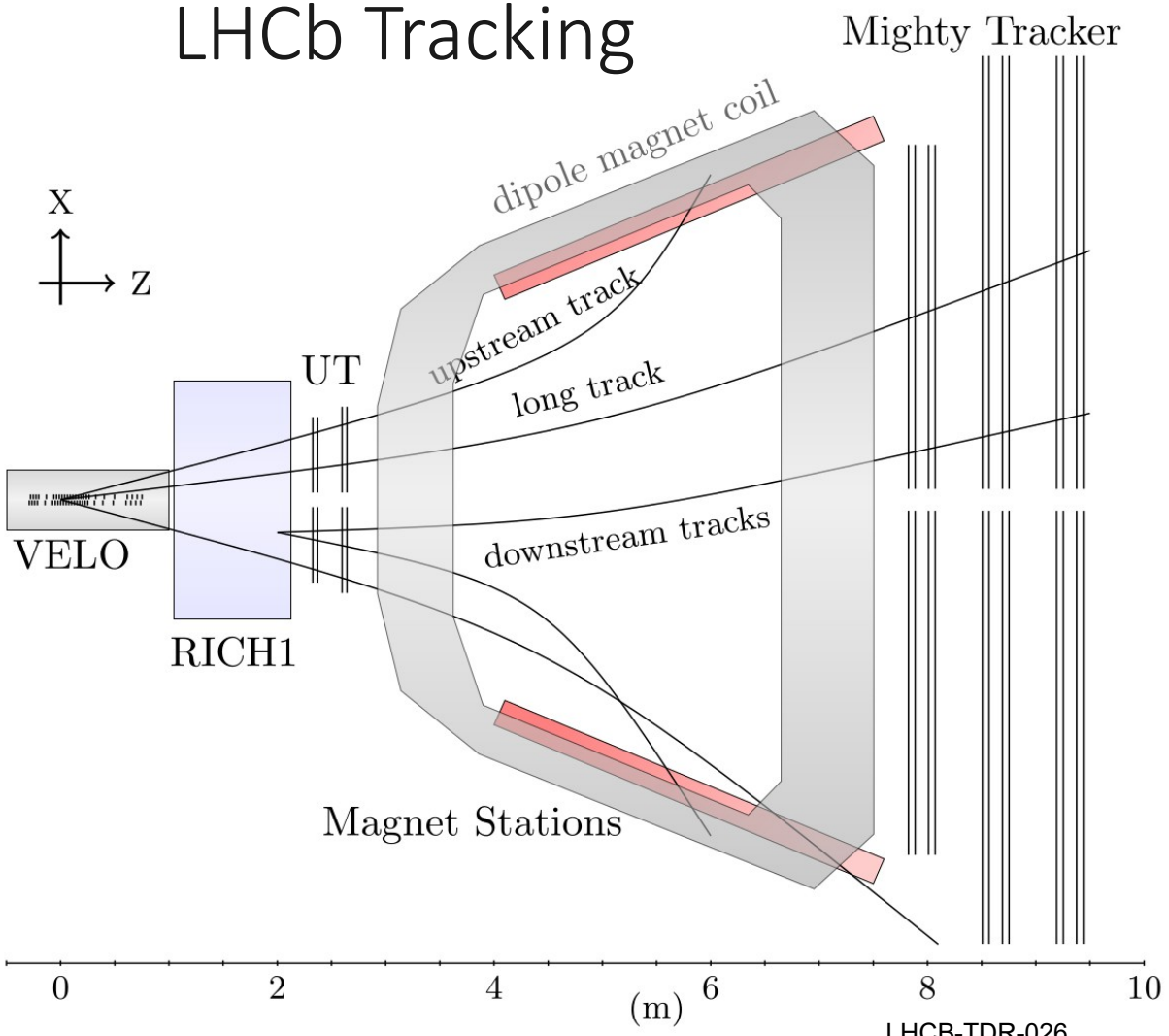
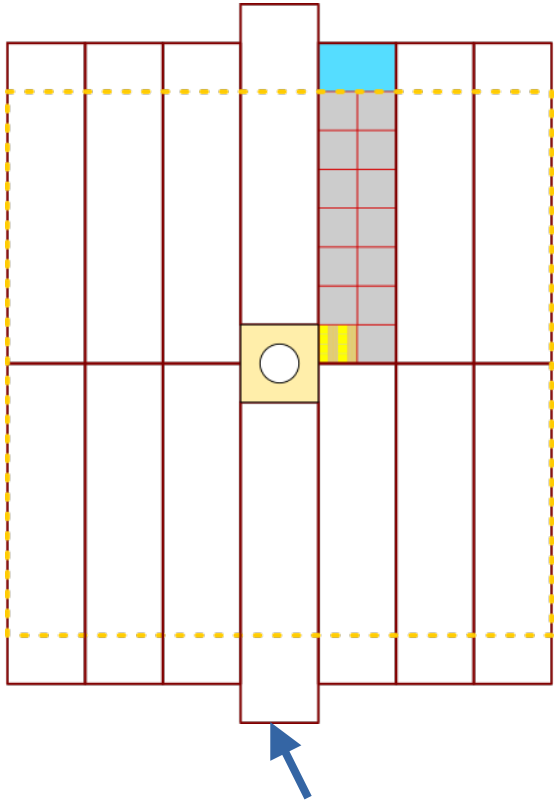
LHCb Tracking



LHCB-TDR-026

- reconstruction of hadron decays
  - many final state particles
  - high pointing precision
- the highest efficiency possible
  - ➔ many layers
- long lever arm
  - ➔ limited by the cavern
- **high resolution**
- **low material budget**

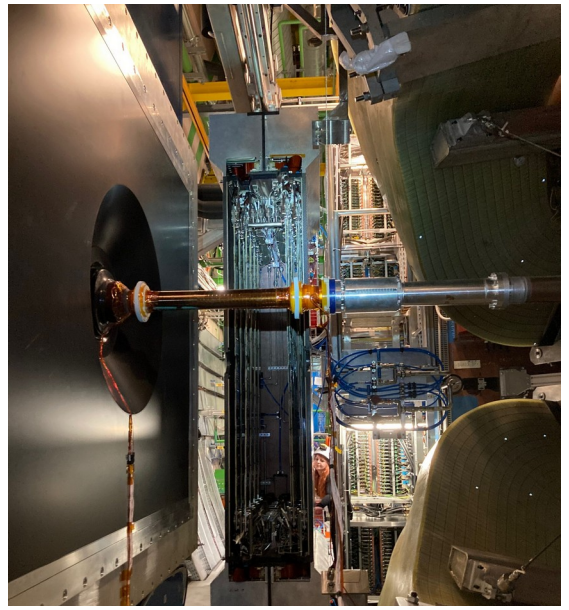
Upstream Pixel

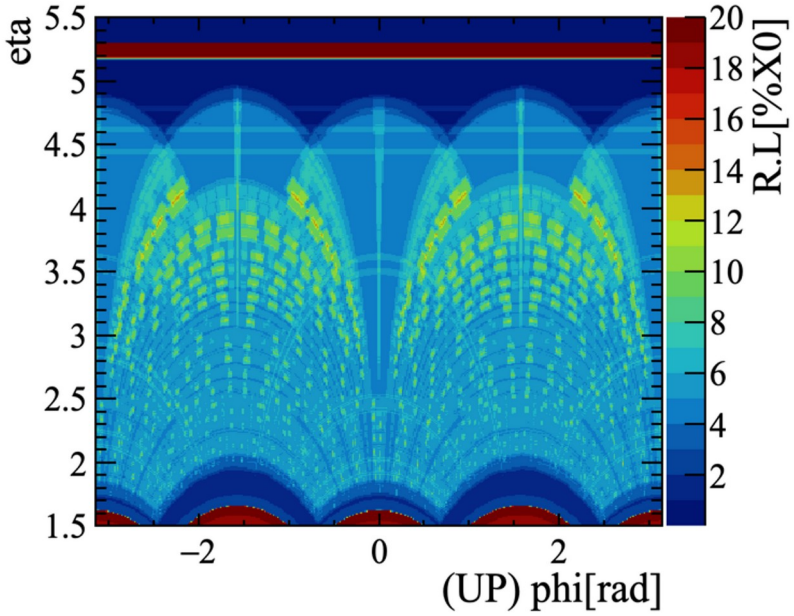


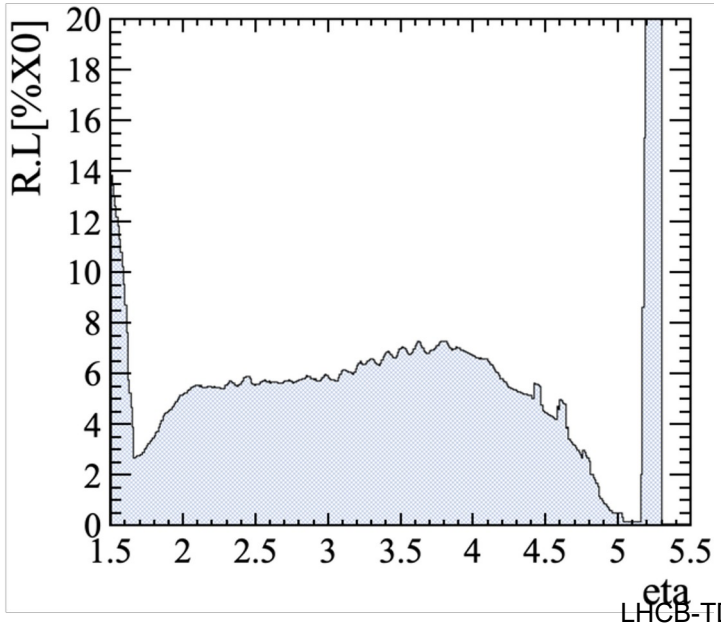
See why this design later

- 4 Layers
- Monolithic Sensors
- 9 m^2 active area
- 74 (34) MHz/cm^2 at 4cm (6cm) from beampipe
- NIEL: $3 \cdot 10^{15}$ 1MeV n_{eq}/cm^2
- TID: 240 MRad

Planned to use the same sensor as Mighty-Pixel and probably similar module design







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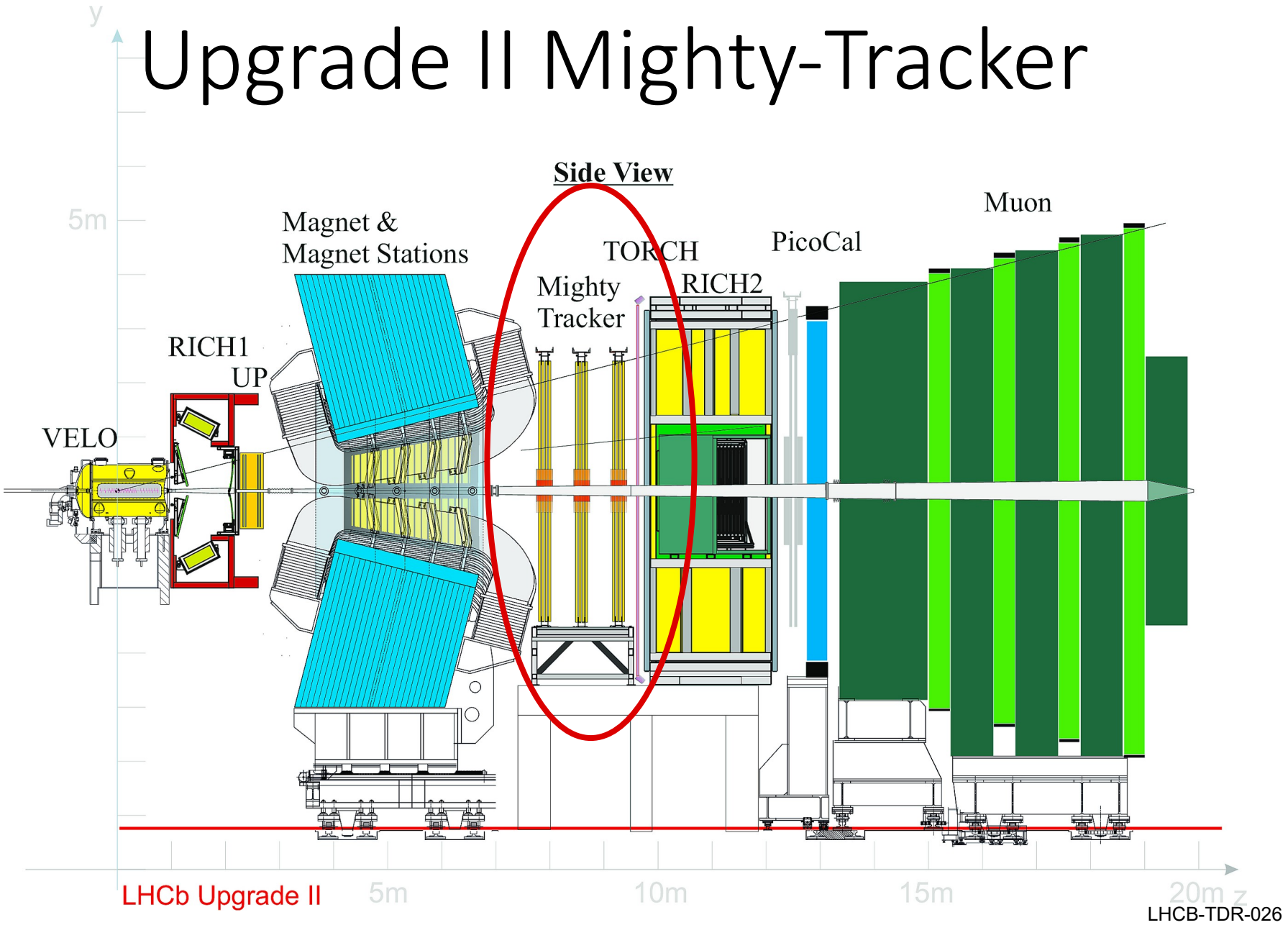
Upgrade II Mighty-Tracker

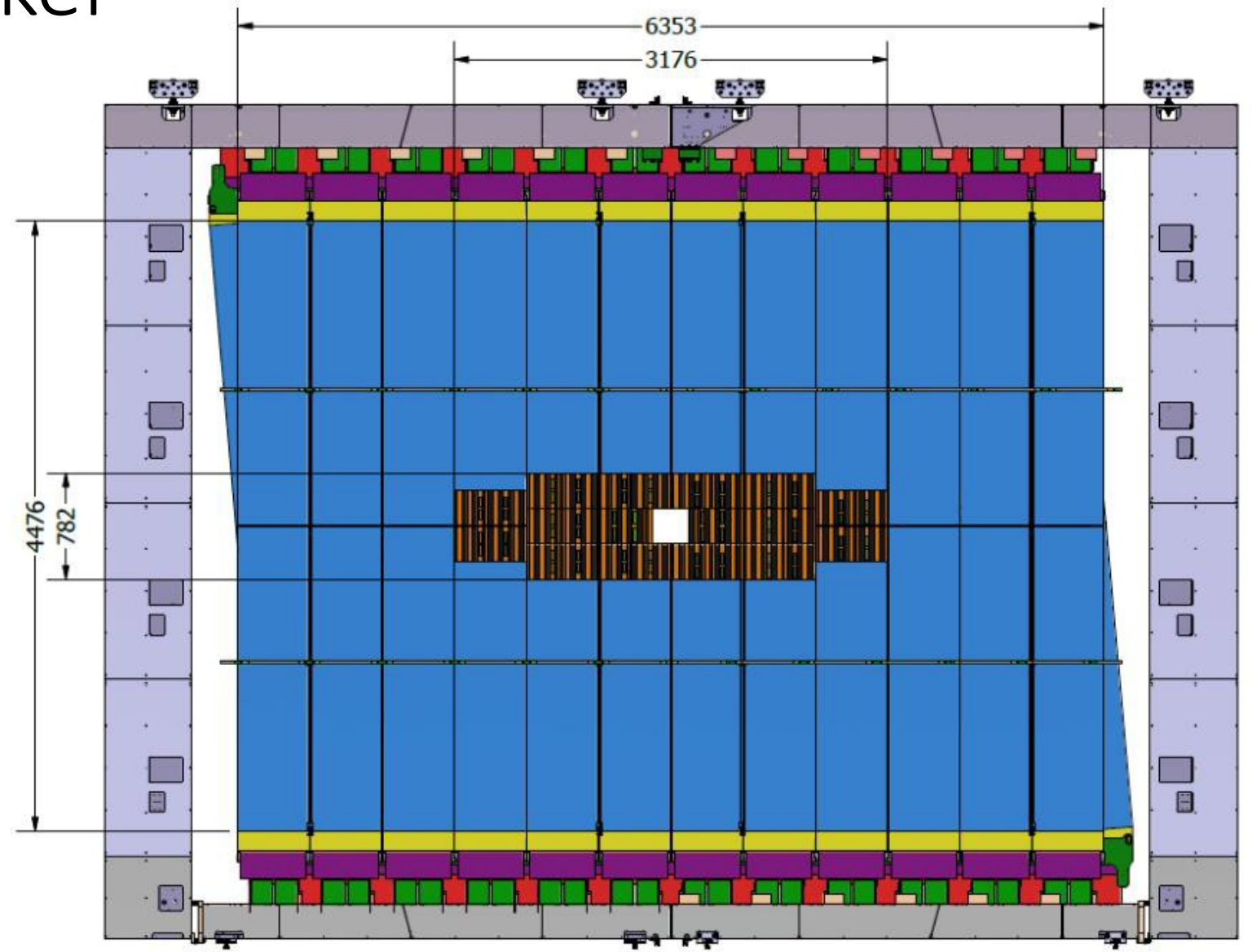


LHCB-TDR-026

Mighty-Tracker
(thank you chatGBT)

The Mighty Tracker

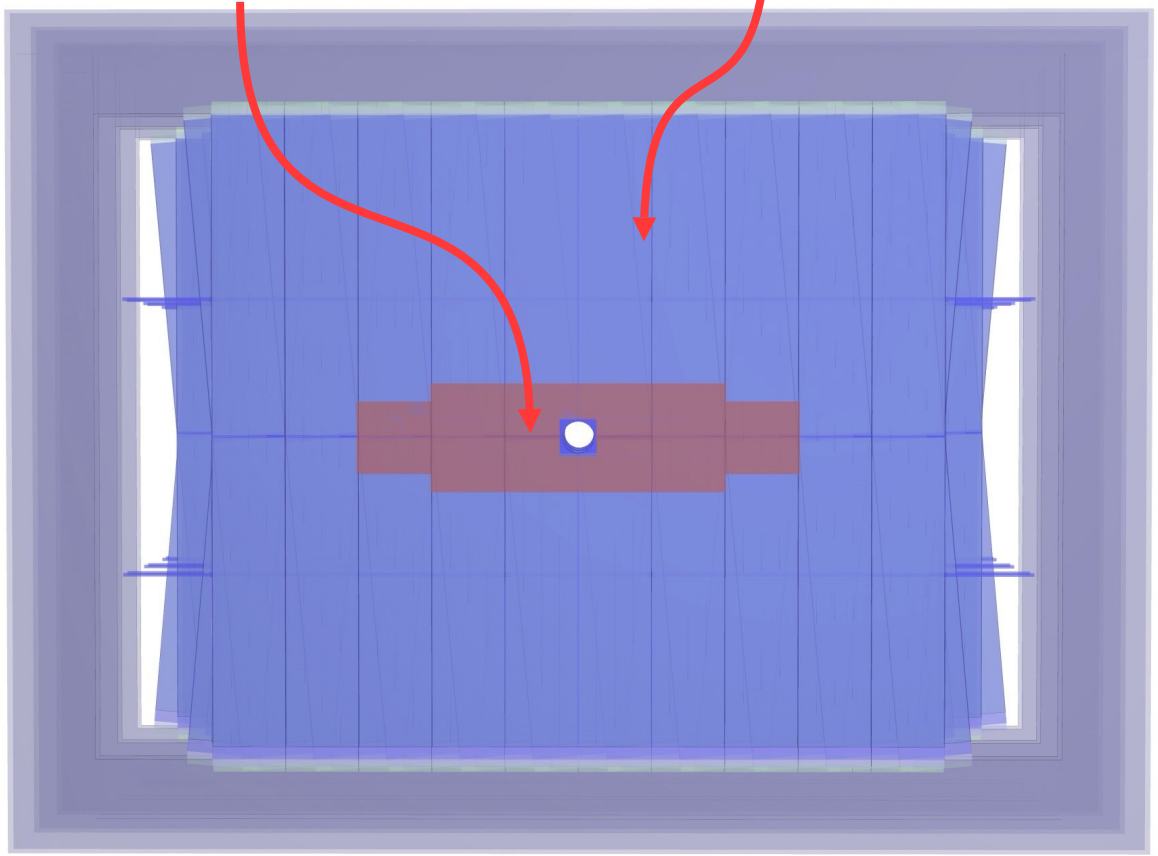
- Mighty SciFi tracker for the outside 12 layers in 3 stations (320m²)
- Mighty Pixel for the high occupancy regions in 6 layers (12.6m²)



Mighty-Tracker

Mighty-Pixel

Mighty-SciFi



Problems:

- High occupancy
- High radiation environment
- Tracking efficiency

Solution:

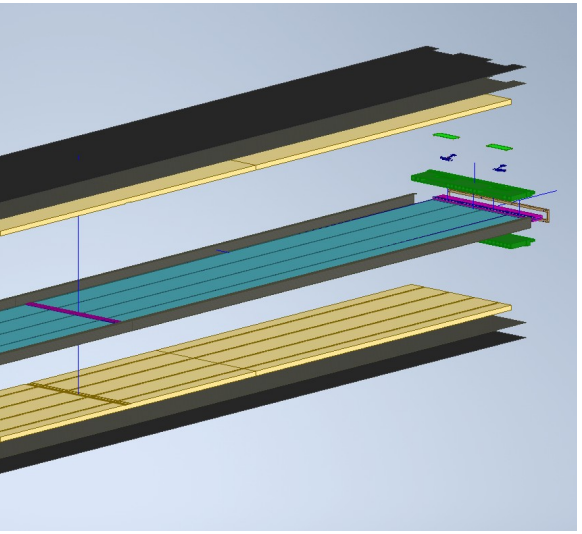
- Cyogenic cooled SciFi
- HV-CMOS MAPS in the central part
- 6 Layers in 3 Stations
- 13 m^2 area
- HV bias 100-200V
- High granularity (50 x 165 μm^2)
- **Low power < 150mW/cm^2**
- **High timing resolution < 3ns**
- Radiation Hard > $3 \cdot 10^{14}$ n_{eq}/cm^2
- **Low material budget <2% of total radiation length**
- **Cheap**

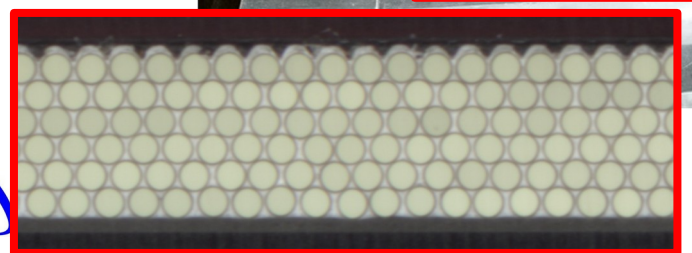
Upgrade 2 Fiber

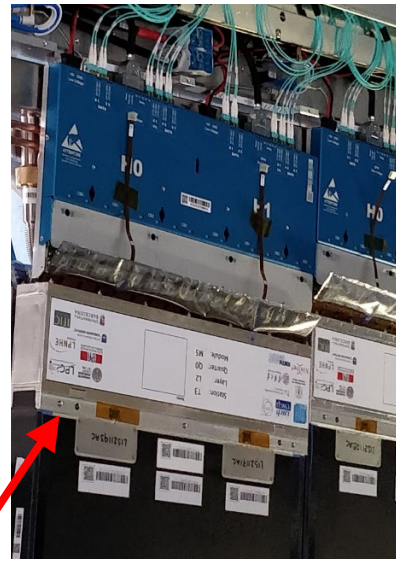
SciFi2 the return of the Light

SciFi Working Principle (Current SciFi)

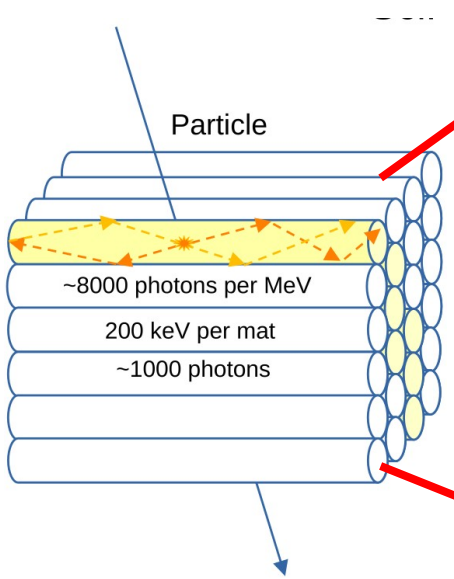
Module:
Long fibers
Minimal support material

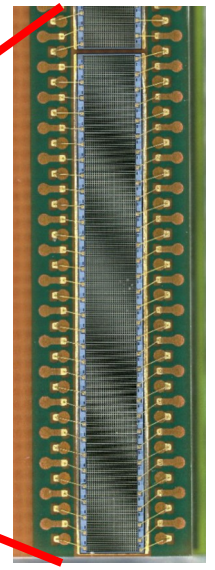




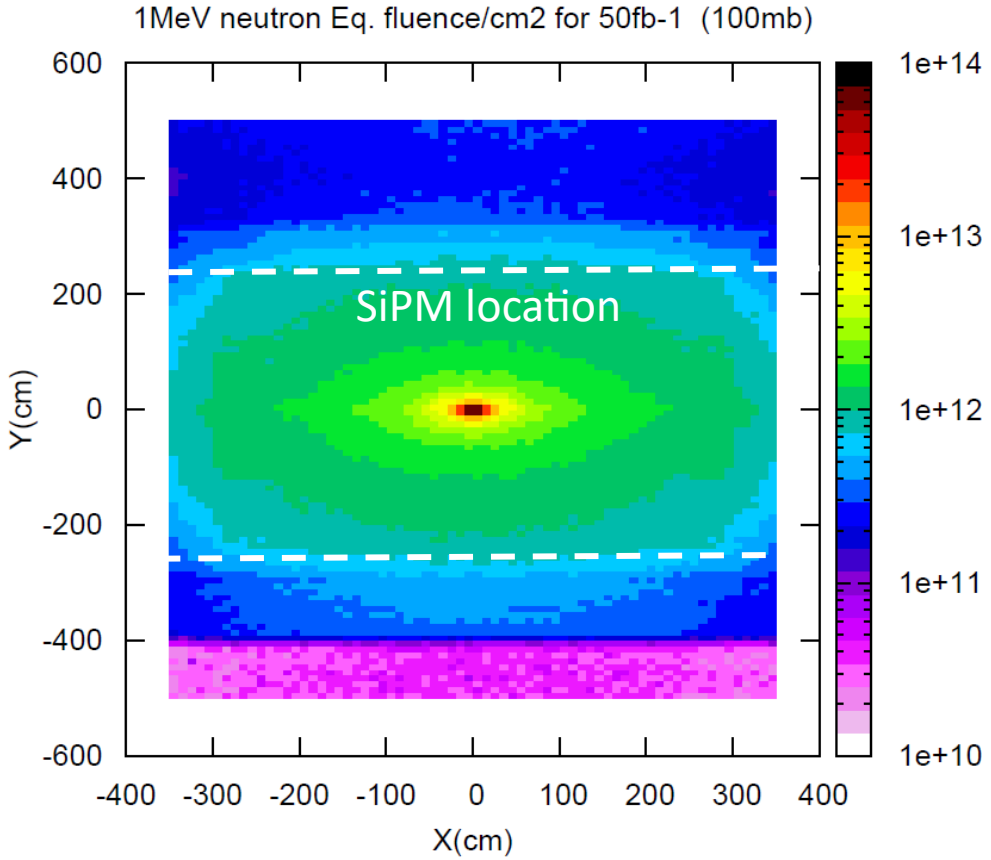


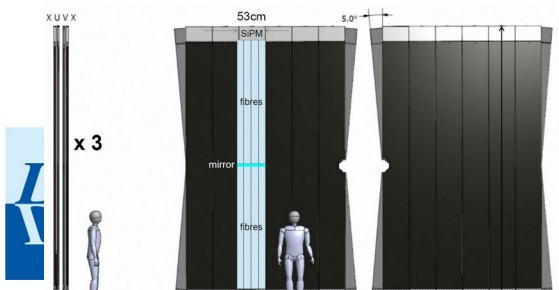
- Very successful application to instrument a large area
- Low material budget ($X/X_0 \leq 1\%$ per detector layer)
- XUVX layout (±5° for U and V)
- Main complexity to produce homogeneous fiber mats
- 70 µm resolution





SiPM Challenges



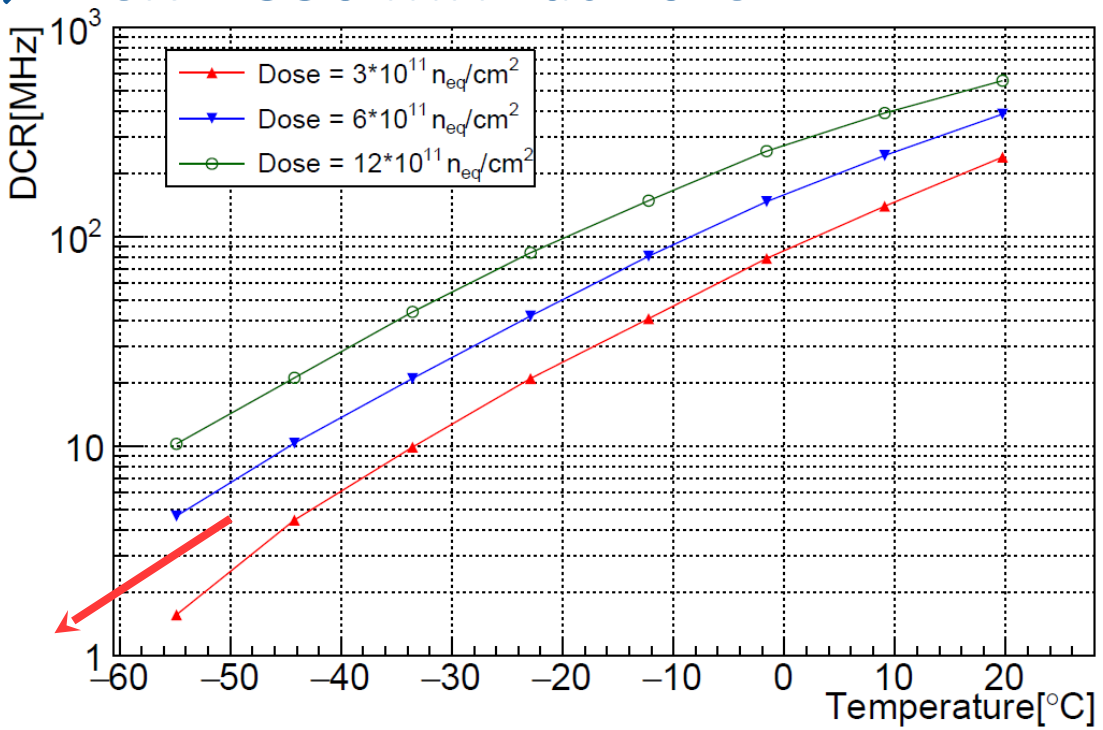


Unirradiated SiPM:

Dark Count Rate (DCR) ~ 0.04MHz

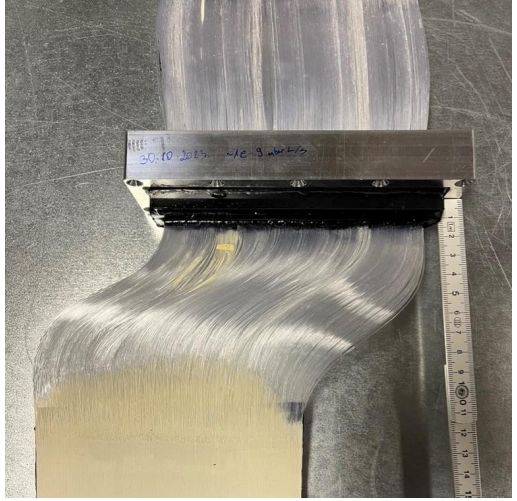
Expect $6 \cdot 10^{11}$ n_{eq}/cm^2

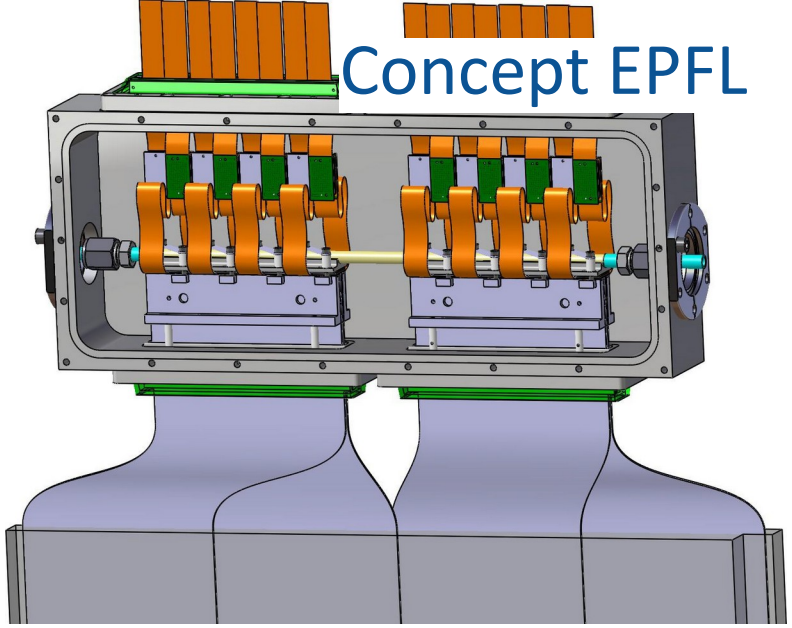
→ DCR ~ 550 MHz at 20°C



You expect ~ ½ DCR per 7K →Cryogenic temperatures

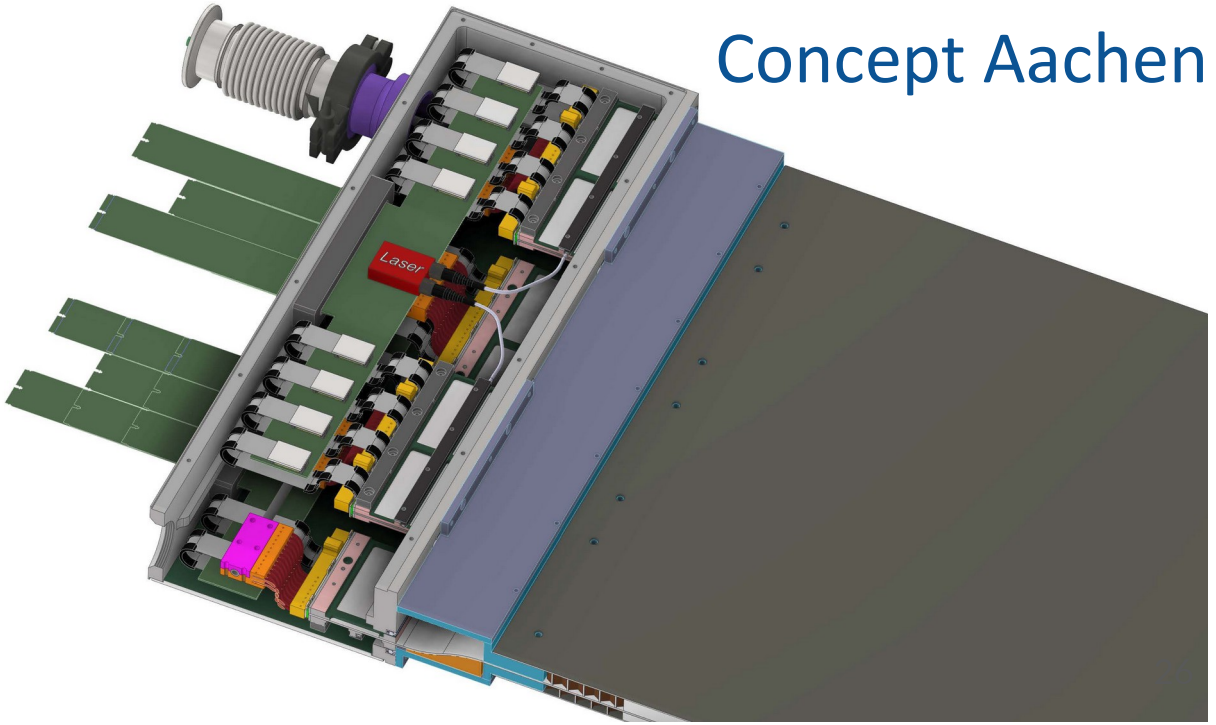
Cryogenic SciFi





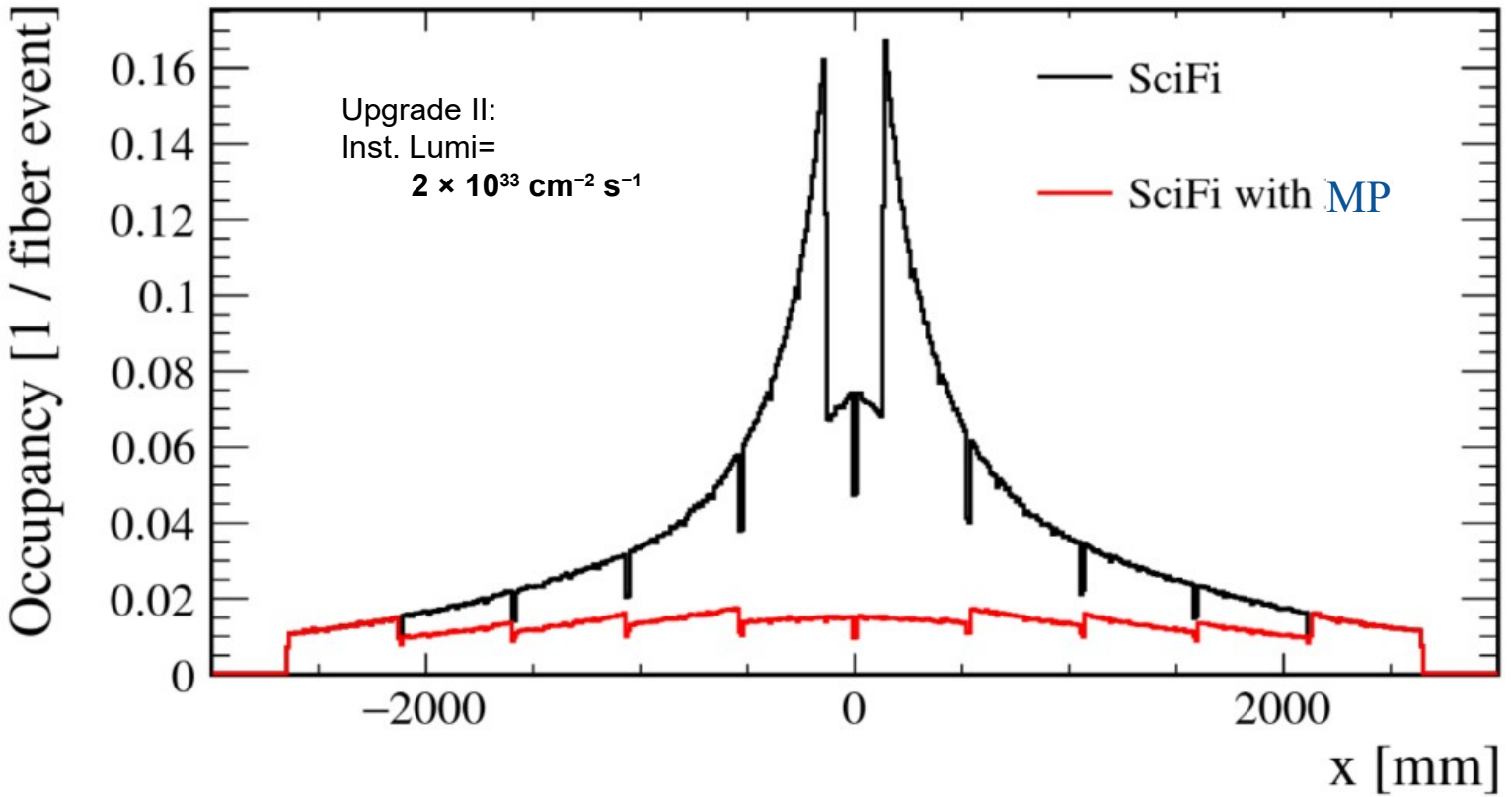
Concept EPFL

- Goal is a “noise free” detector
- Challenges: cryogenic cooling for a larger tracking detector
- Fiber bending at the end
- Thermal insulation of the coldbox
- Use 2-phase N_2
- About 2-2.8kW cooling power needed
- First test show great promise



Concept Aachen

Why do we need the Mighty-Tracker



LHCB-TDR-023

The number of hits/fiber/event is too high to allow efficient tracking

Need to have a higher granularity in the central region.

Mighty Pixel

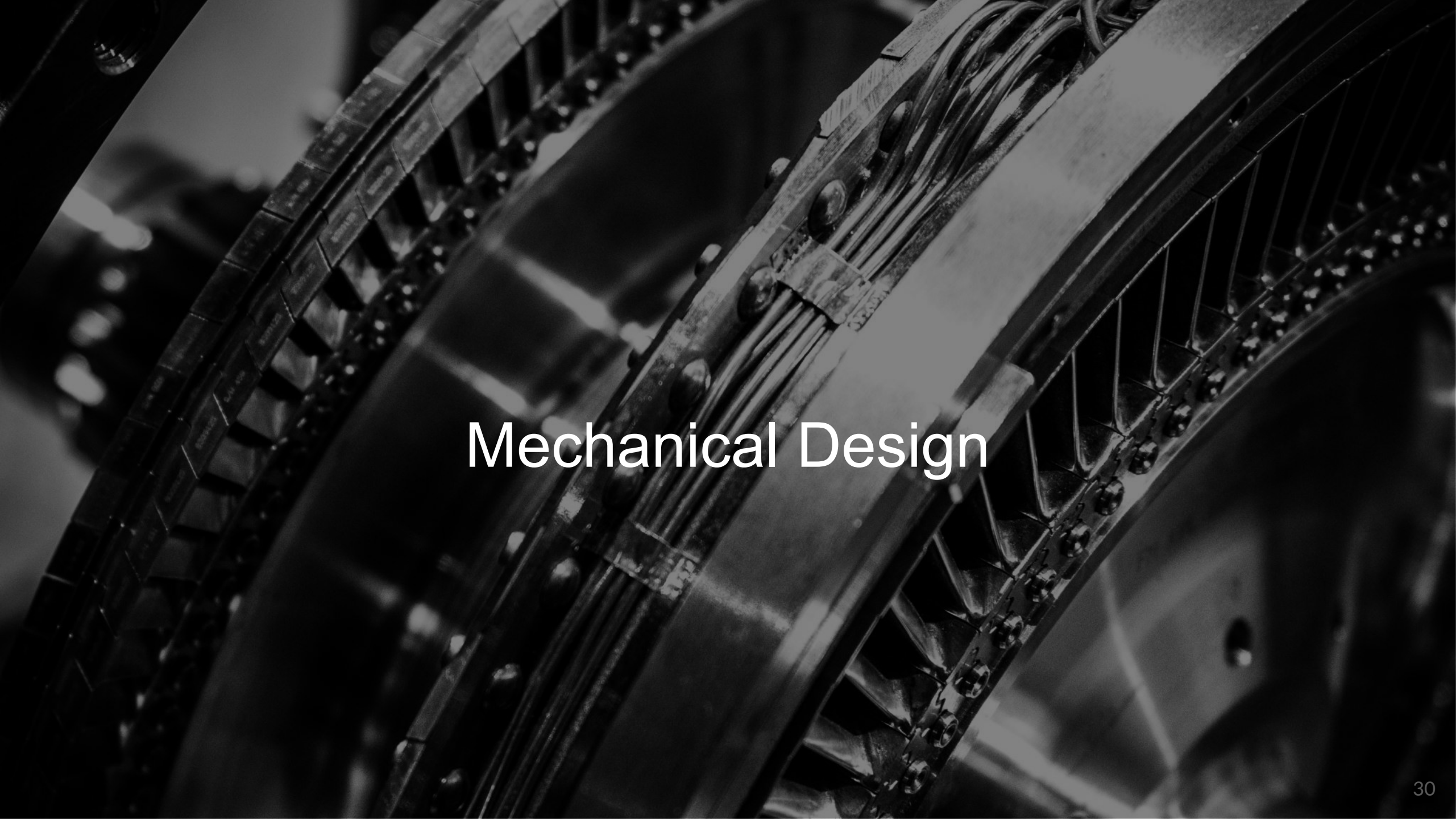
Large Scale CMOS Pixel Detector

HV-CMOS

- One of the main drivers of the project is the size of the silicon area
- MAPS chips are limited to ~2x2 cm^2 (foundry)
- The most critical points are:
  - In Time **Efficiency**
  - **Power** Consumption
  - **Radiation** Tolerance

Design Specifications:	
In-time efficiency	> 99% within 25 ns window
Timing resolution	~ 3 ns
Power consumption	< 150 mW/cm^2
Pixel size	< 100 µm x 300 µm
Radiation tolerance	3 x 10^{14} 1 MeV n_{eq}/cm^2
Data transmission	4 links of 1.28 Gb/s each
Compatibility with the LHCb readout system	

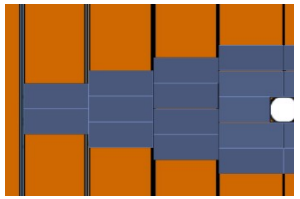
LHCb-INT-2019-007, 2019



Mechanical Design

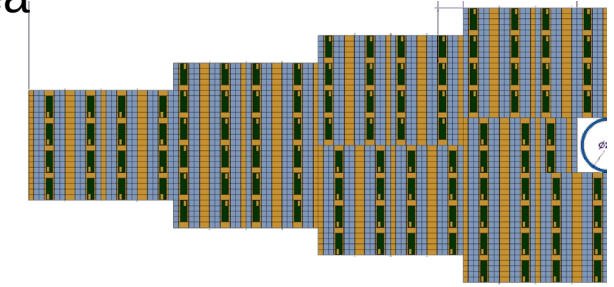
A Short History of the Mighty

18m^2
Some Silicon area



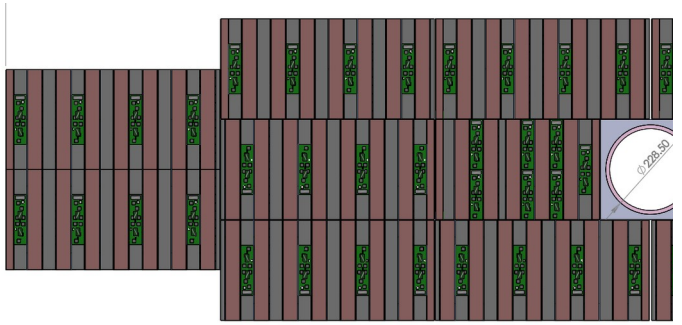
Fully integrate silicon into the fiber planes

18m^2
FTDR
detailed ideas for readout

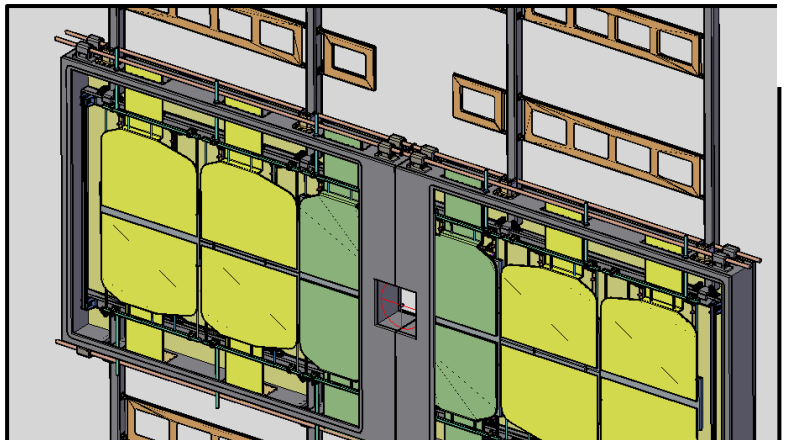


Separate silicon and fibers
Ohh and we have to be cold

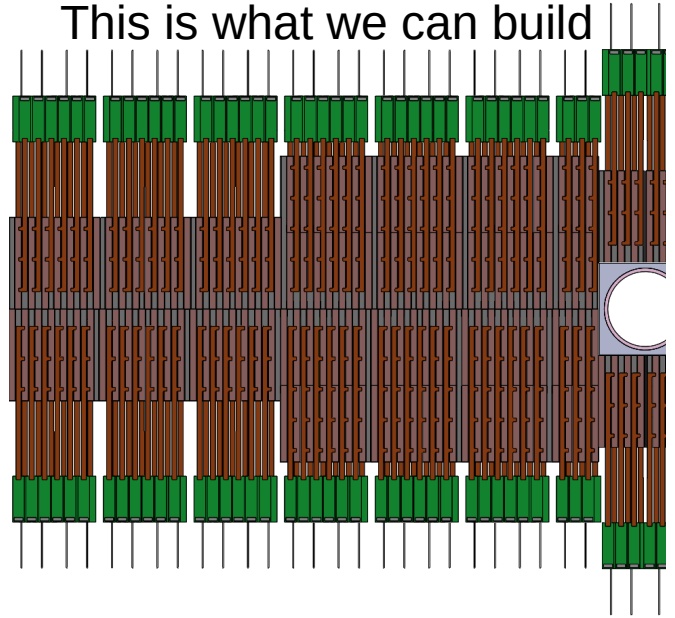
13m^2
Scoping document
This is what we can afford



Support structures are designed and clear budget



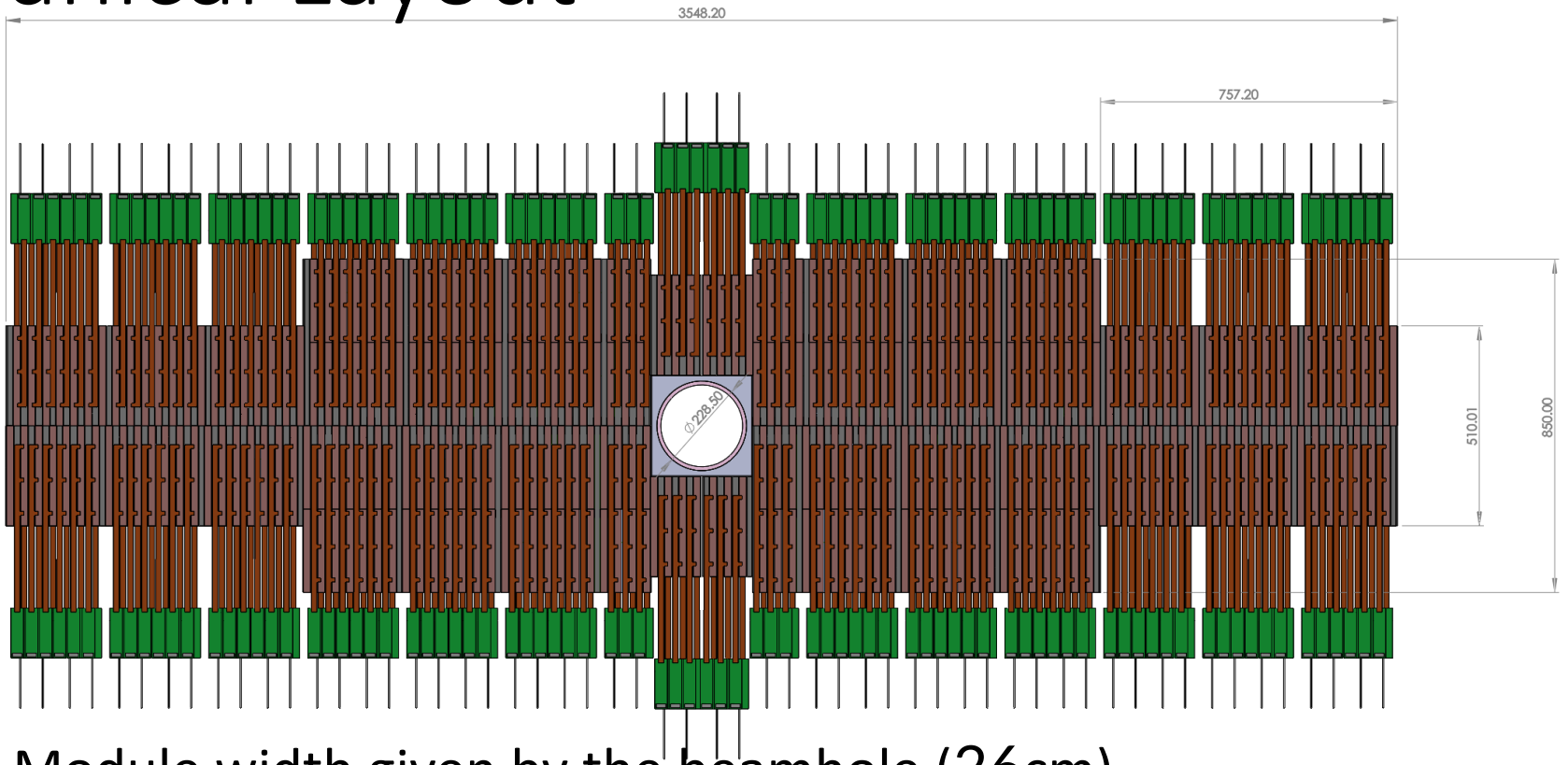
14m^2
Current design
This is what we can build



Cooling solutions and auxiliary electronics are realistic

Mechanical Layout

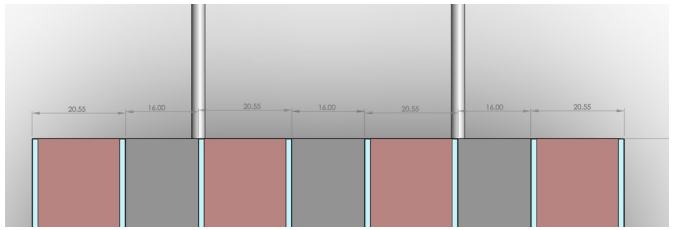
One Layer 2.4m²
2 Layers per station
6 Layers in total

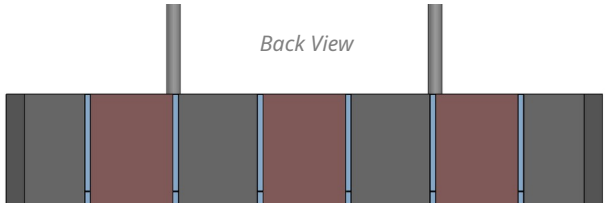


- Module width given by the beamhole (26cm)
- Shape follows the highest acceptable occupancy in the fiber region
- Readout is moved out as far as possible from the hottest region

Modules

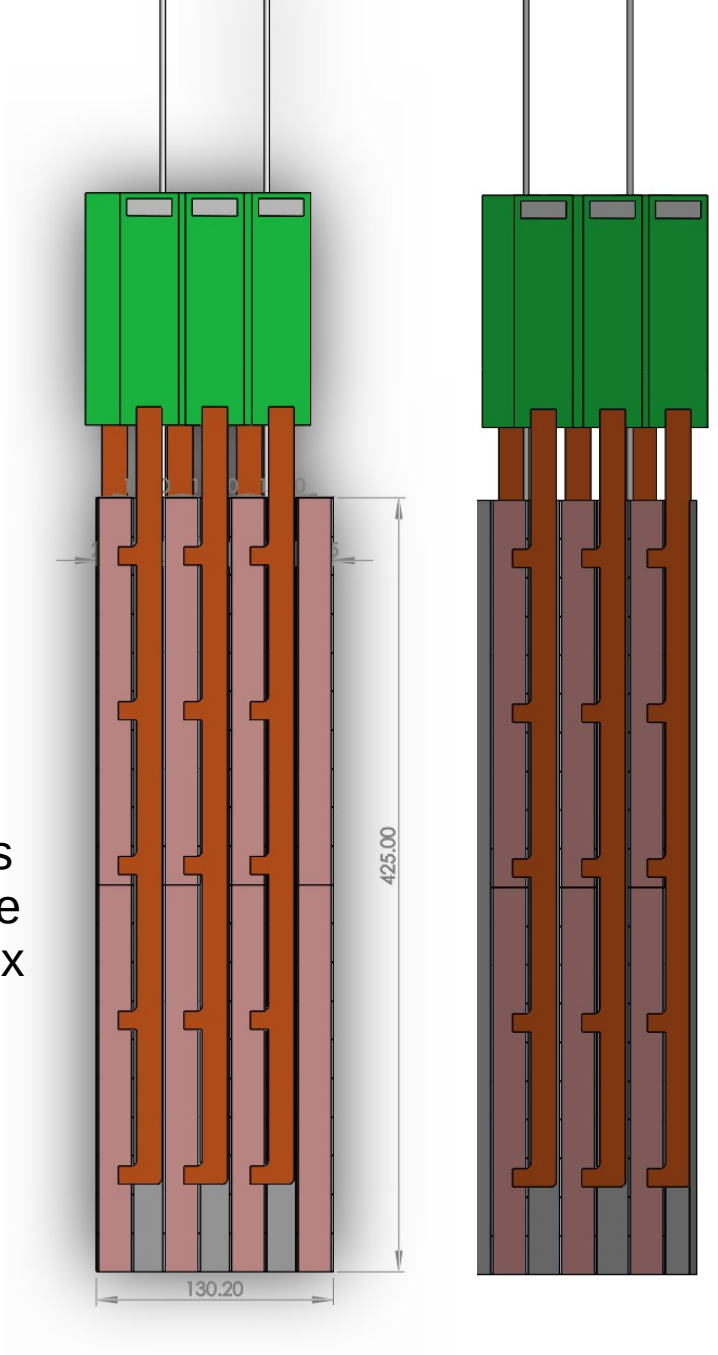
Front View





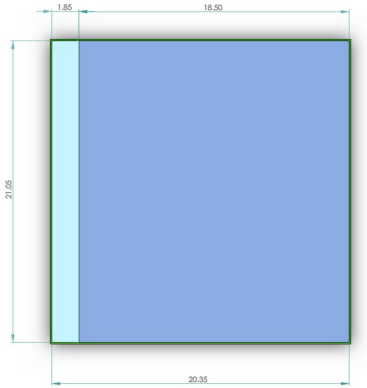
Back View

- Front and Back have 4 and 3 rows
- Active area ASIC is assumed to be ~18.6mm → fully covered area in x
- Gap in y ~200µm per sensor (active area)
- T – shaped cutout
- Various readout board positions thinkable



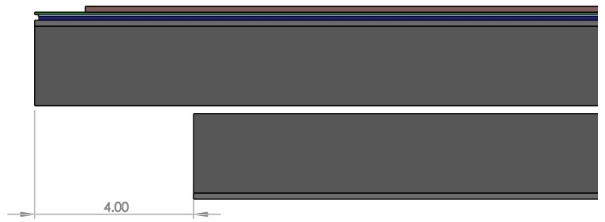
Front View

Back View

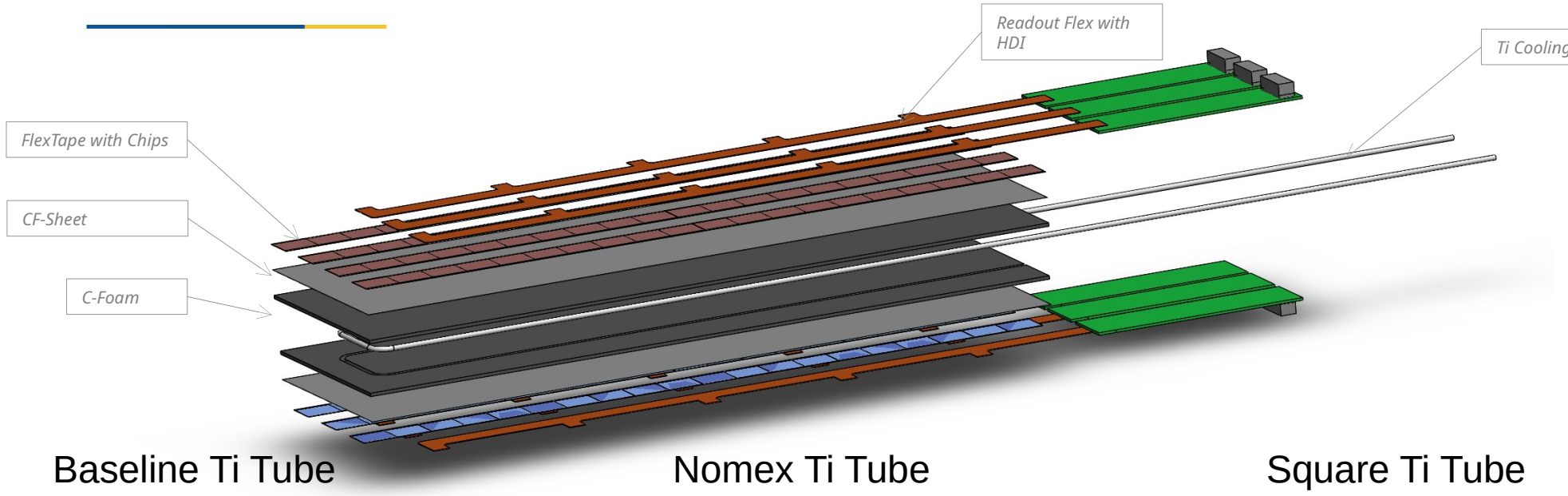


** Footprint: +200 µm*

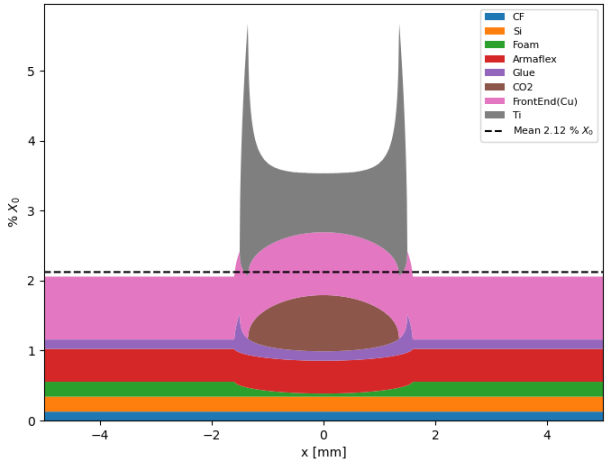
Cut-Out for the module interconnection (both edges)



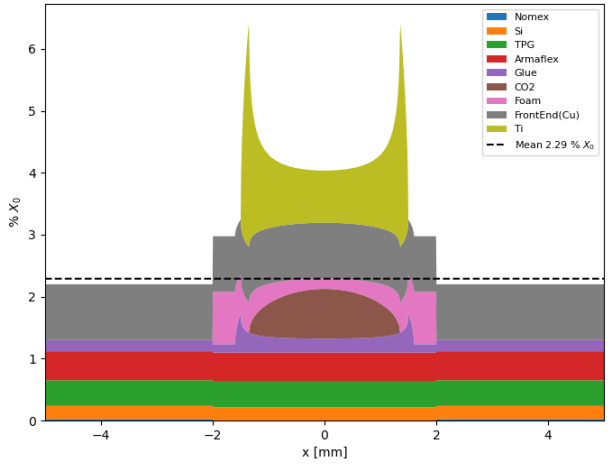
Module Stack



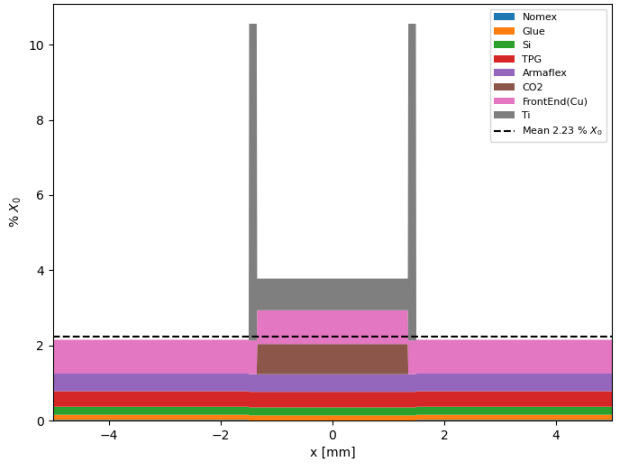
Baseline Ti Tube
w. Foam



Nomex Ti Tube
No Foam

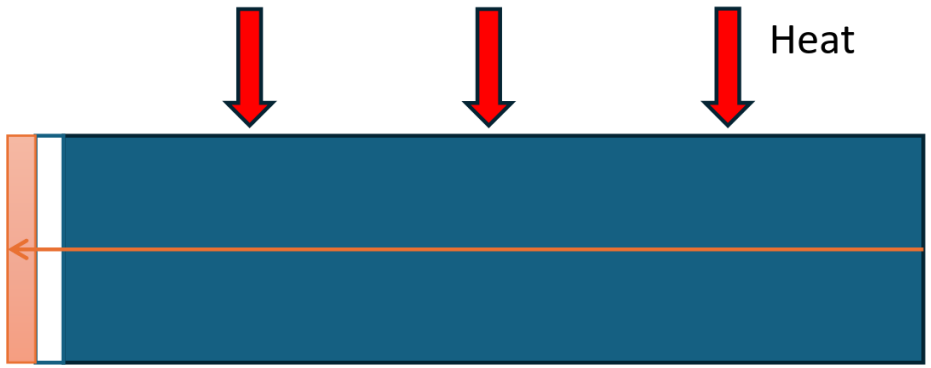


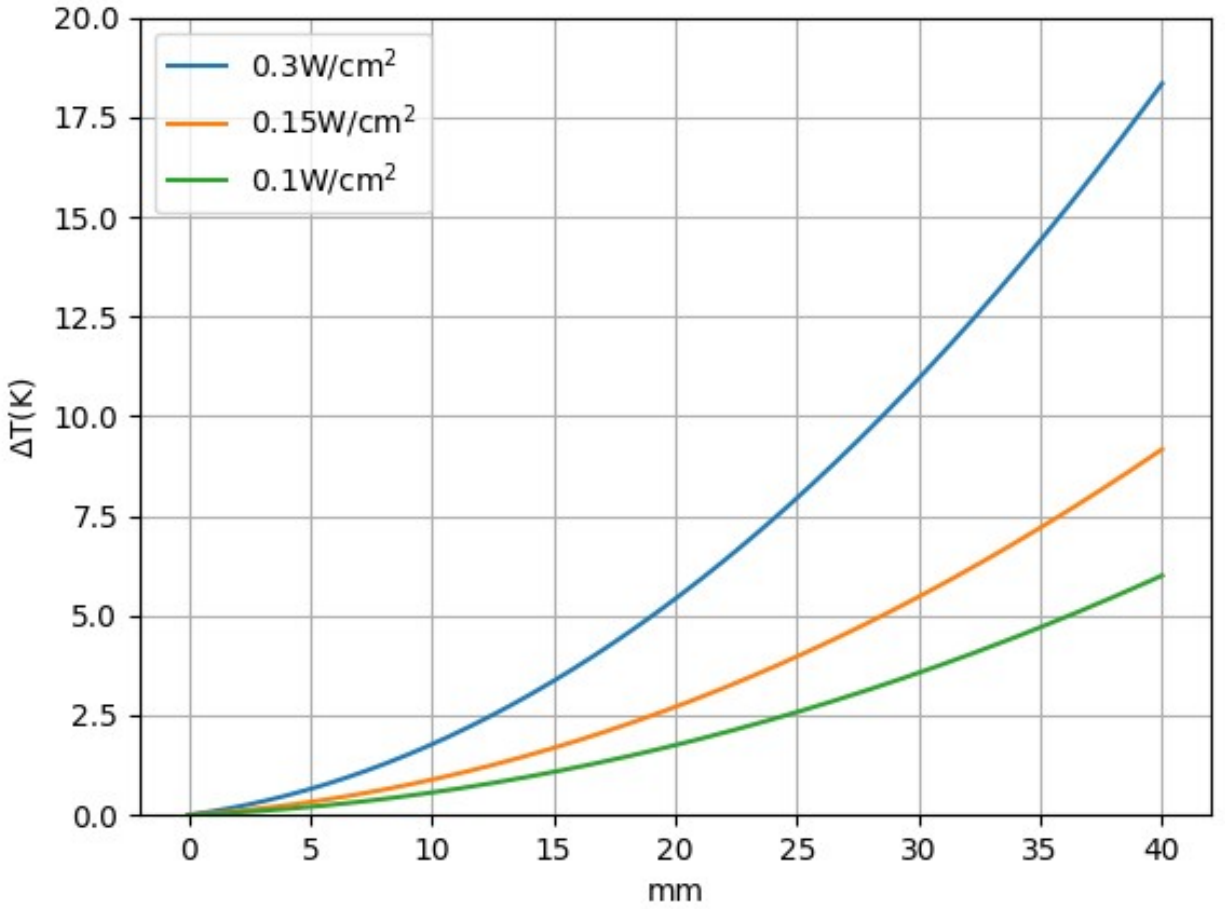
Square Ti Tube
No Foam

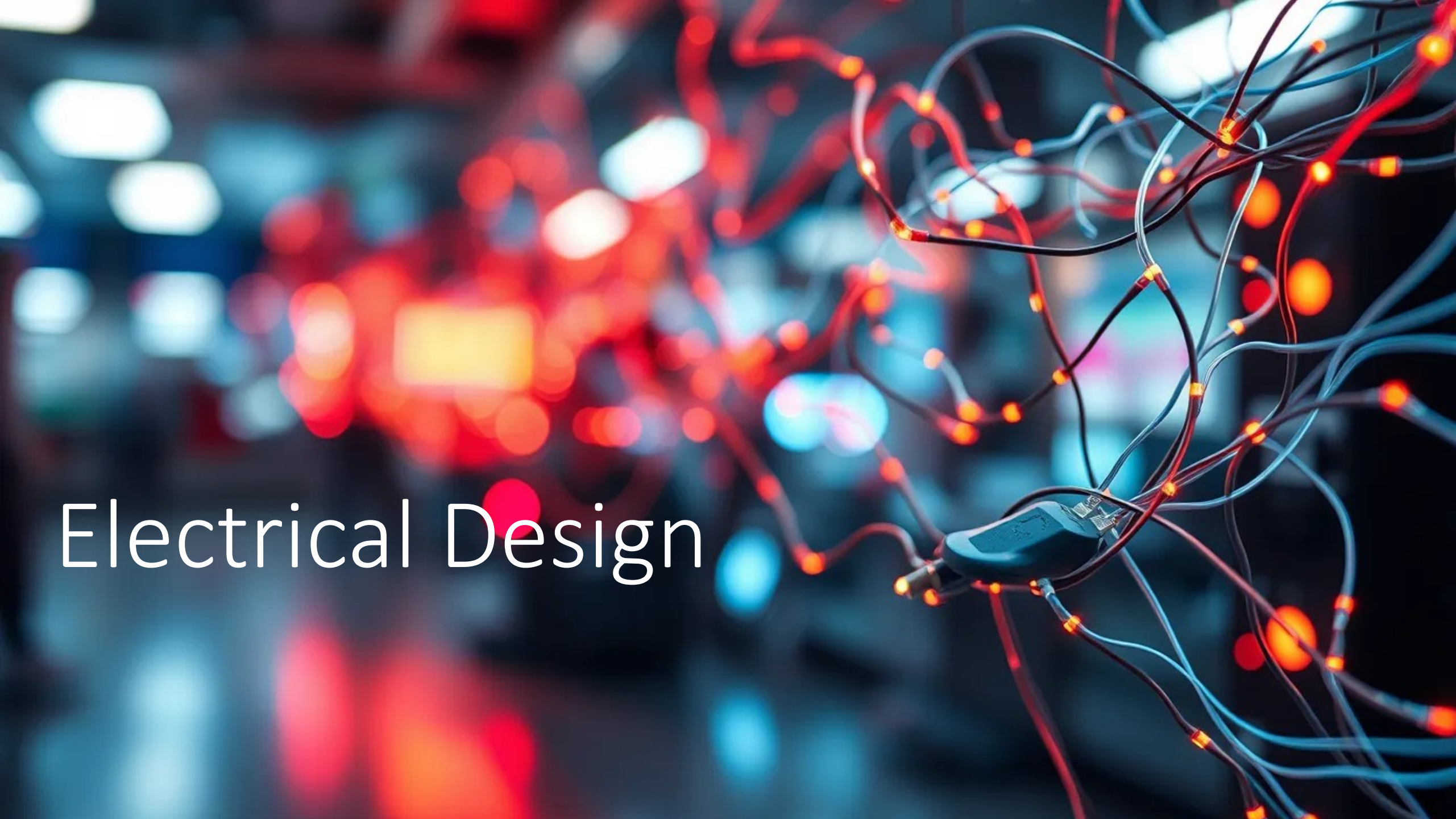


Cooling

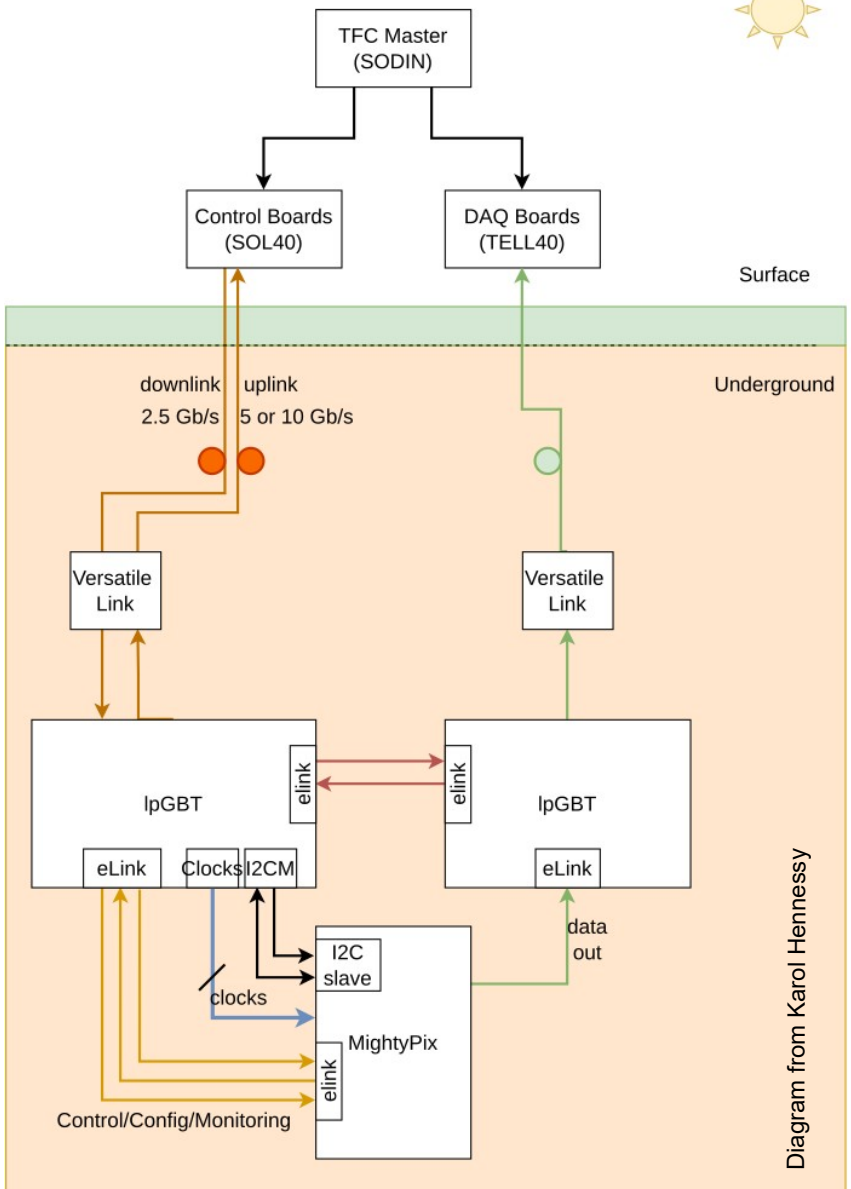
- Baseline two phase CO_2
- The natural detector layout favours a colder beamhole area
- For -10°C at chip → -25°C coolant
- Sensor power dictates the number of cooling lines






Electrical Design

DAQ Concept

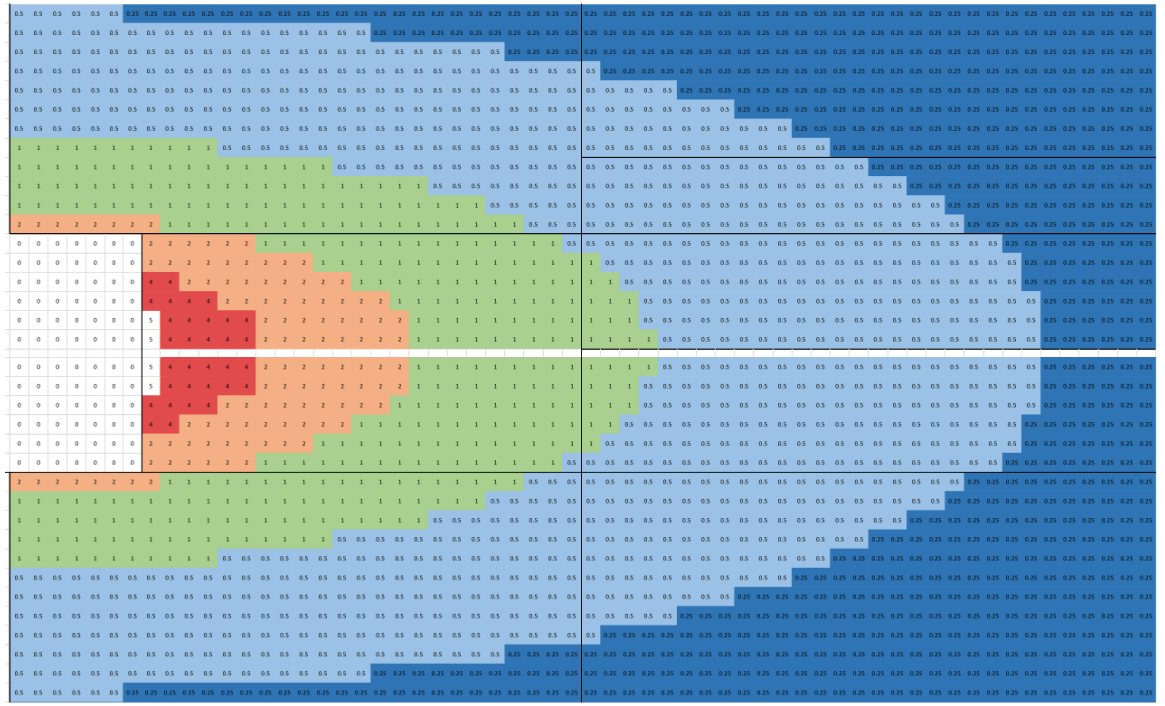


Triggerless readout → **All hits** have to be shipped **out** of the Detector!

The readout **speed and number of links** will be be **adjusted** to the expected occupancy

Hottest chip: 1.7hits/25ns → 17MHz/cm² **~3Gb/s** per chip (+margin)

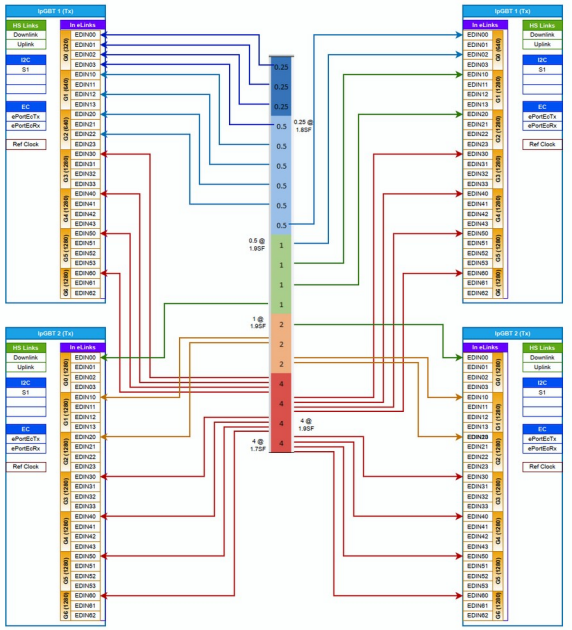
→ we need more than one link



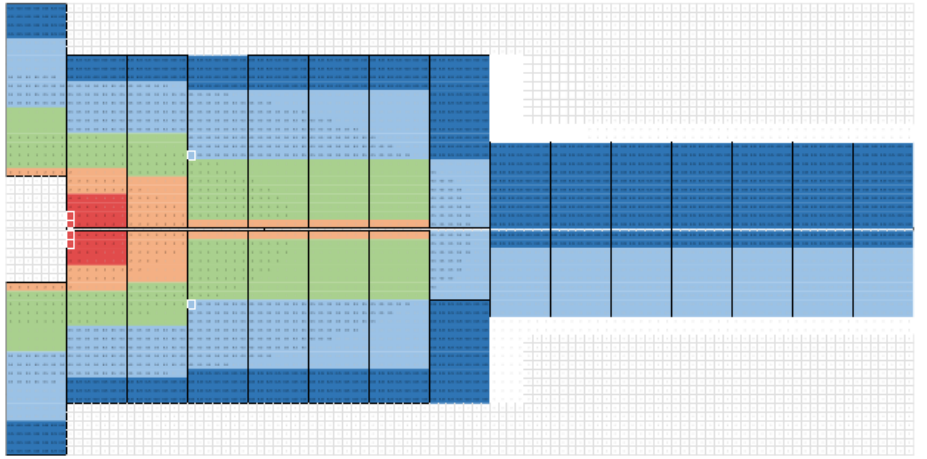
0.25	320Mbps
0.5	640Mbps
1	1280Mbps
2	x2
4	x4

Link Optimization

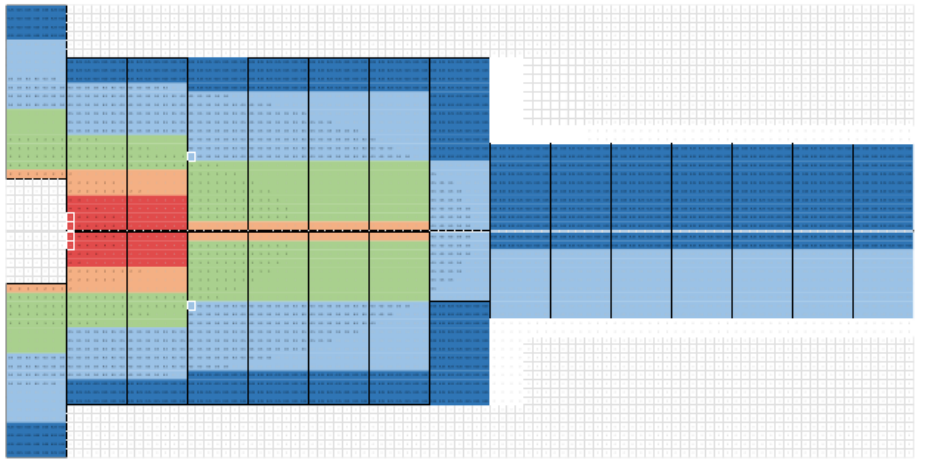
- To build the modules one wants to reduce the number of module flavours
- This is especially important, if we use the same flex/connector everywhere



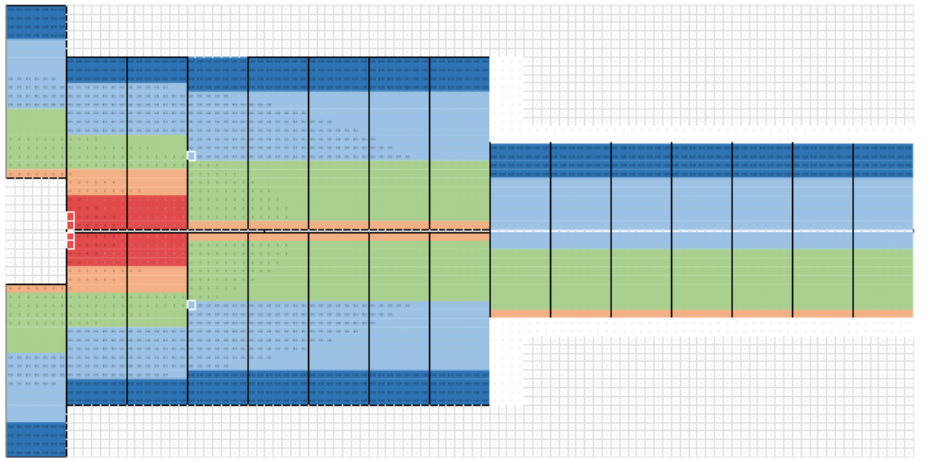
4 flavours



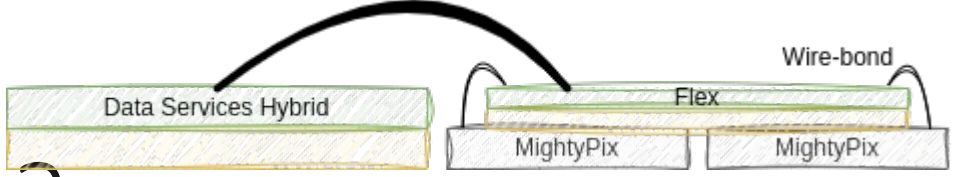
3 flavours



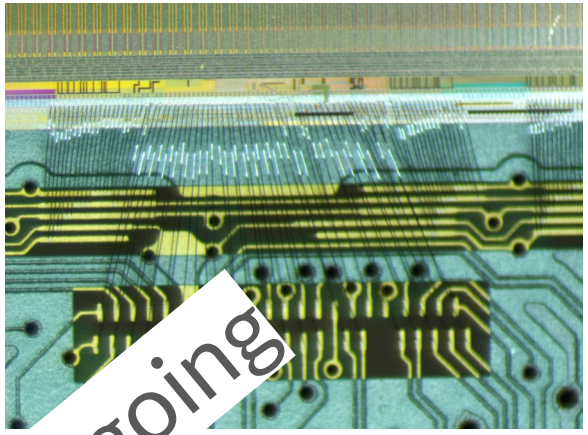
2 flavours



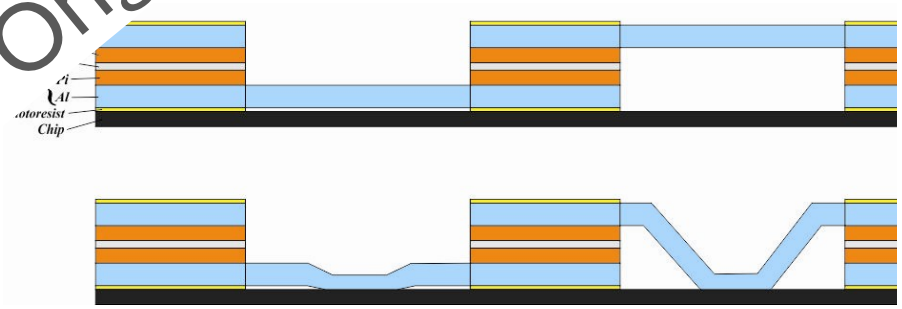
How to Connect?



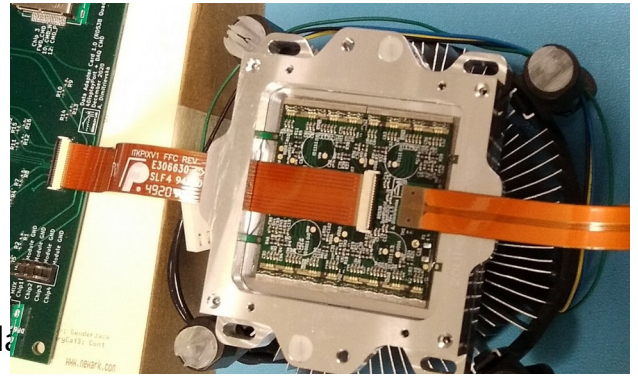
- Wirebond
  - One time connection
  - Low material budget
  - Sensitive
- SpTab
  - One time connection
  - Needs Al-Flex
  - low material budget
- Connector
  - Connections possible multiple times
  - Unsecure connections
  - High material budget



Evaluation Ongoing



ALICE TDR 17

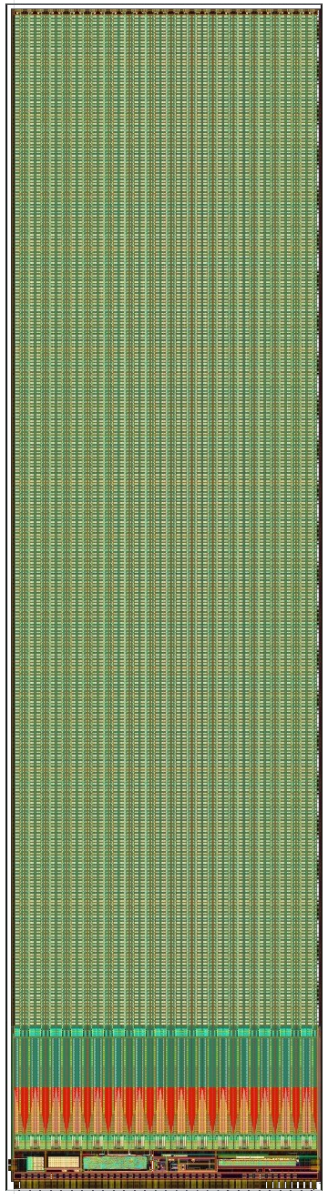


Kl

HVCMOS Sensor Design

MightyPix1 Design Specification

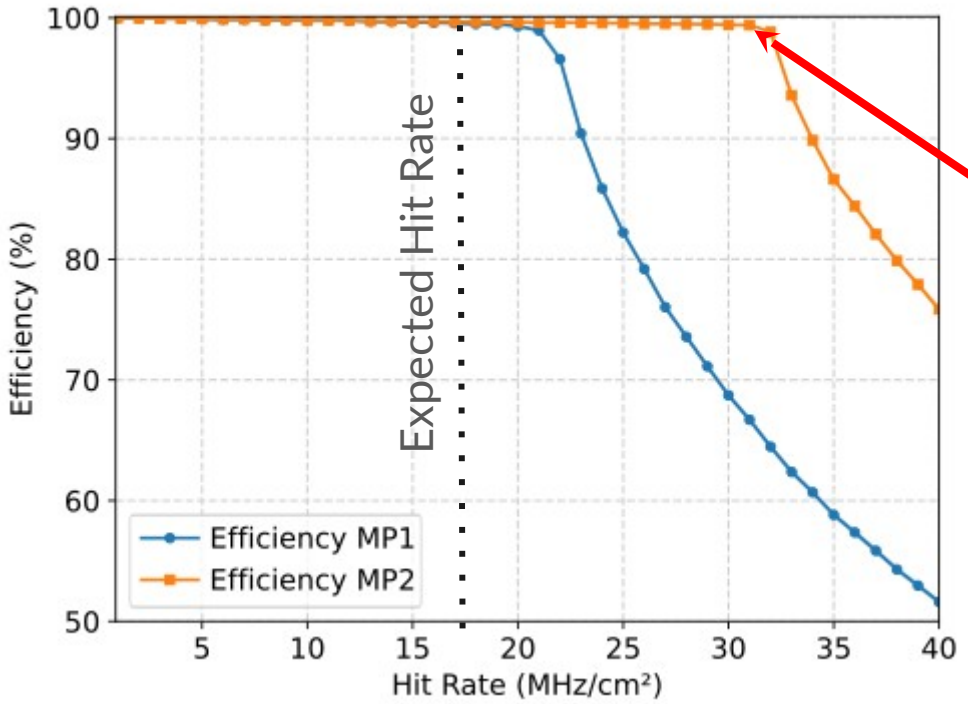
- Chip size: 5 x 20 mm^2
- Pixel matrix: 29 x 320
- Pixel:
  - 50 x 165 μm^2
  - CMOS amplifier and CMOS comparator (~3ns Resolution)
  - Data format: 2 x 32bit per Hit
  - Digital Interfaces:Timing and Fast Control (TFC)
  - Slow Control (I2C)
  - Shift-Register Interface (SR)
  - Clock Generation:
  - External: 640 MHz and 40 MHz from lpGBT
  - Internal: CML and CMOS PLL with 40 MHz reference clock (planned to be used in LHCb)
- Bias Voltages:
  - Integrated 10bit voltage DACs
  - Supplied externally
  - HV > 120V possible
- Data output 1 x 1.28Gbit/640Mbit/320Mbit
- NIEL 3 x 10^{14} n_{eq}/cm^2



Layout for MightyPix1
(1/4 of full size)

Hit Rate Simulation

S. Scherl (KIT/Liverpool)

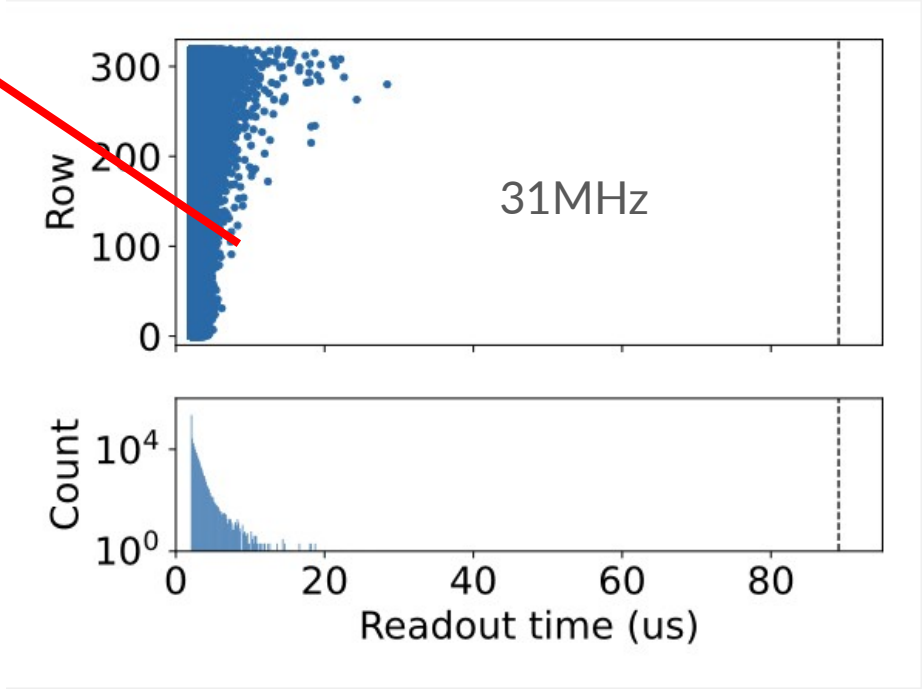


Expect a Hit rate up to **17 MHz/cm²**

MightyPix 1 should work up to **20 MHz/cm²**

MightyPix 2 will work up to **32 Mhz/cm²**

Probably further reduction possible with less data



S. Scherl (KIT/Liverpool)

Hit Rate Simulation

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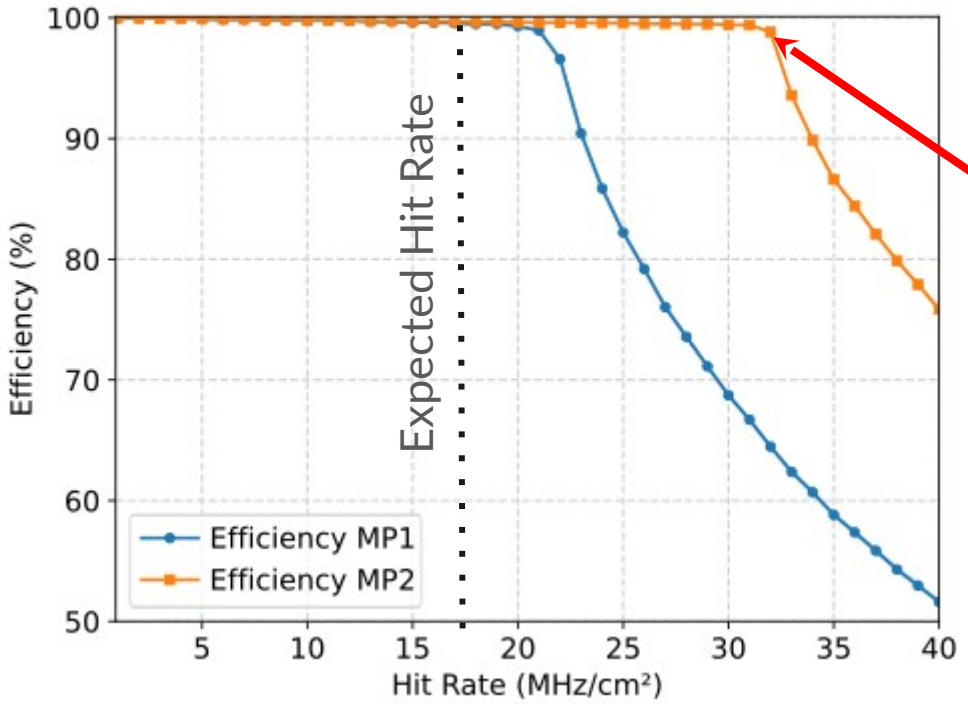

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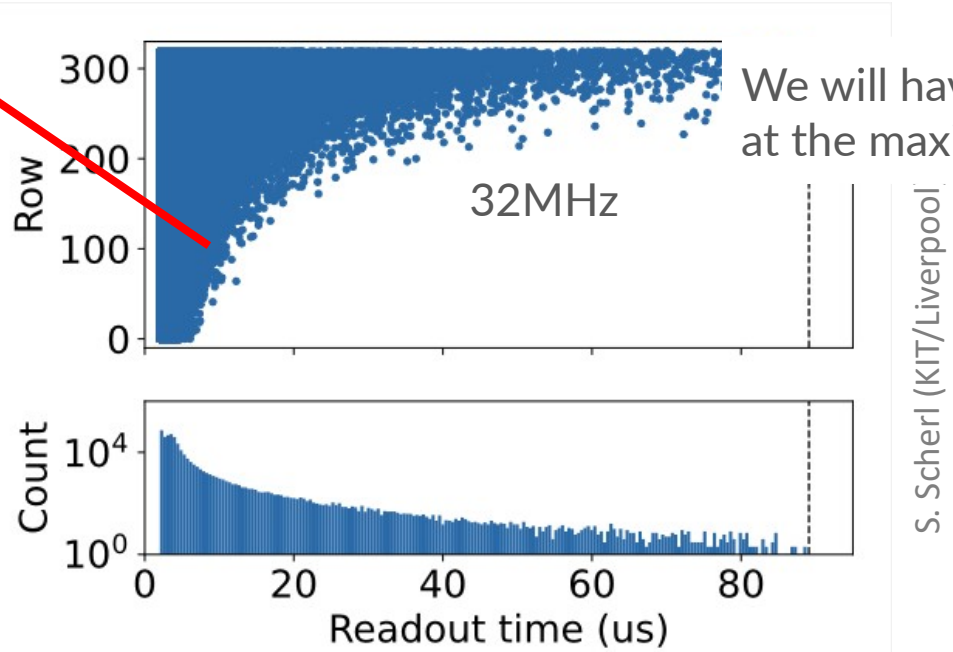


We will have a sharp drop at the maximum hit rate

S. Scherl (KIT/Liverpool)

Current Status of the Sensor

MightyPix 1

There is a problem with the configuration of the MP1

→ could be roughly fixed by FIB surgery

The time binning is rough

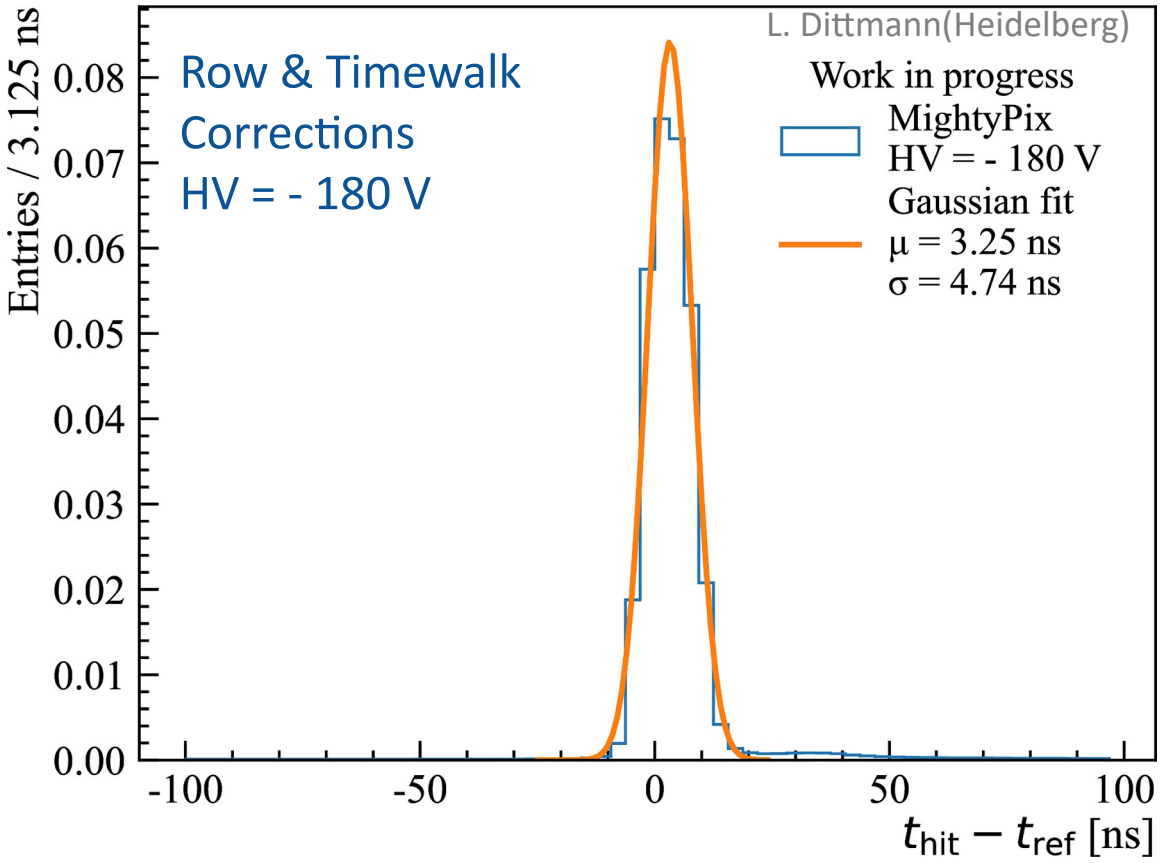
4.74 ns measured → ~ 2.9 ns intrinsic uncertainty

Power consumption 234 mW/cm² (scaled to full chip)

Due to chip repair we can not use this chip in the testbeam

→ Same analog pixel design in TelePix 2 (½ the pixel size)

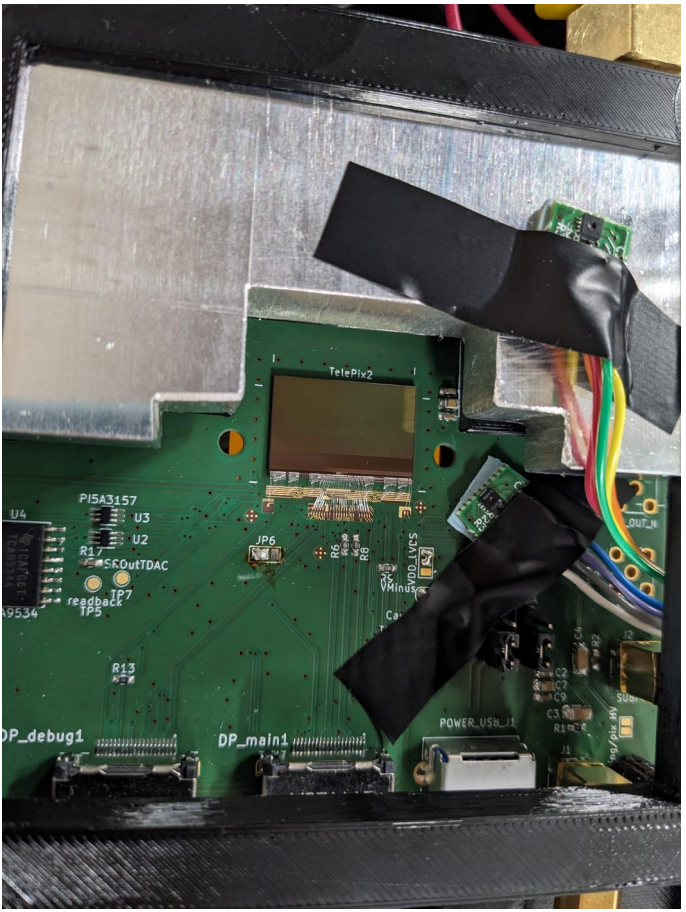
Lab measurement



Many Thanks to our colleagues from DESY, KIT and Heidelberg we are validating this with the TelePix 2

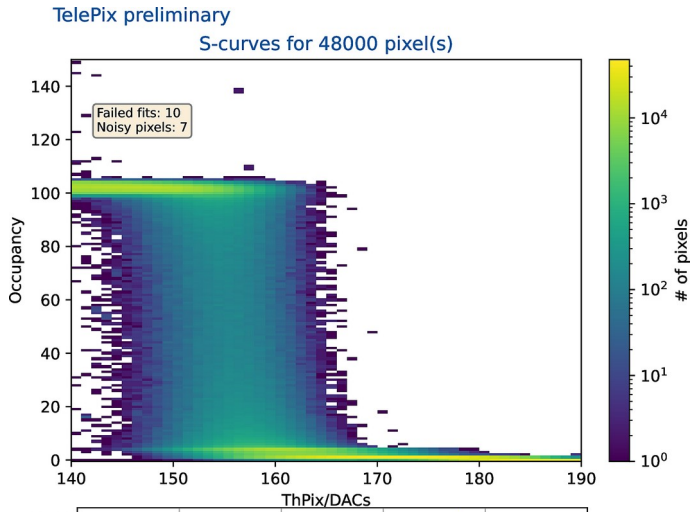
*these sildes will not be uploaded since DESY is preparing a publication soon

TelePix

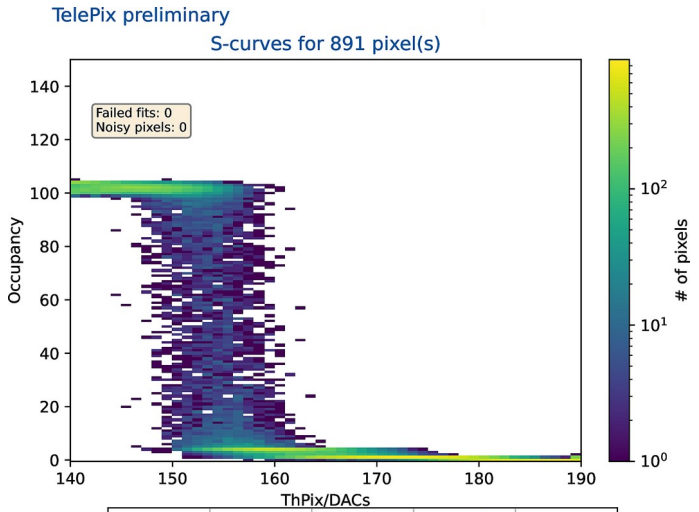


- Sensor designed for DESY testbeam as telescope sensor
- Same analog Pixel (with half the size) as the MightyPix1
- Workhorse to get our DAQ infrastructure up and running (very successfully) thanks to the basil framework and support from SiLab

We could get started with the basics:



Tuning



Time Resolution Measurement

Idea & Goal:

- To be in-time efficient (Hit within 25ns window) a time resolution $\Delta T < 3$ ns is necessary

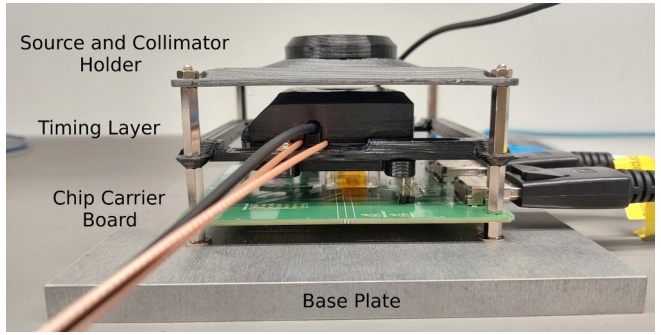
What is needed:

- TS from chip → Part of data word
- TS from reference layer → Scintillator with 2 SiPMs

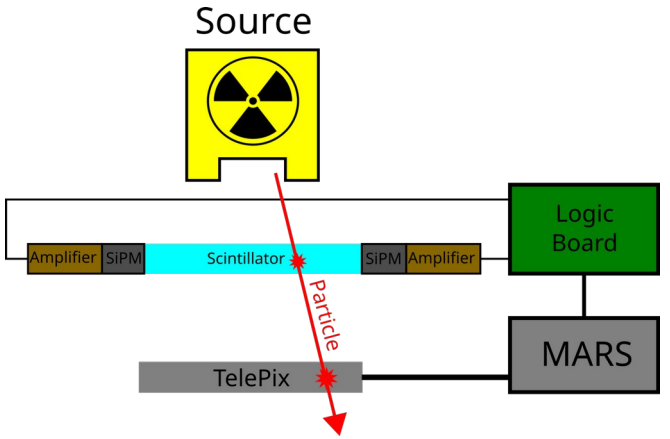
$\Rightarrow \Delta T = T_{chip} - T_{TL}$

Procedure:

- HV: -120 V chip biasing
- Perform scan of “x” min with Sr-90
- Corrections: Row & column delay, time walk corrections



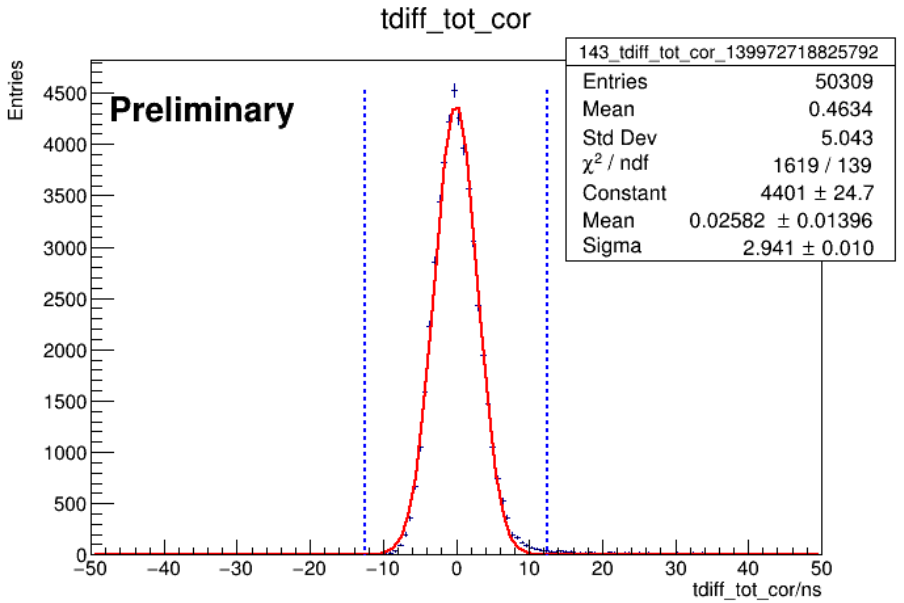
N. Sommerfeld and H. Schmitz

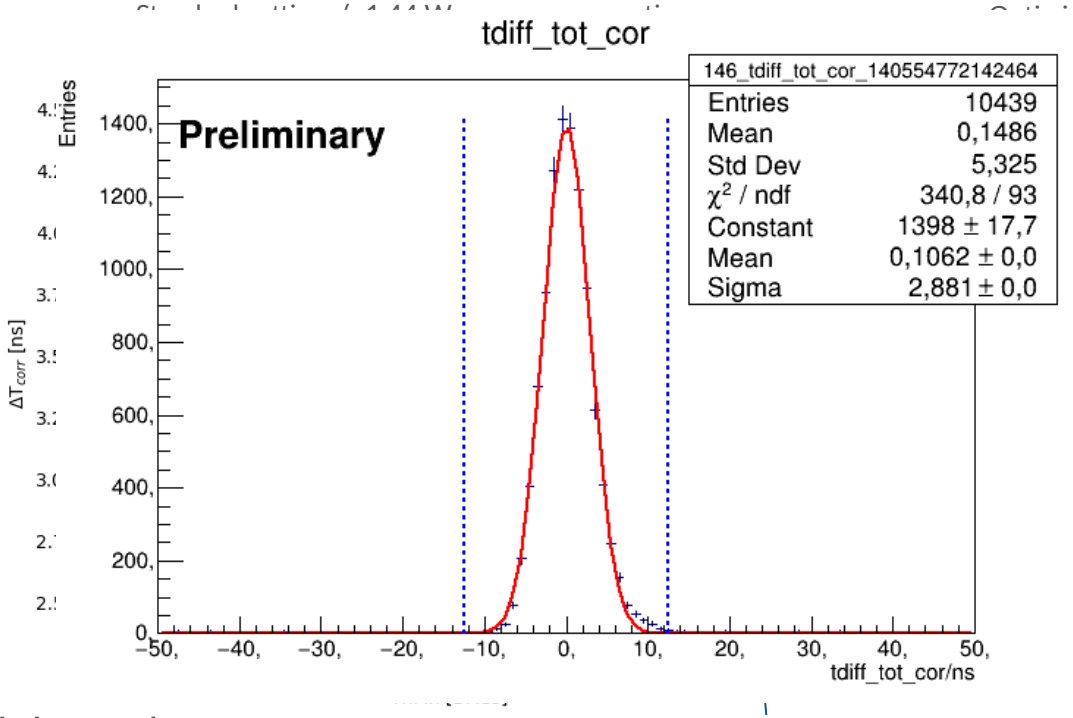


Time Resolution- Results

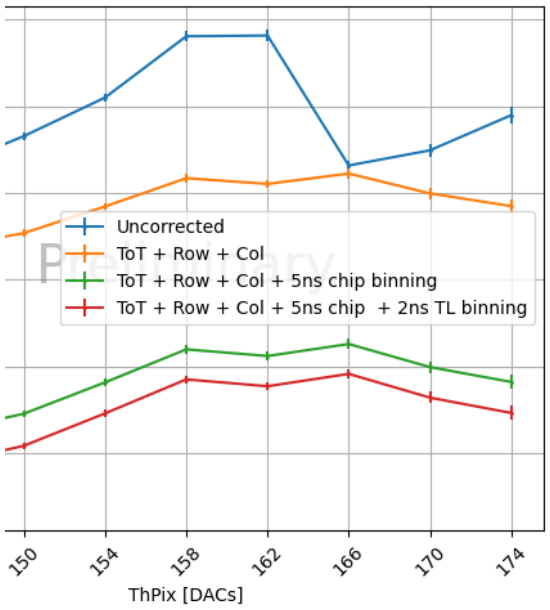
After 10^{14} 1MeV n_{eq}

After correction





ed settings (~1.7 W power
ption, VDDD: ~0.7W & VDDA: ~1W)



- Time resolution highly threshold dependent
→ No plateau
- Compatible with testbeam → ~3 ns w/o binning correction

Fit fails if time walk is too large

N. Sommerfeld and H. Schmitz

Moving Forward

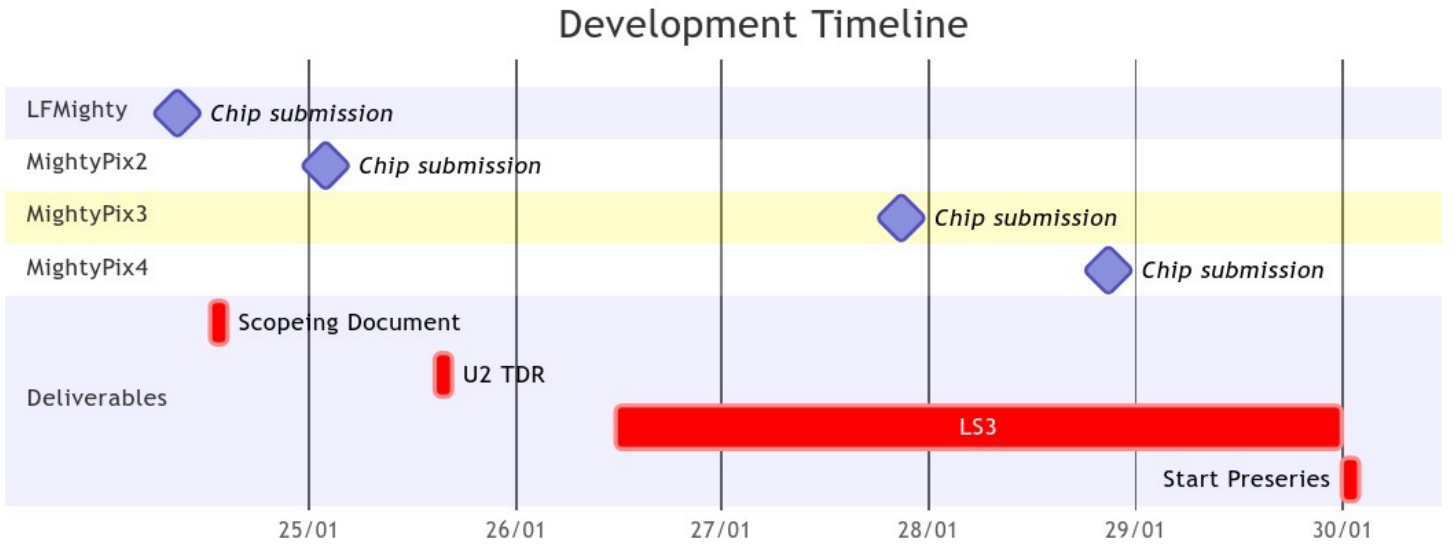
TSI was bought and closed the 180nm HVCMOS production end of 2023

→ thanks to the “standard” process we can go back to AMS

Will investigate LFoundry submission in parallel

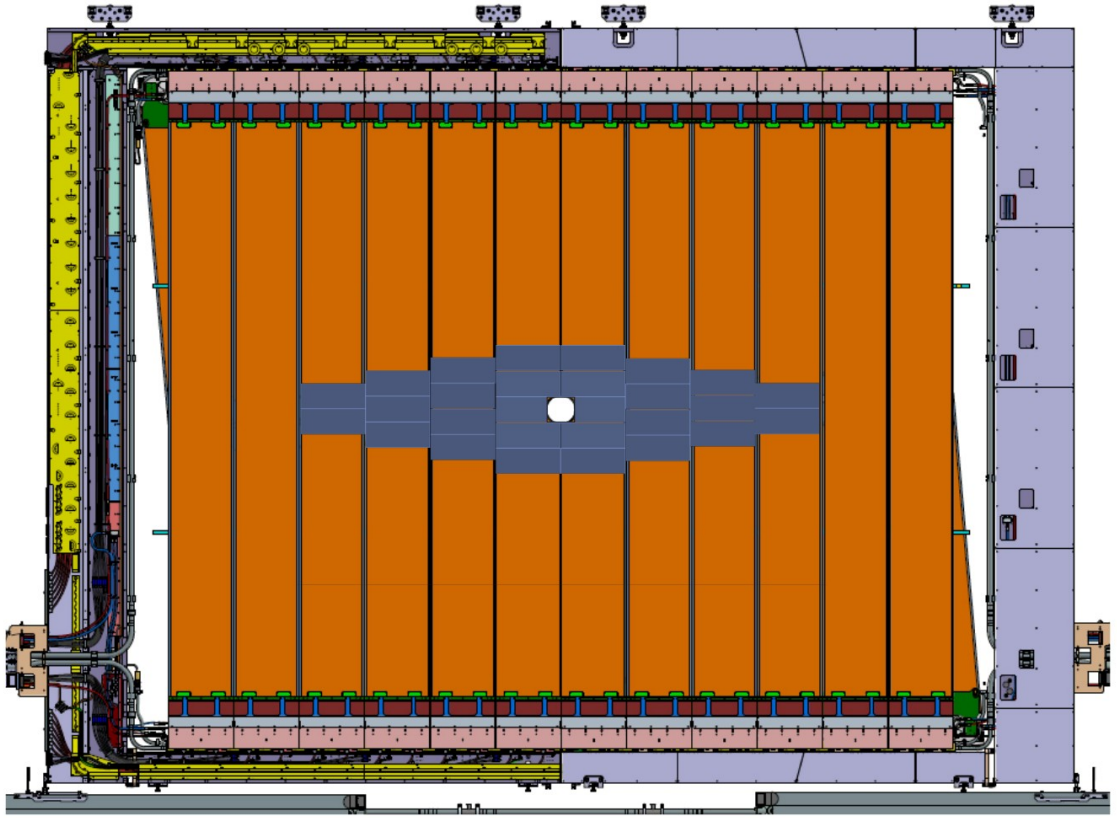
Main changes for MightyPix 2:

- Correct errors from MightyPix 1
- Faster FSM (prob. 32Bit output)
- Faster “slow” control to program the chips
- Evaluate the AMS and LFoundry processes

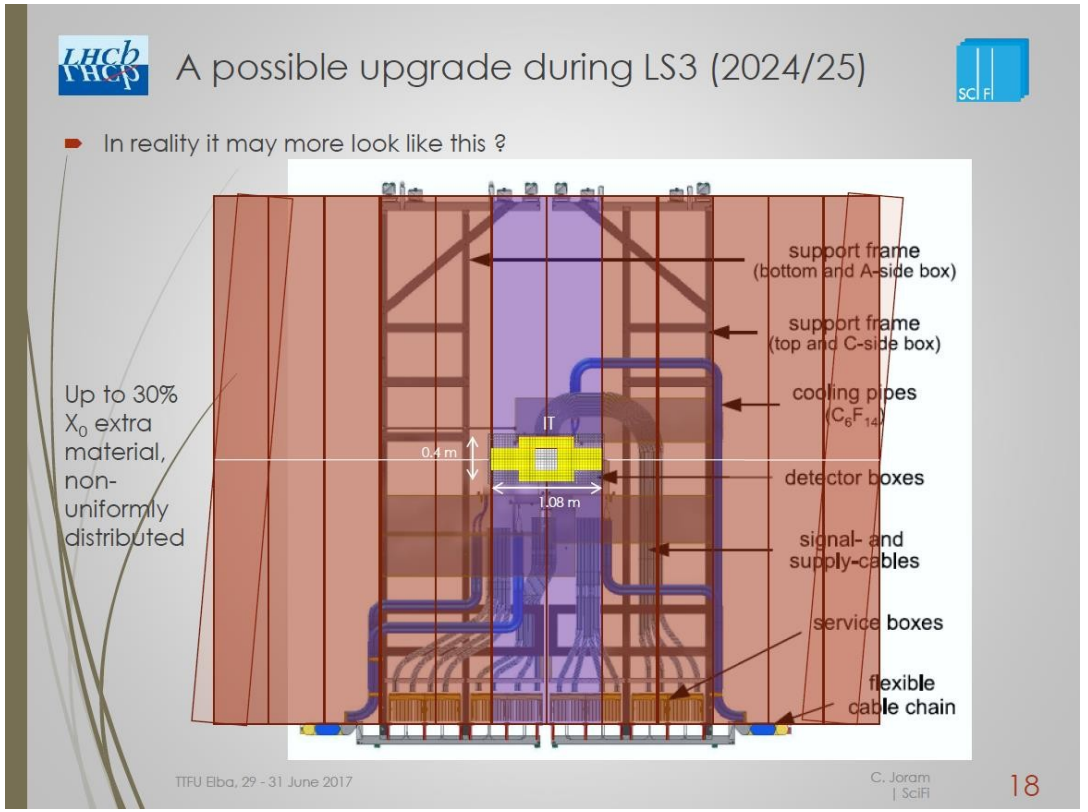


Keep the Goal in Mind!

Tracking Heaven



Tracking Hell



From 2019 Blake Leveringdon

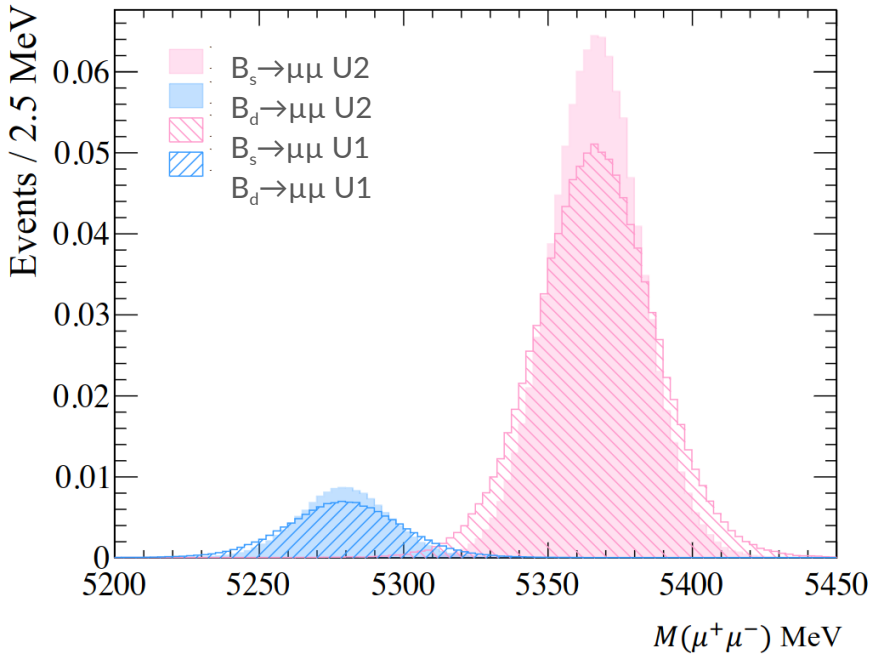
Summary

- A lot of work already done
- Module Design in last iterations
- Electrical DAQ layout being finalized
- Sensor is fast enough
- Scoping document published

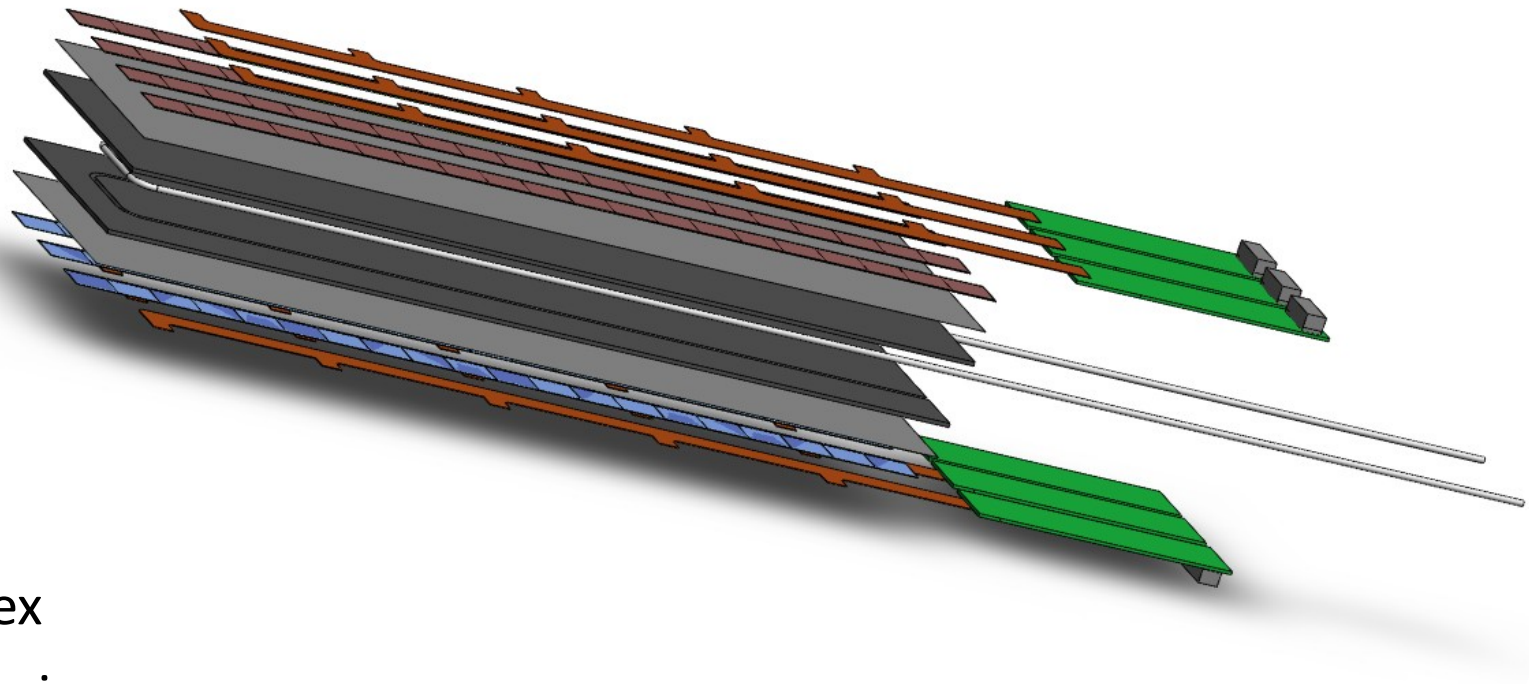
Plans

- Next step TDR
- Testbeam with TelePix 2
- Submission of MightyPix 2
- Avoid Purgatory
- Have a LHCb after LS4

Mary Richardson-Slipper (Edinburgh)



Plans for Bonn



- Wafer testing
  - FPGA setup
  - ASIC knowledge
  - Wafer prober
- Chip to Flex (Sensor Modules)
  - Mounting of 5 sensors on flex
  - Evaluating pick and place vs gig
  - Needed are ~5 Sensor Modules/day → 3 year production
  - Wirebonding or SpTab
  - QA

Backup

LHCb note 2008-055

LPHE note 2008-13

Survey of the Cables of the Inner Tracker

V Fave
EPFL

October 16, 2008

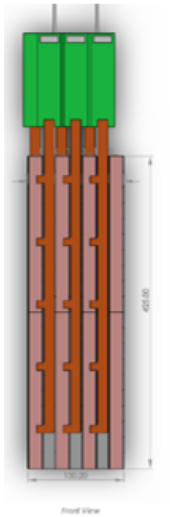
Abstract

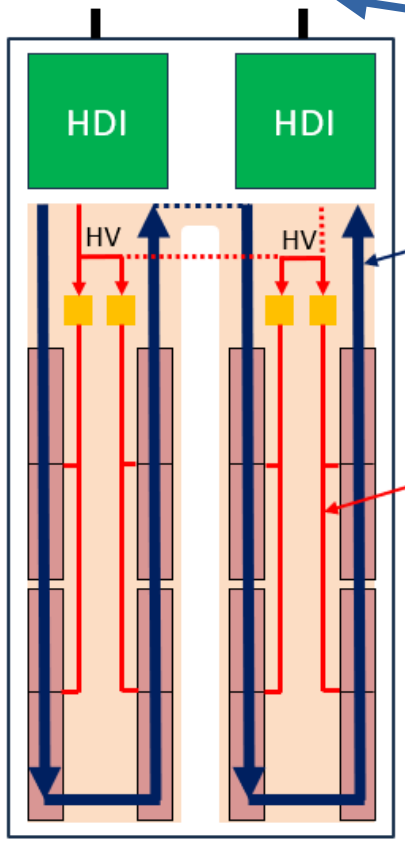
The position of the cables of the Inner Tracker in July 2008 is surveyed. The different steps from photo taking to XML implementation are presented.

For the original IT detector it took many Students and a lot of work to correctly estimate the material budget of all the services

Power

Serial Powering





Integrated MT module

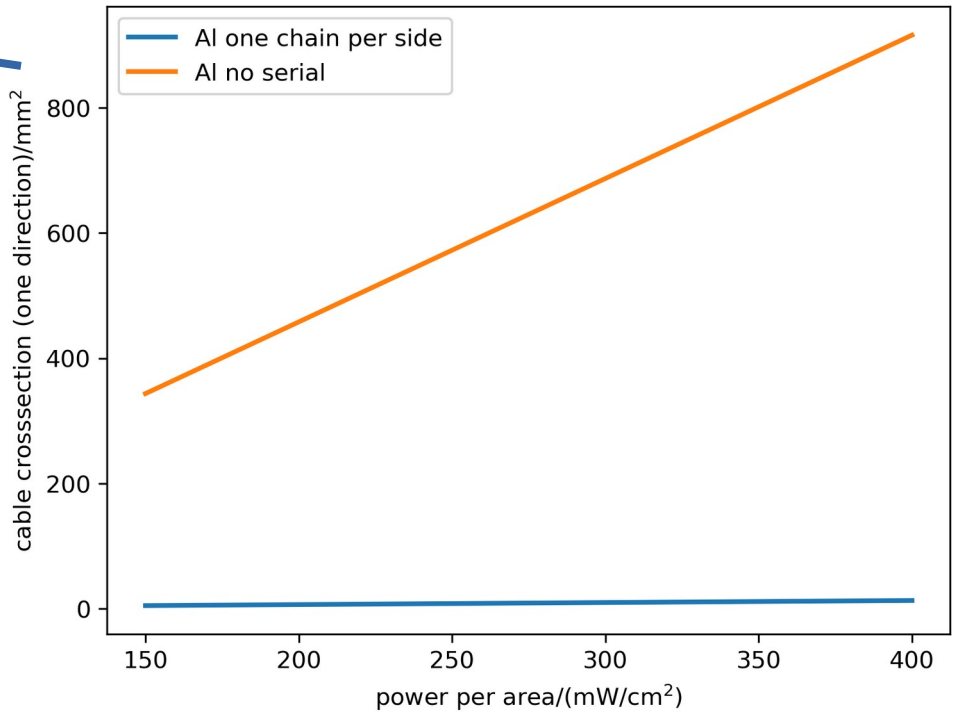
Here we don't want to have the thick cables!

Serial Powering, 2 options:

1. Across 2 columns, 8 drops
2. Across 4 columns, 16 drops

Sensor Bias (HV), HV switch per columr

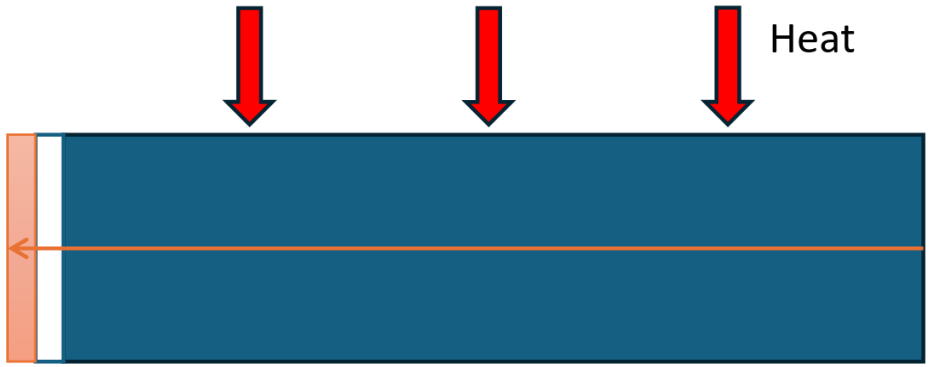
1. Single HV feed to module
2. Dual feed for redundancy

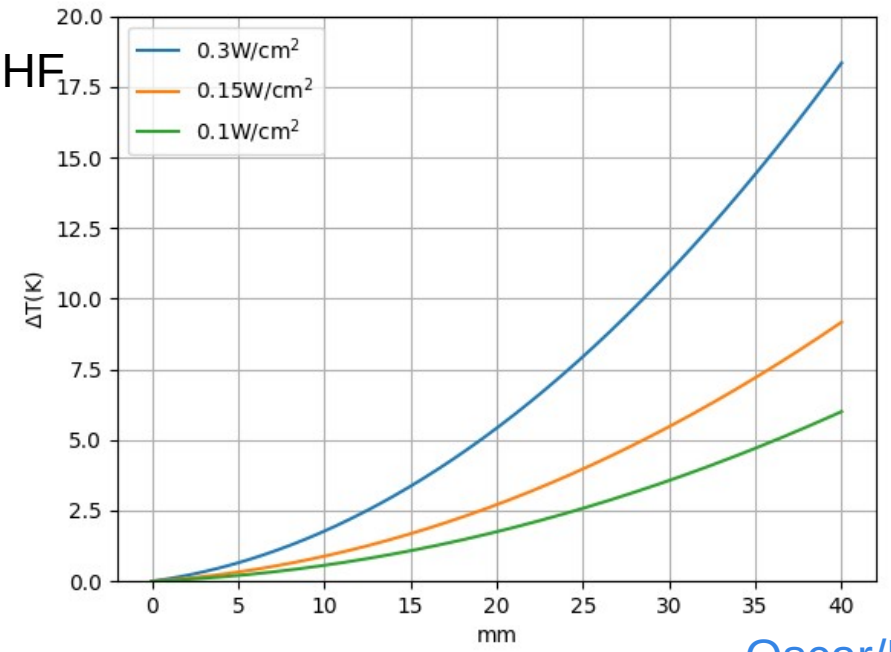


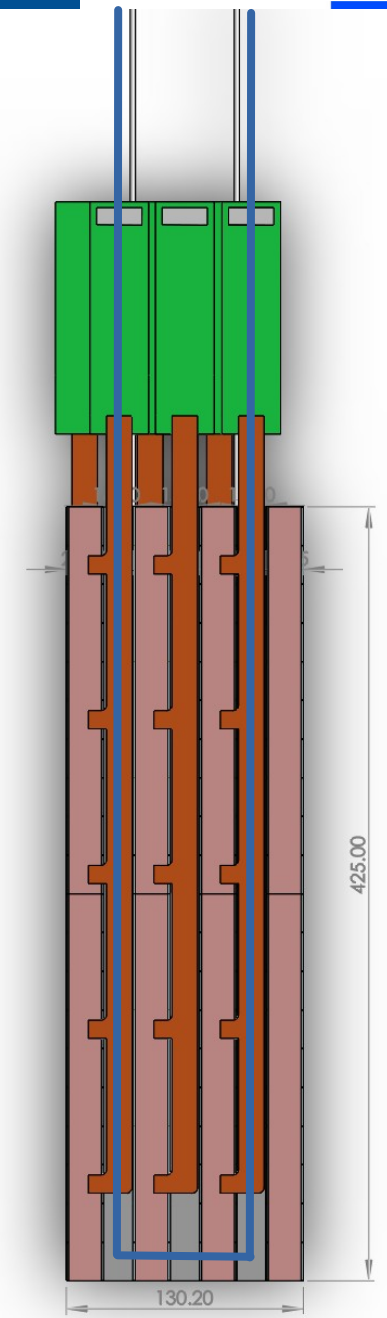
LV-Power

- At the moment one cooling line is planned to cool 3.5-4 sensors
- This already creates a ΔT~10°C depending on the cooling pipe distance + ΔT~10°C CF to sensor → Coolant to sensor ΔT~20°C
- Minimal Temperature that can be achieved with CO_2 is -30°C (we want -20°C), which translates to ~-10°C on the coldest sensor → 0°C on the warmest senor
- Probably we want more cooling at the “bottom” of the module

For 12m^2 we need ~40kW cooling power
This fits nice with one CO2 plant (~50kW) 0.5MCHF

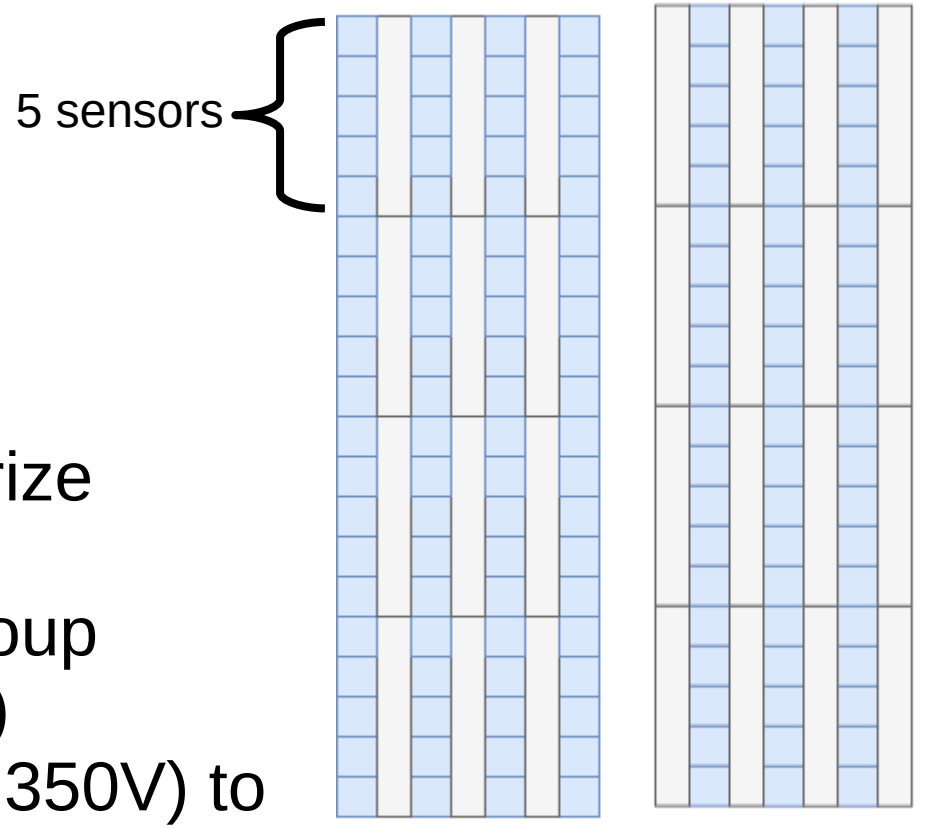






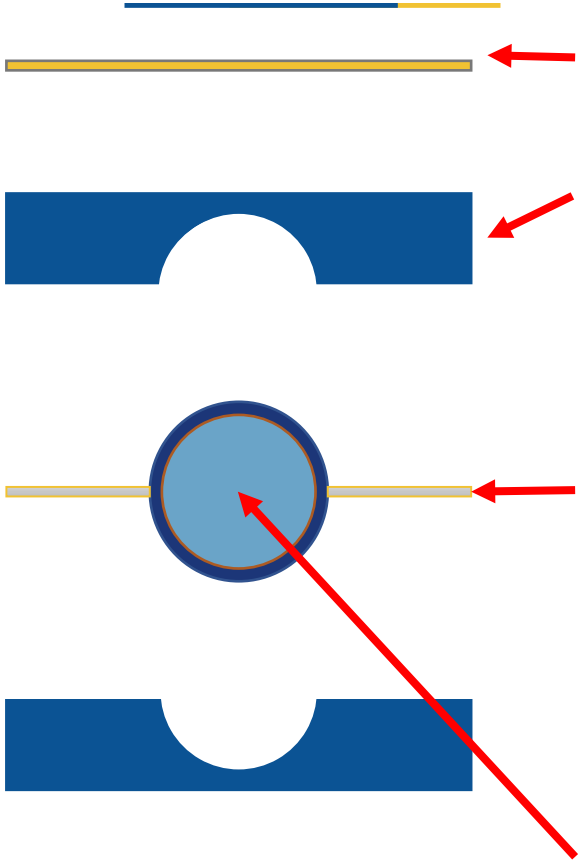
Oscar/Bilal

Serial Powering



- Integrated into the ASIC
  - Backup: maybe external chip possible (factorize problem)
- ASIC group of 5 would make a good power group 1.67A (up to 3.4A depending on sensor power)
- Use GaN FET (up to 700V avilable, maybe 2x 350V) to secure against HV failure
- Have to optimize cooling within one module

Module Prototypes



Carbon fibre - Cocuring in Liverpool (~150um)

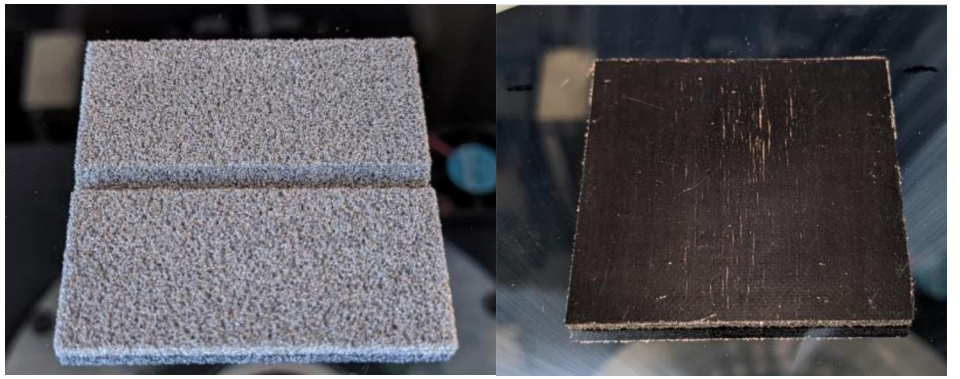
Carbon foam available for small samples

- 2 mm thick

Carbon veil + Glue (Hysol + graphite)

Polyimide tubes
Lewvac, 2.822mm OD, 76µm wall thickness
Microlumens can provide longer lengths (55" 2.54mm OD)

We will use Titanium tubes if we have to reach a low temperature



Material Budget Baseline

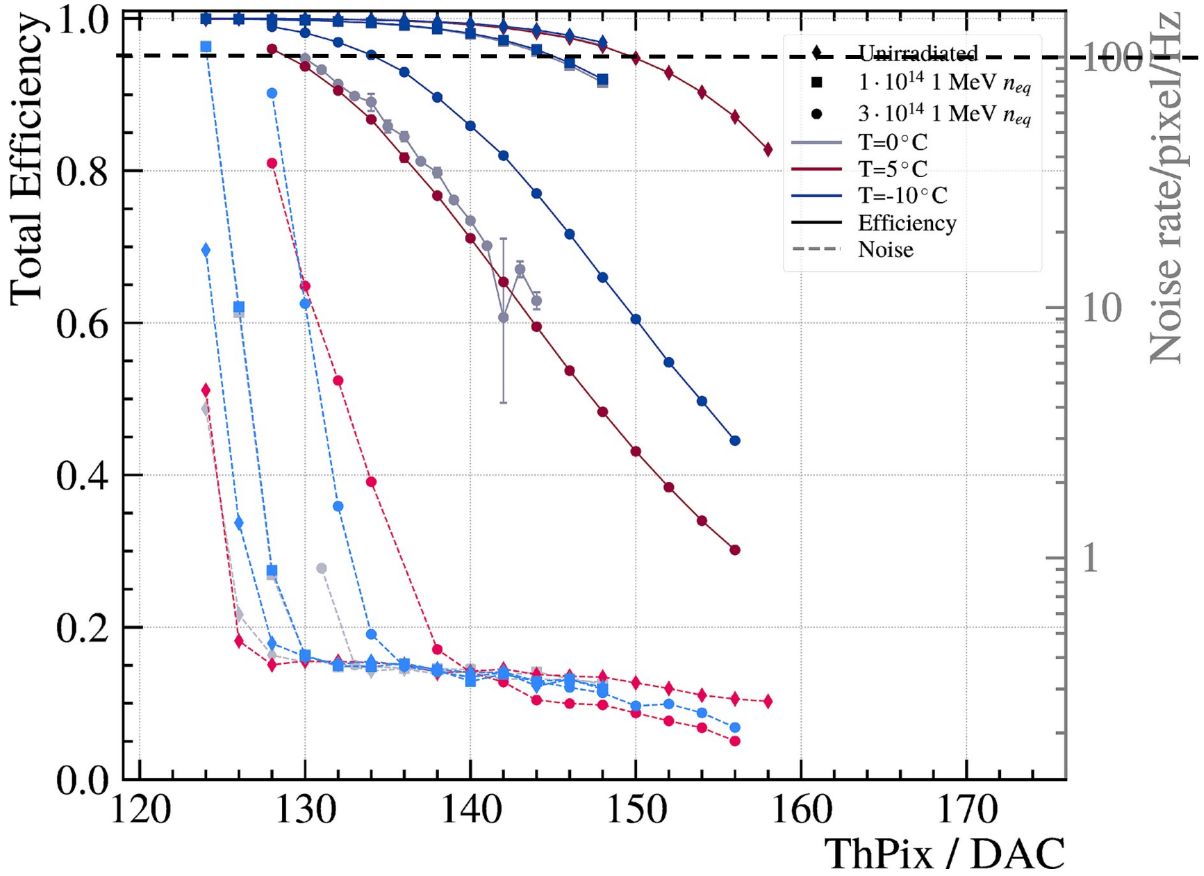
	Thickness um	Layers	X0	X/X0	Filling factor	With Scifi	Density g/cm3	Mass /cm2
Silicon	200	1	9.37	0.213	1			
Cooling tube	50	2	28.6	0.004	0.12		1.43	0.002
Carbon form	4200	1	185.65	0.226	1		0.23	0.097
Carbon fibre	300	2	23.70	0.253	1		2.2	0.132
Flex tape	340	1		0.356	1		1.71	0.058
Glue	120	1	35.49	0.034	1		1.17	0.014
Armacell	12300	2	801.27	0.307	1	19.266	0.08	0.197
PCB	1570	1	17.0	0.185	0.2	6.422	2.44	0.077
SUM	31730			1.578			0.182	0.577

Current estimation per layer
Largest Contributions:
insulation and flex pcb

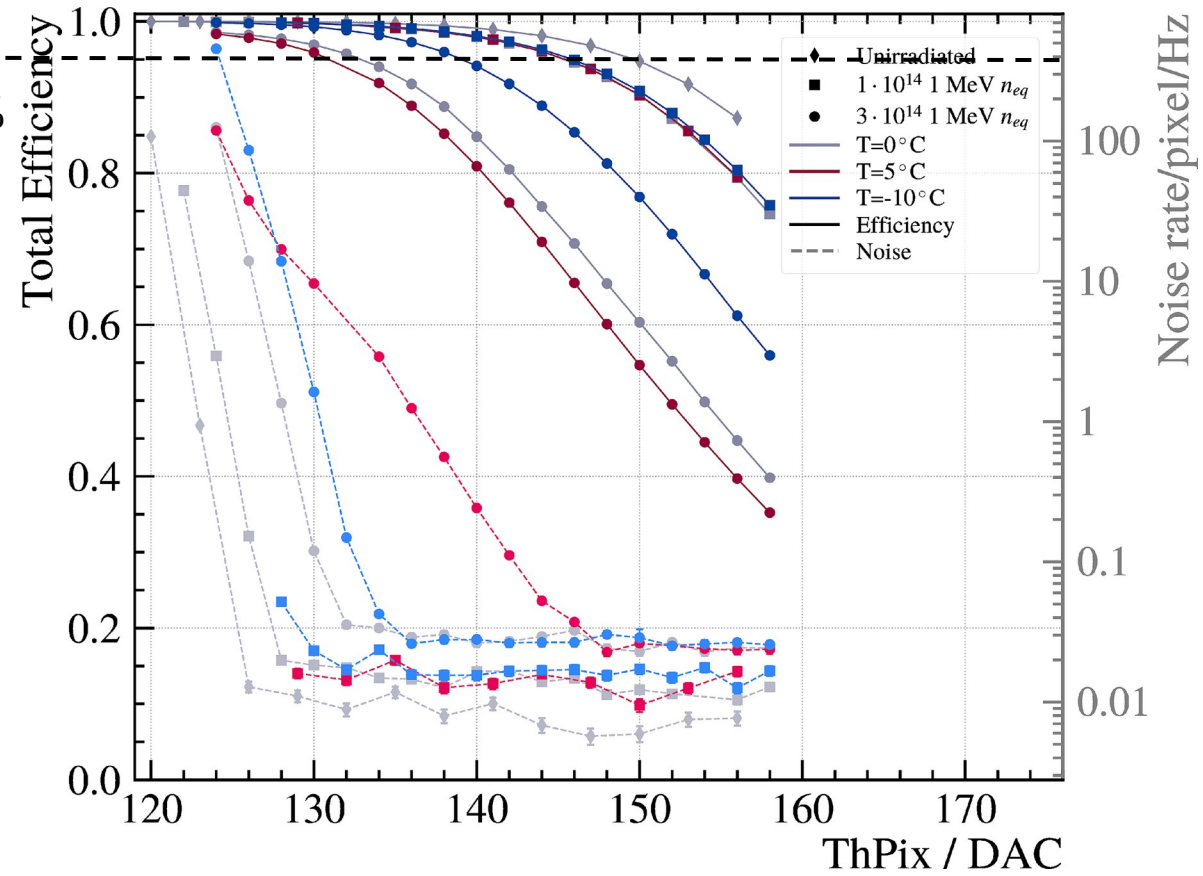
Under investigation
→ warmer operation
→ aluminum flex pcb

Testbeam results

June 22:
With PLL (low stat. For irrad. sensor)



Dec. 22:
W. 500MHz input clock



AP3.1 shows a short operation range

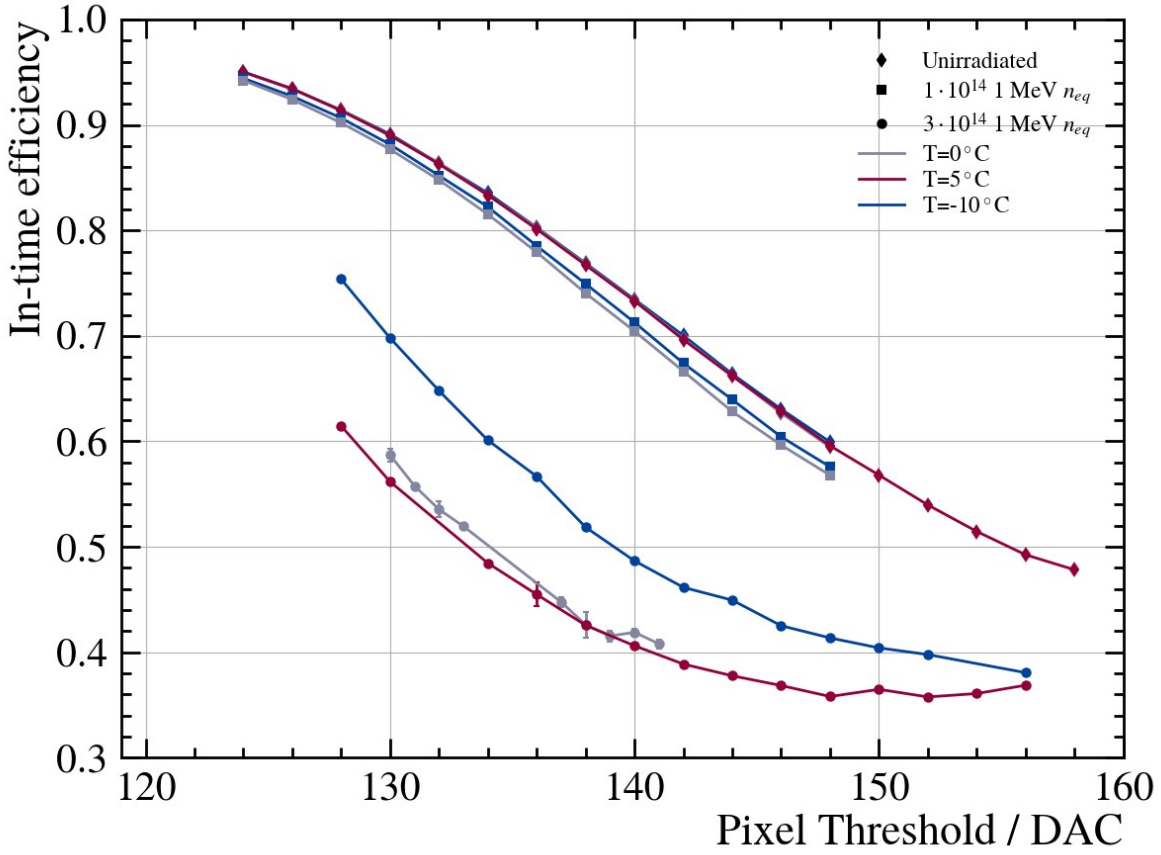
Significant decrease in efficiency at $3 \cdot 10^{14}$ MeV n_{eq}/cm^2

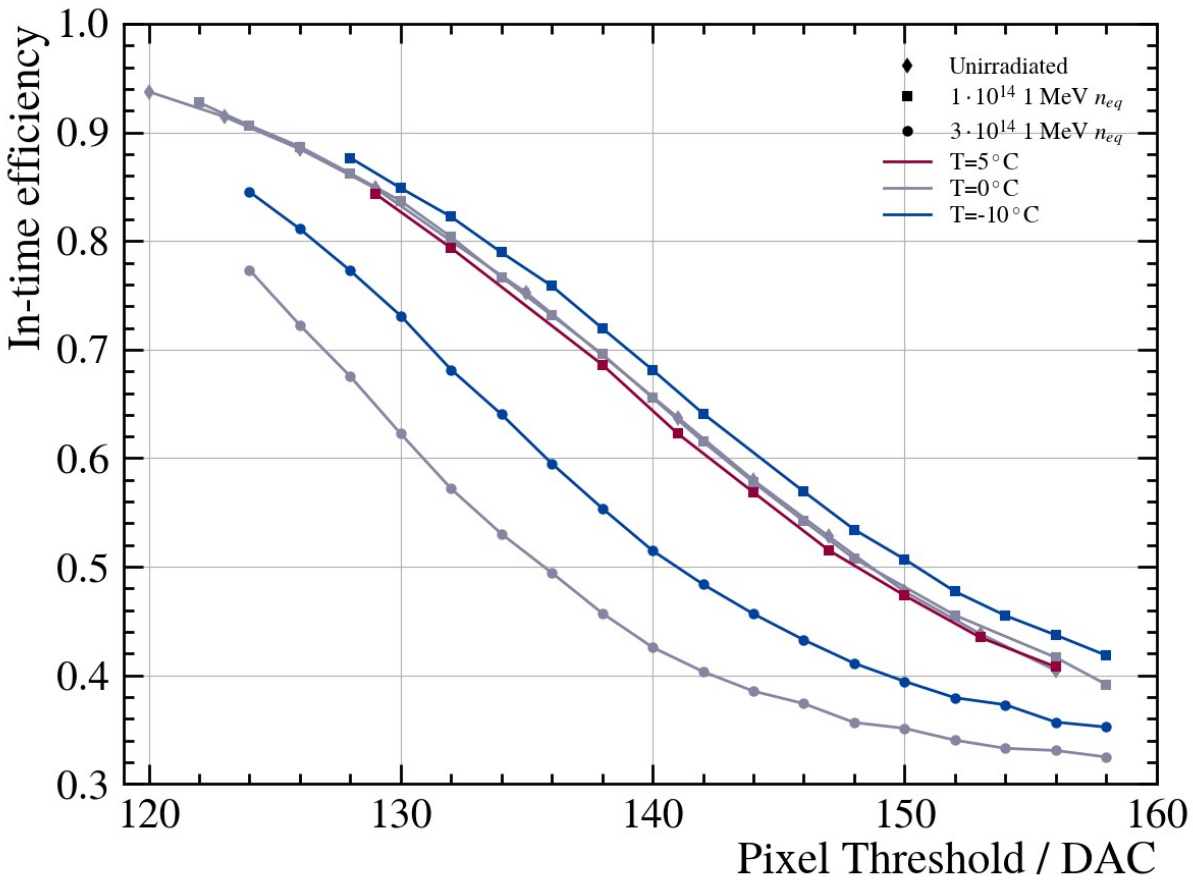
External clock (high frequency) recovers a bit the efficiency, but only with cooling some operation possible

Timing

In-time efficiency=hit within 25ns

This is with TOT and row correction

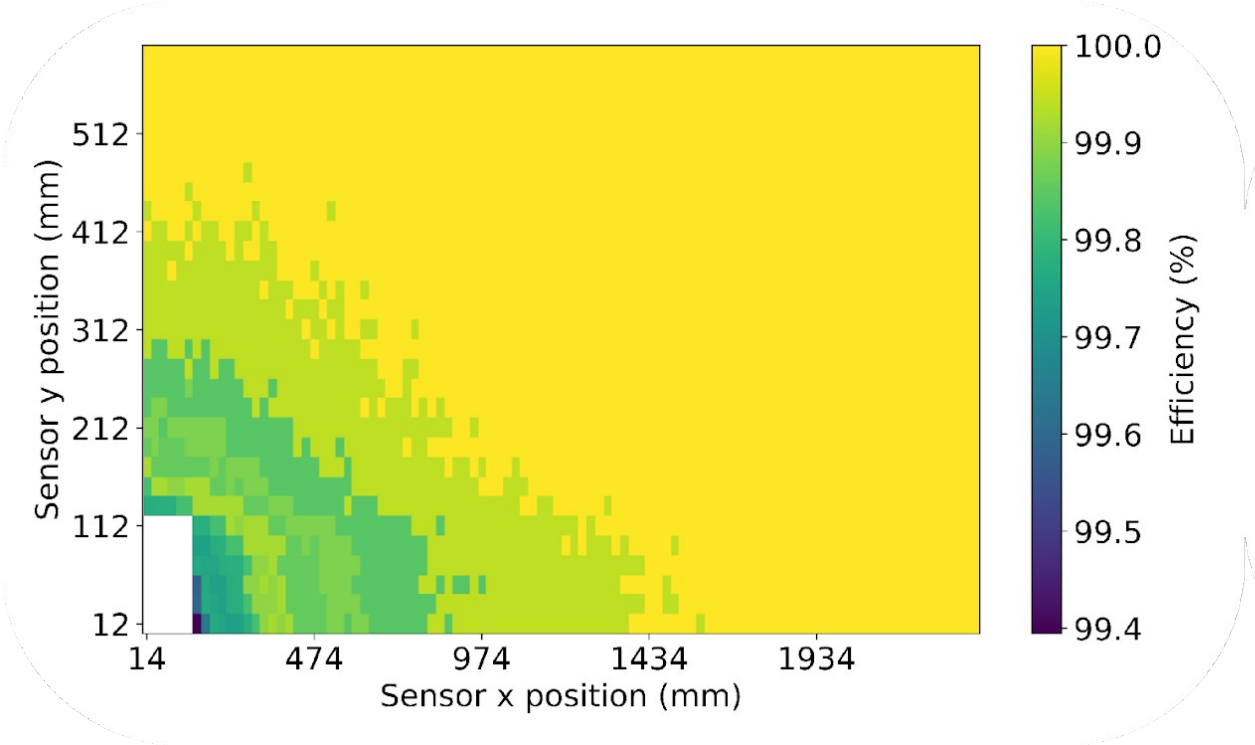


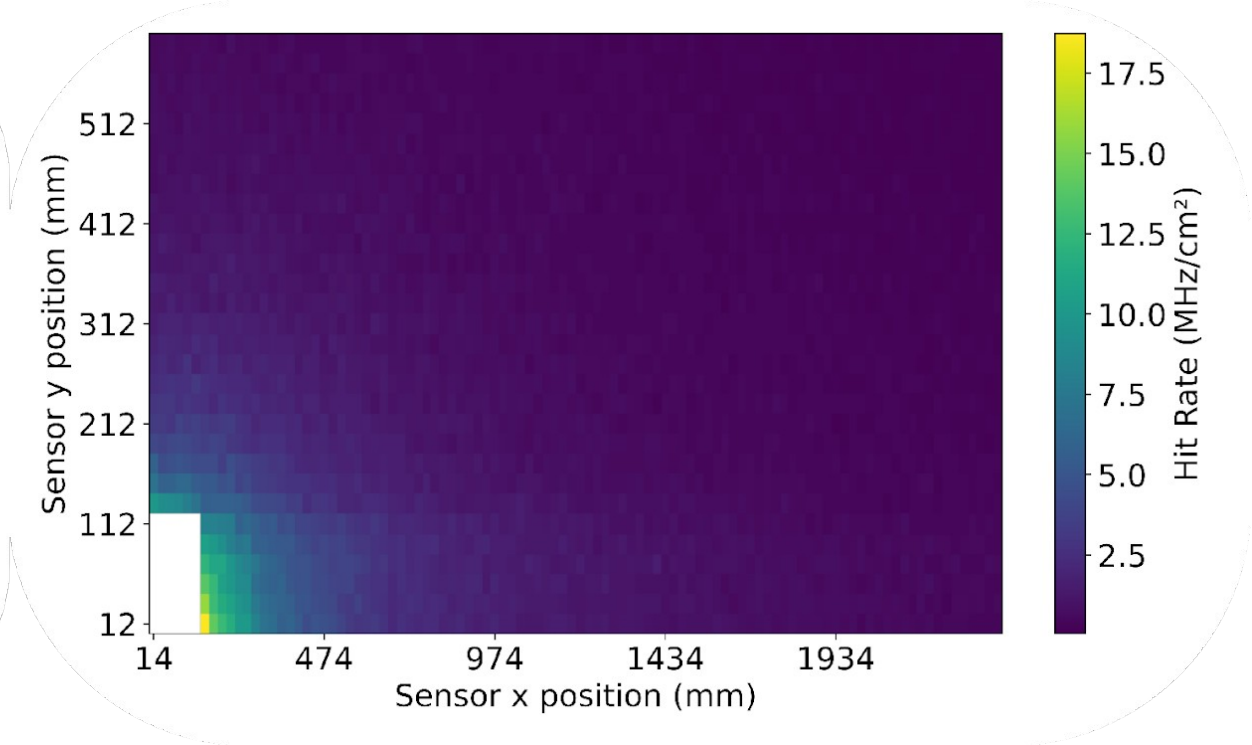


As expected the time resolution is not good enough (~5ns at best)

High impact of the radiation for $3 \cdot 10^{14}$ MeV n_{eq}/cm^2

Hit rate

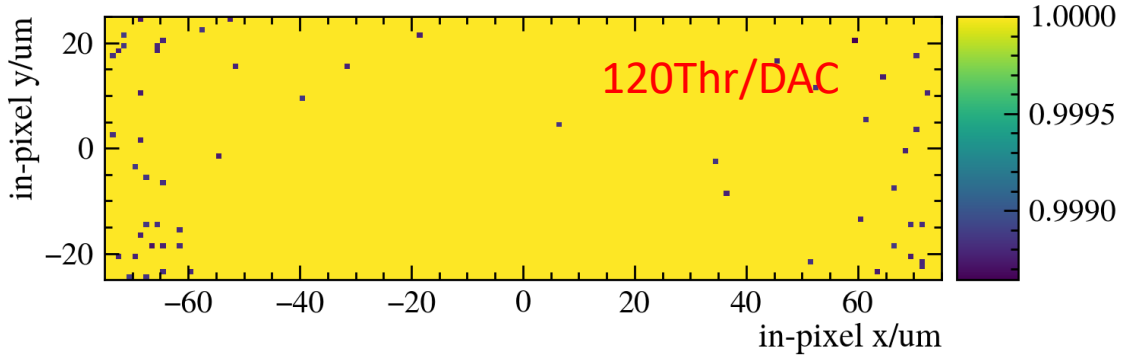


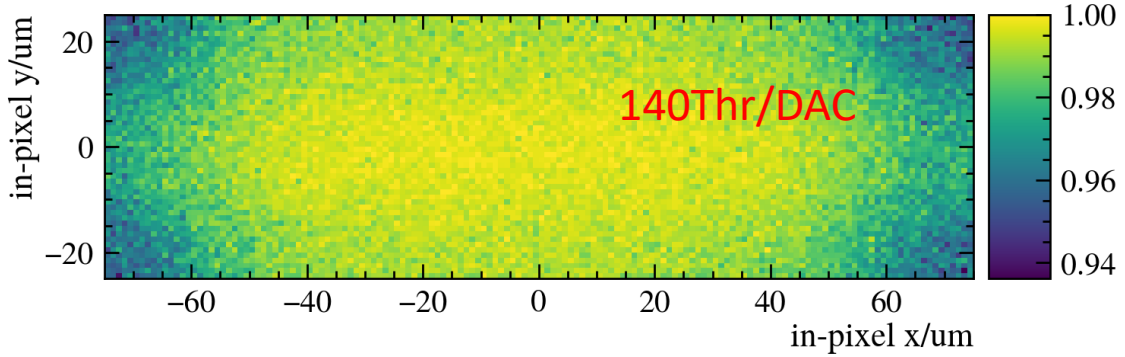


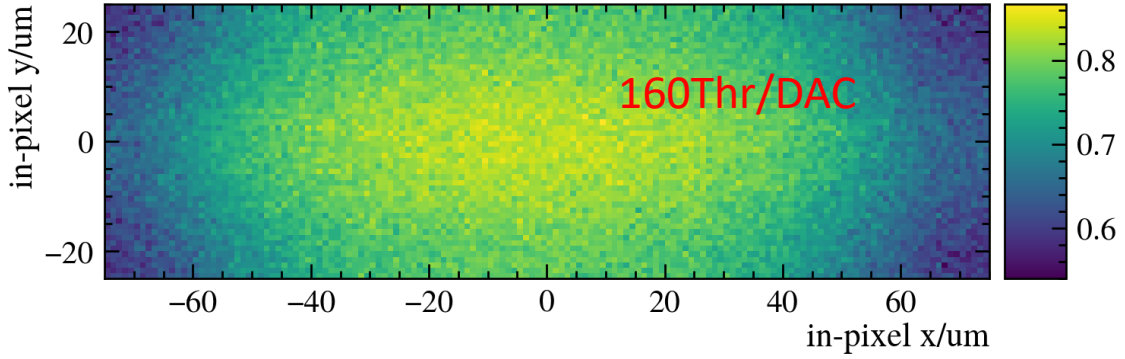
Max hit rate 17MHz/cm^2

The simulation of the MightyPix FSM readout efficiency.
Limited at the moment by statistics.
→ But even in simulation not 100% efficient, but close to it.

Single pixel Efficiency





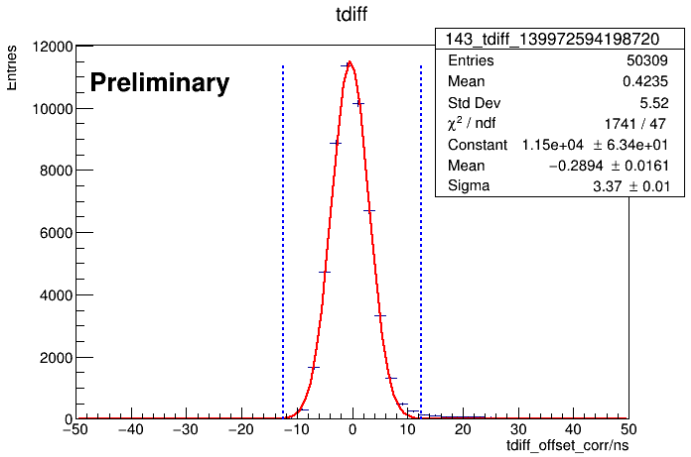


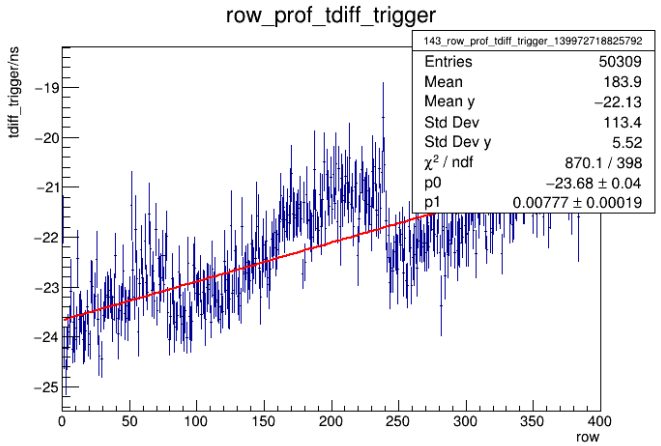
- Overlay of all pixels
- As expected first loosing the corners
- We know that a higher bias would compensate this (partially)
- Corners and short side loose the most charge due to charge shearing with neighboring pixels

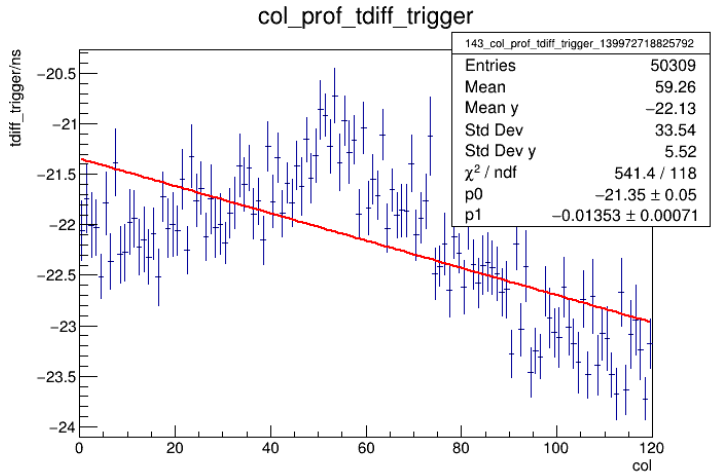
Time Resolution-Observations

Linear fit as guide (bin by bin correction is used)

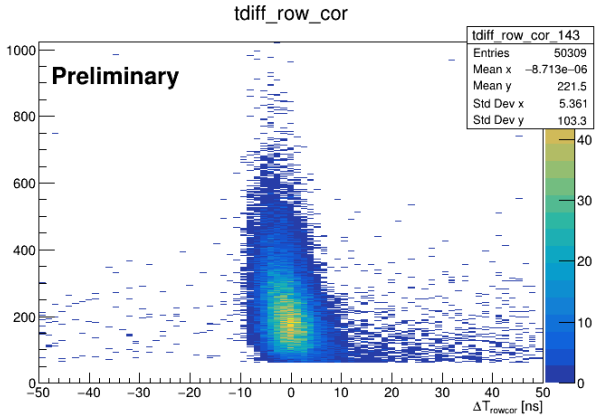
Before correction







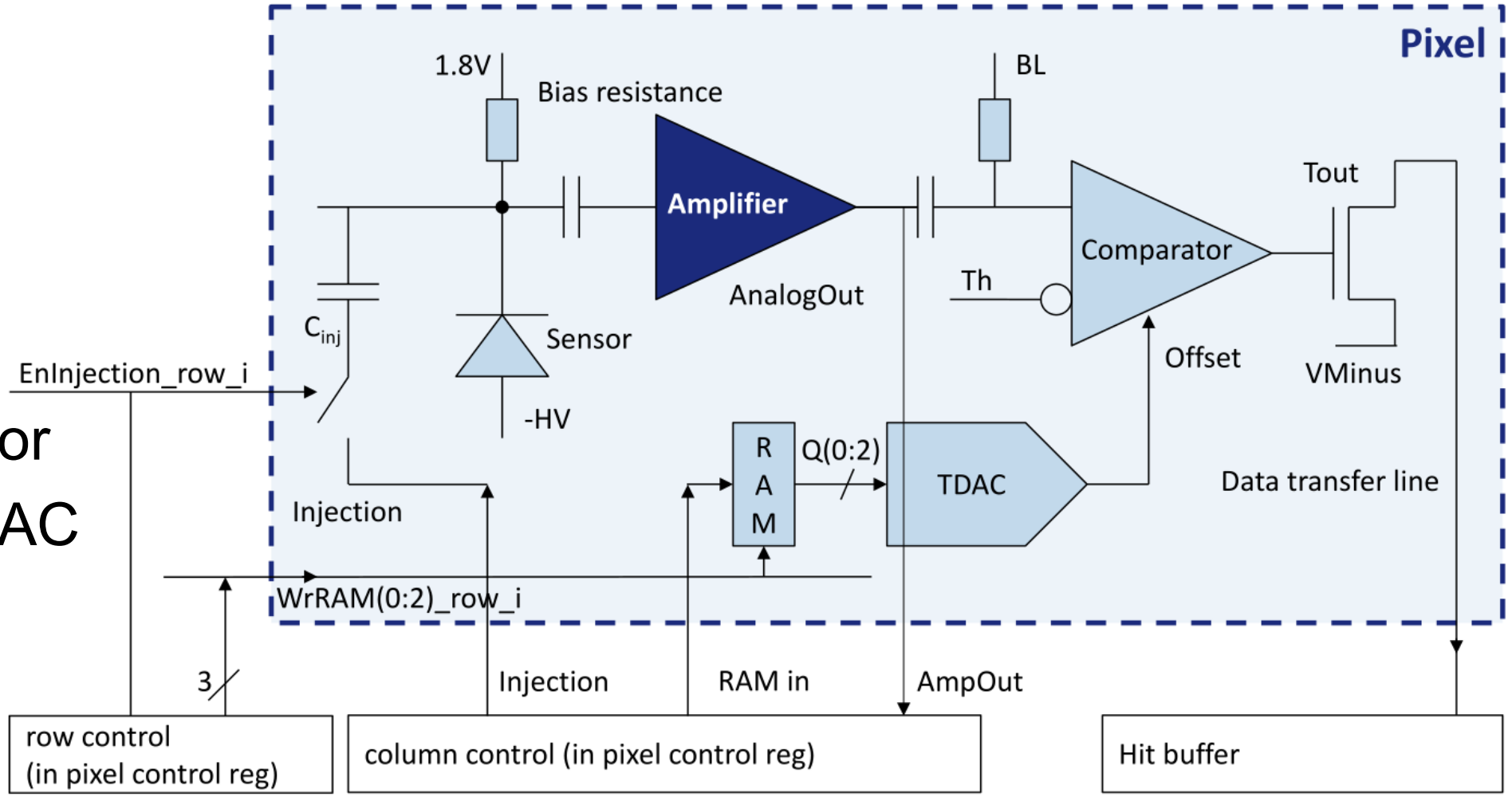
- Row dependence:
  - Linear dependence due to different capacitances expected
  - Observed structure due to different metal layers (3 used & 1 switch)
- Column dependence:
  - No clear structure expected
  - FSM located ~ col 60 → TS at edges are delayed
  - Asymmetry not understood
- ToT dependence:
  - Time walk effect expected & observed



Analogue Part

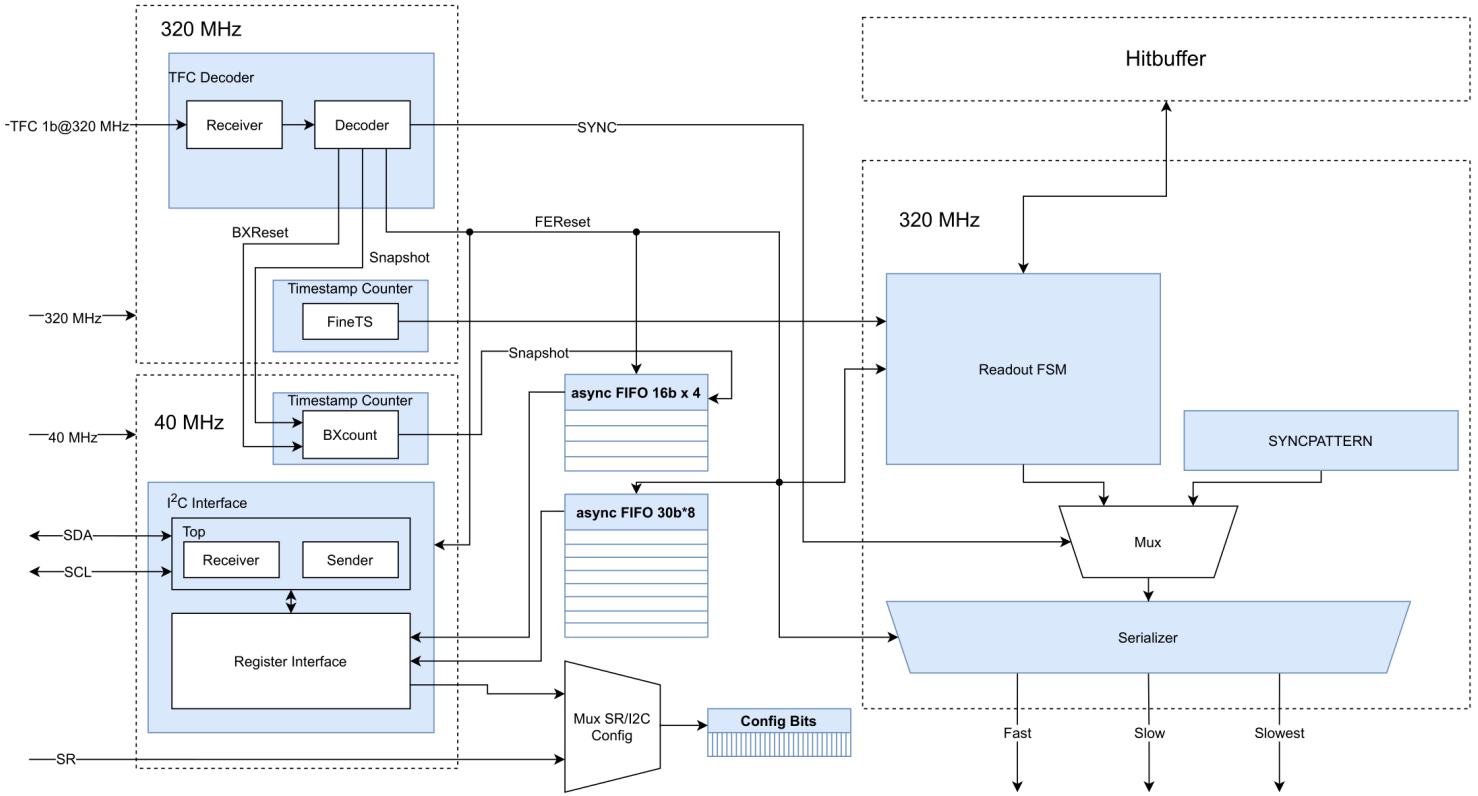
In Pixel:

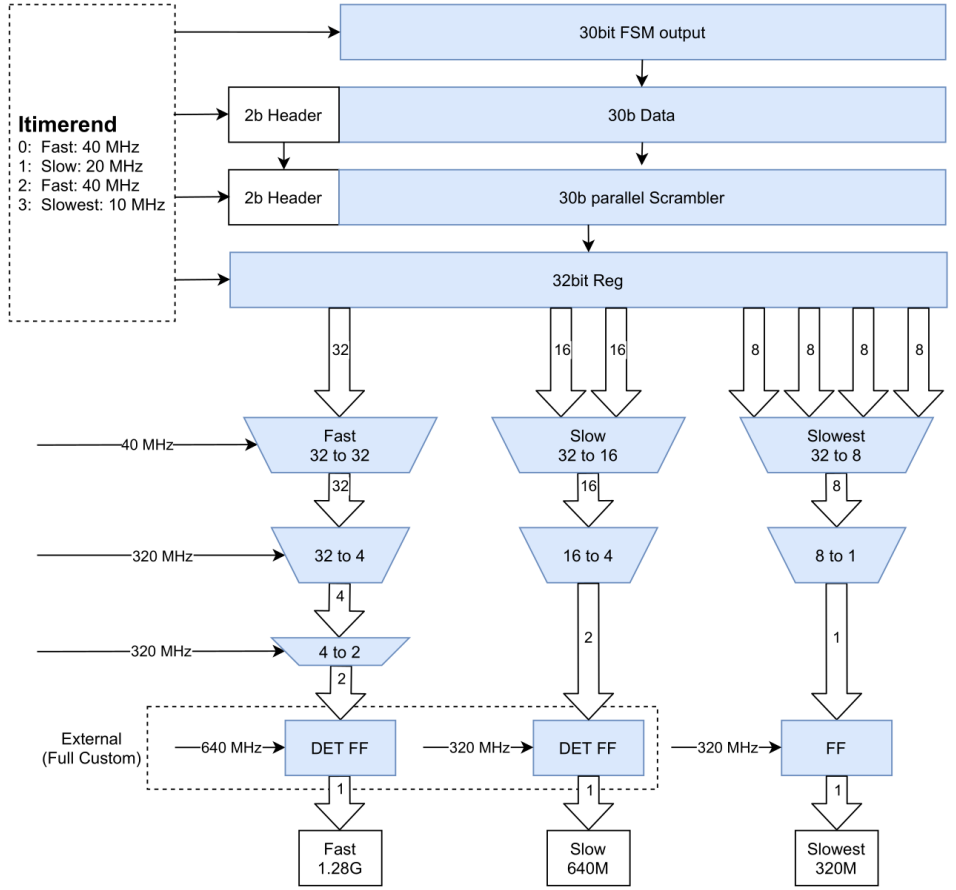
- Sensor diode
- CSA amplifier
- CMOS Comparator
- Threshold tune DAC
- RAM for tune bits



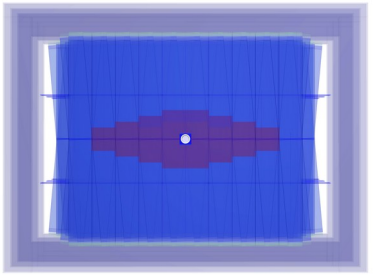
Source: Ivan Perić

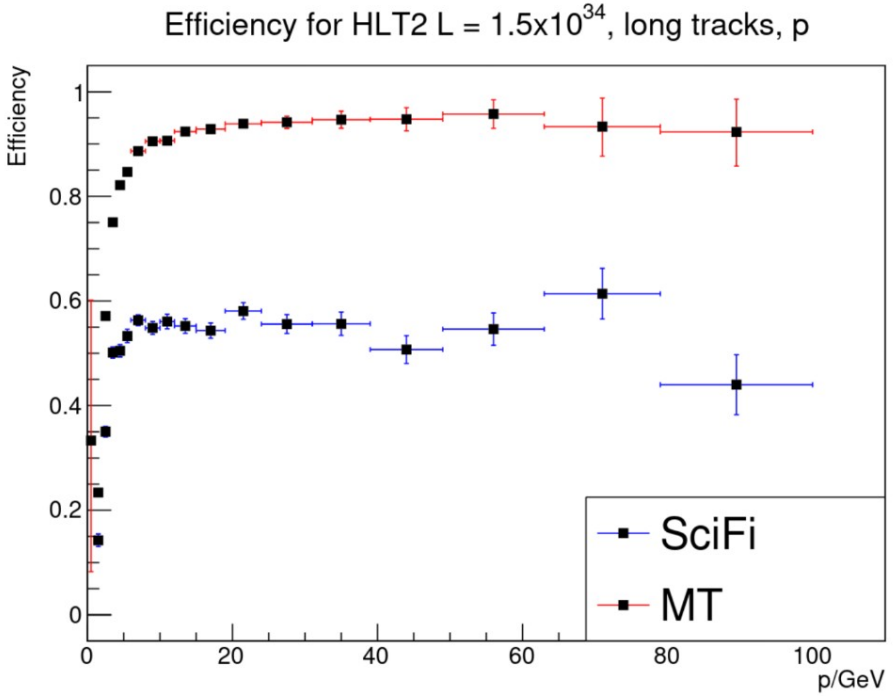
FSM and Serializer

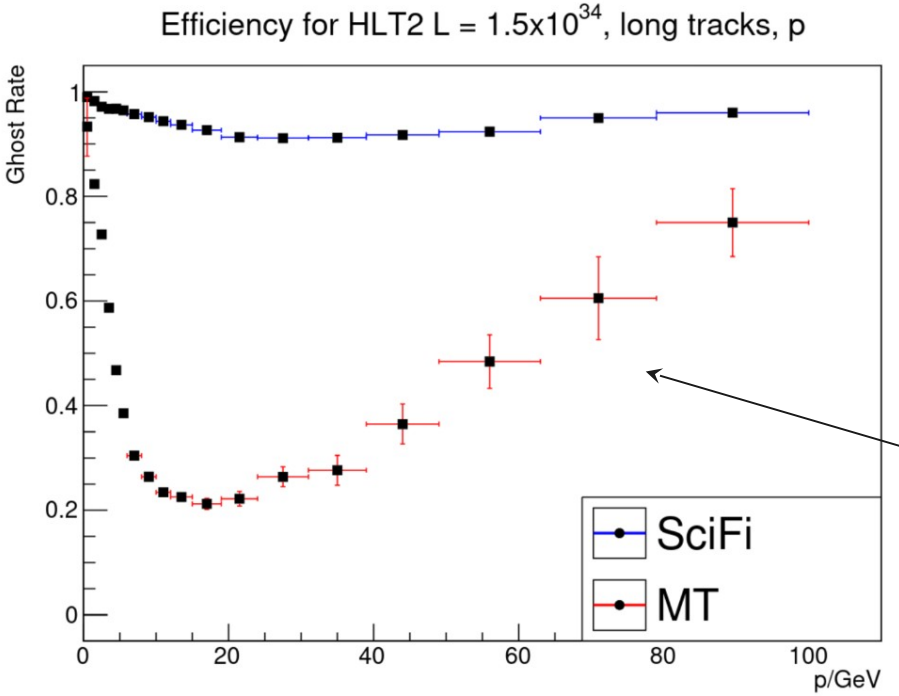




Beyond Occupancy:







This is where the pixel kicks in

LHCB-TDR-023

These plots are only looking at the SciFi part (Pixel not considered)

→ Need to reduce the fiber length to have a acceptable efficiency and ghost rate

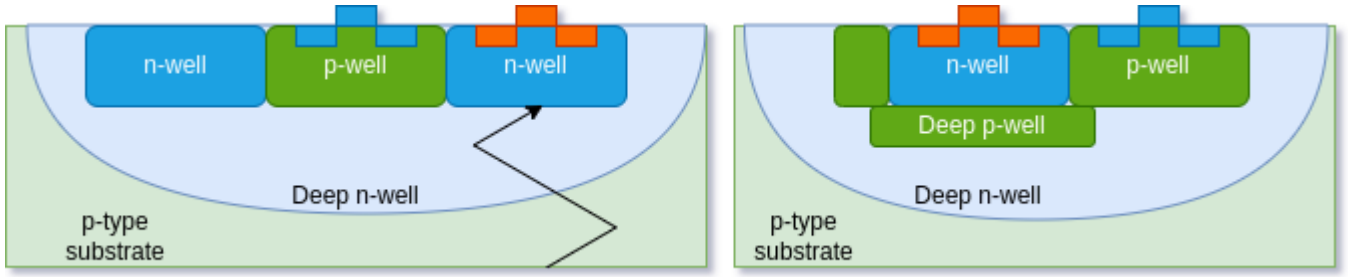
Preliminary studies show that the efficiency including the pixel are >98%

Testbeam with AtlasPix3.1

- AtlasPix3.1 is the closest full size chip of the HVCMOS family
- Amplifier and Comparator are different (no 3ns time resolution)
- Interest in the radiation hardness and stability of the time resolution

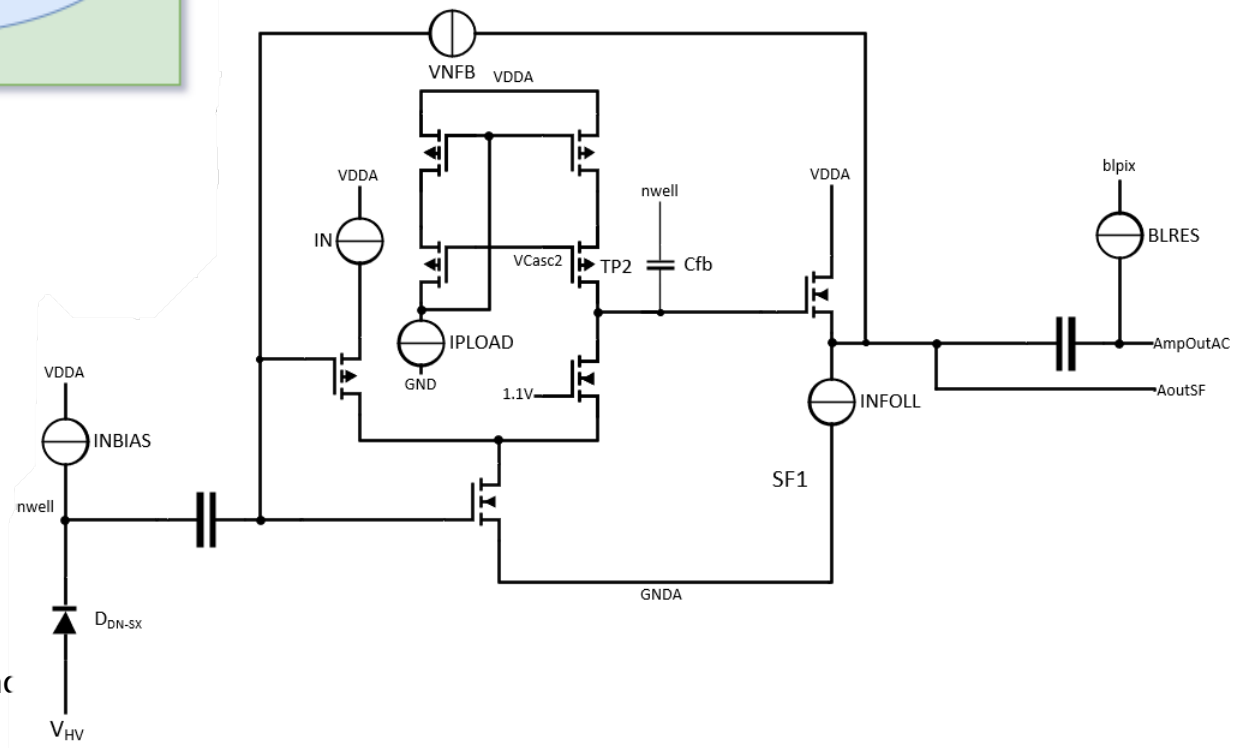
CMOS Amplifier/Comparator

New deep p-well enables the use of CMOS amplifier and comparator in the pixel cell



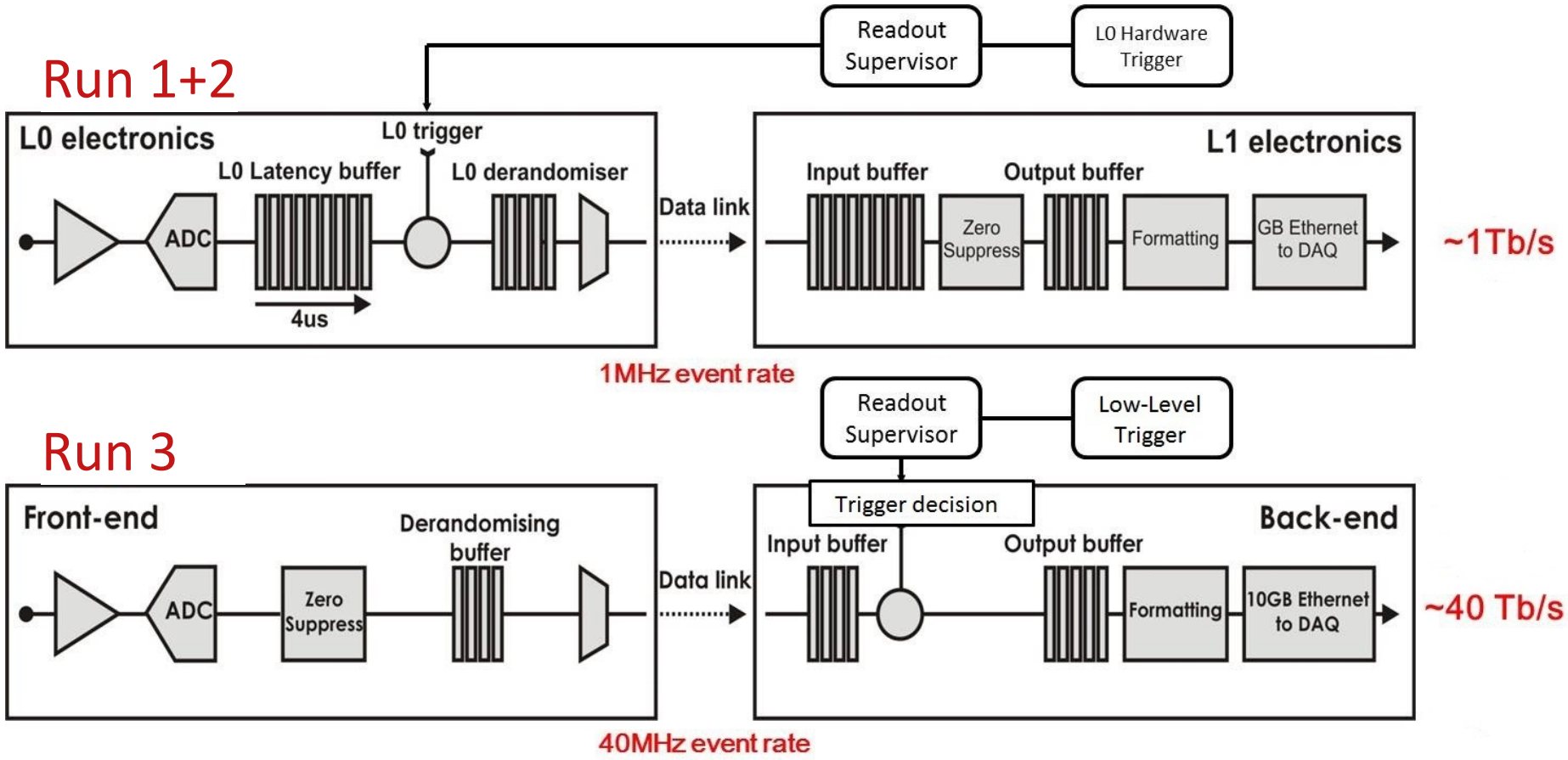
Old New

- CMOS style amplifier
- ENC: 67 e^- (88 fF pixel capacitance)
- Timewalk: 2.4 ns for signals from
- 2400 e^- to 24000 e^-



Klaas Pac

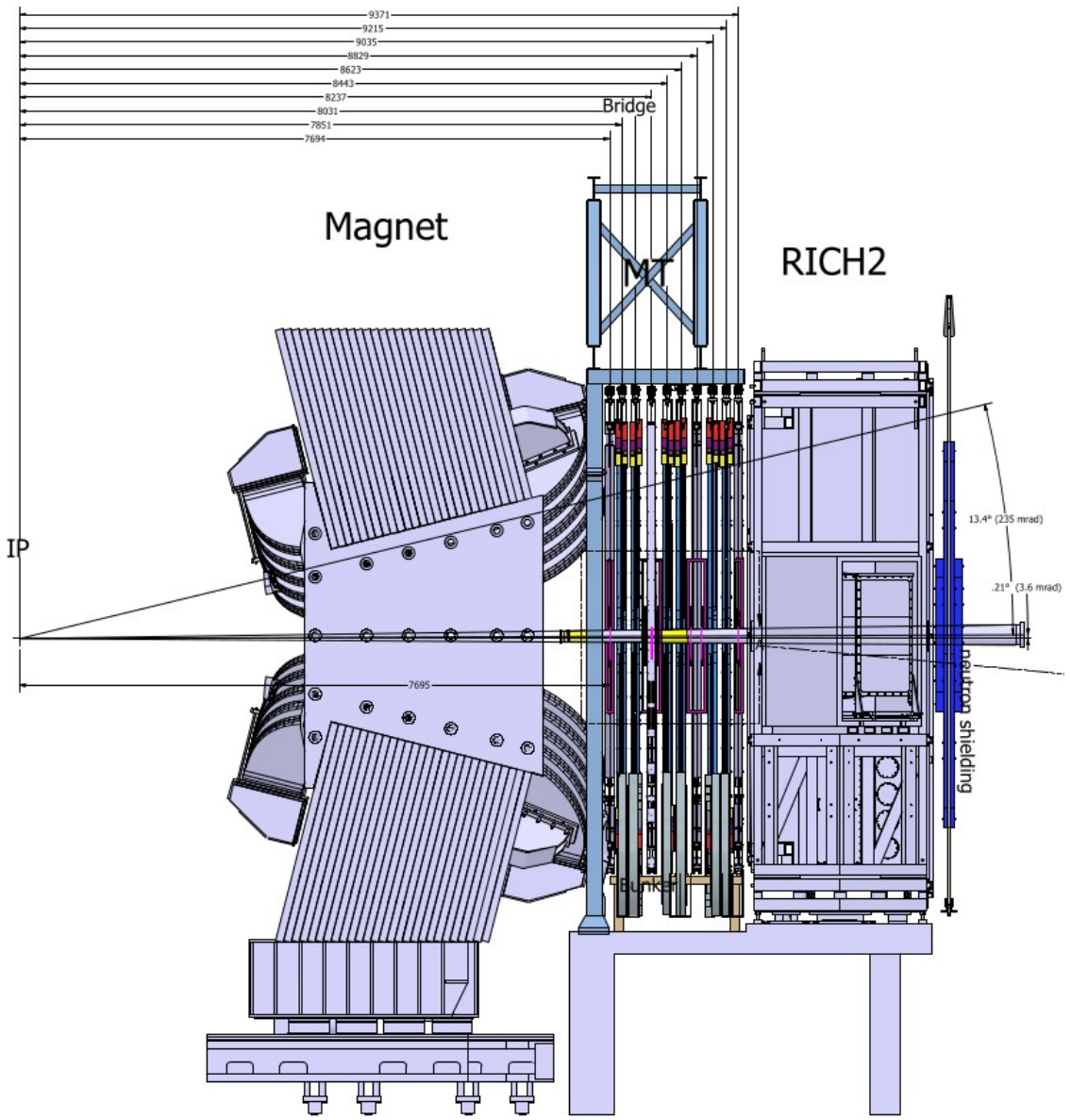
LHCb Upgade I → “Triggerless” readout



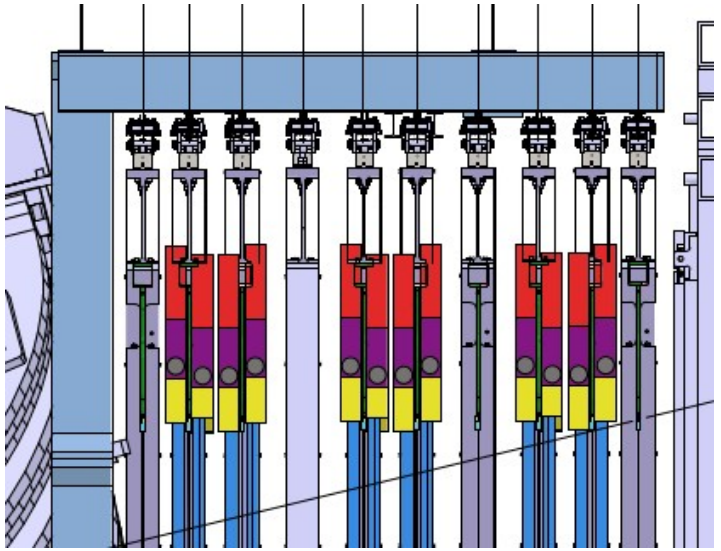
With a later High level Trigger more relevant data can be recorded!

F Alessio 2013 JINST 8 C12019

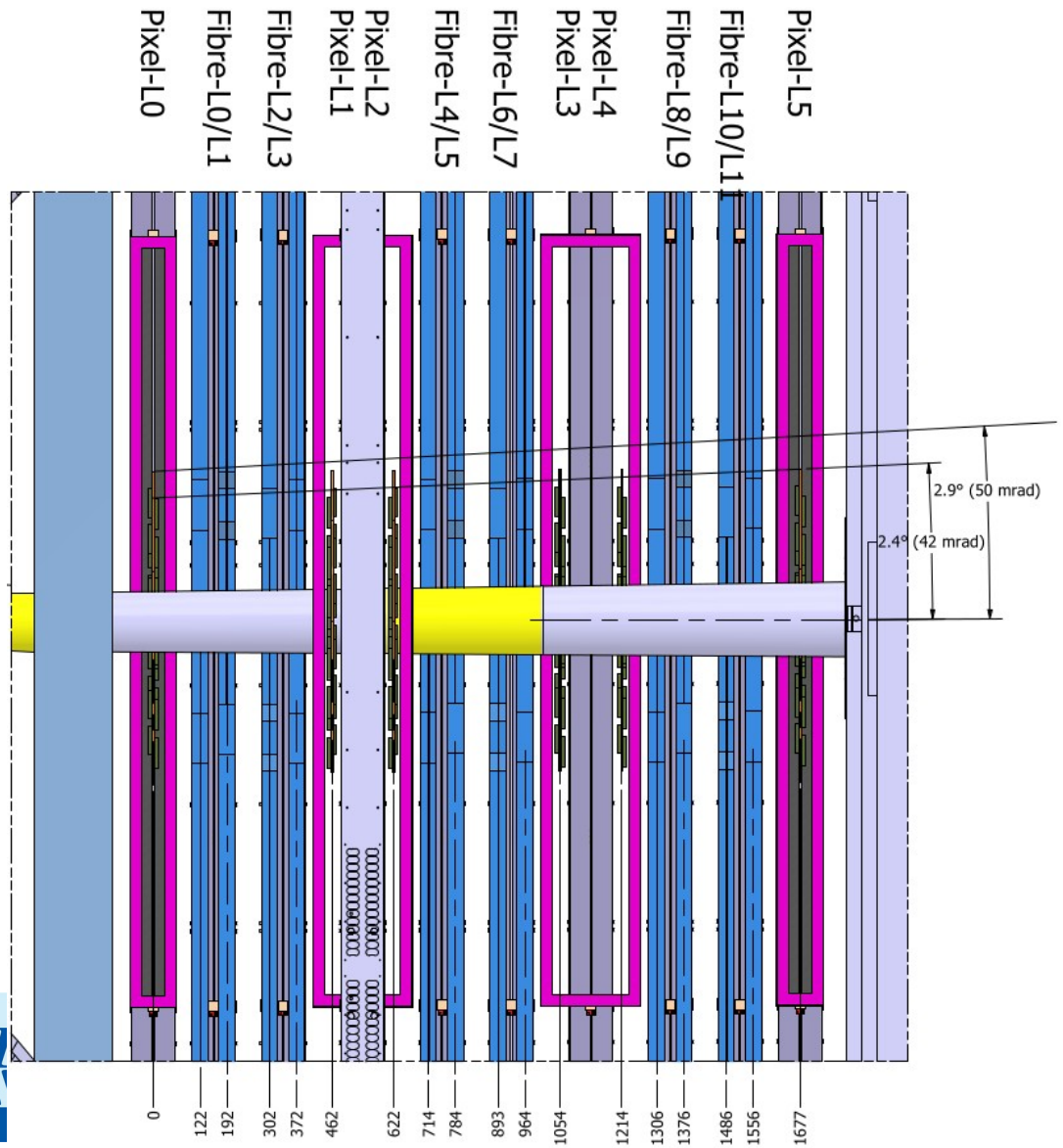
Cavern



- We have to move the current pillars
  - New Bridge (see Augusto's talk later)
- MT stays in the current envelope
  - Moving first layer under study at the moment
- No additional space close to the C-Frame

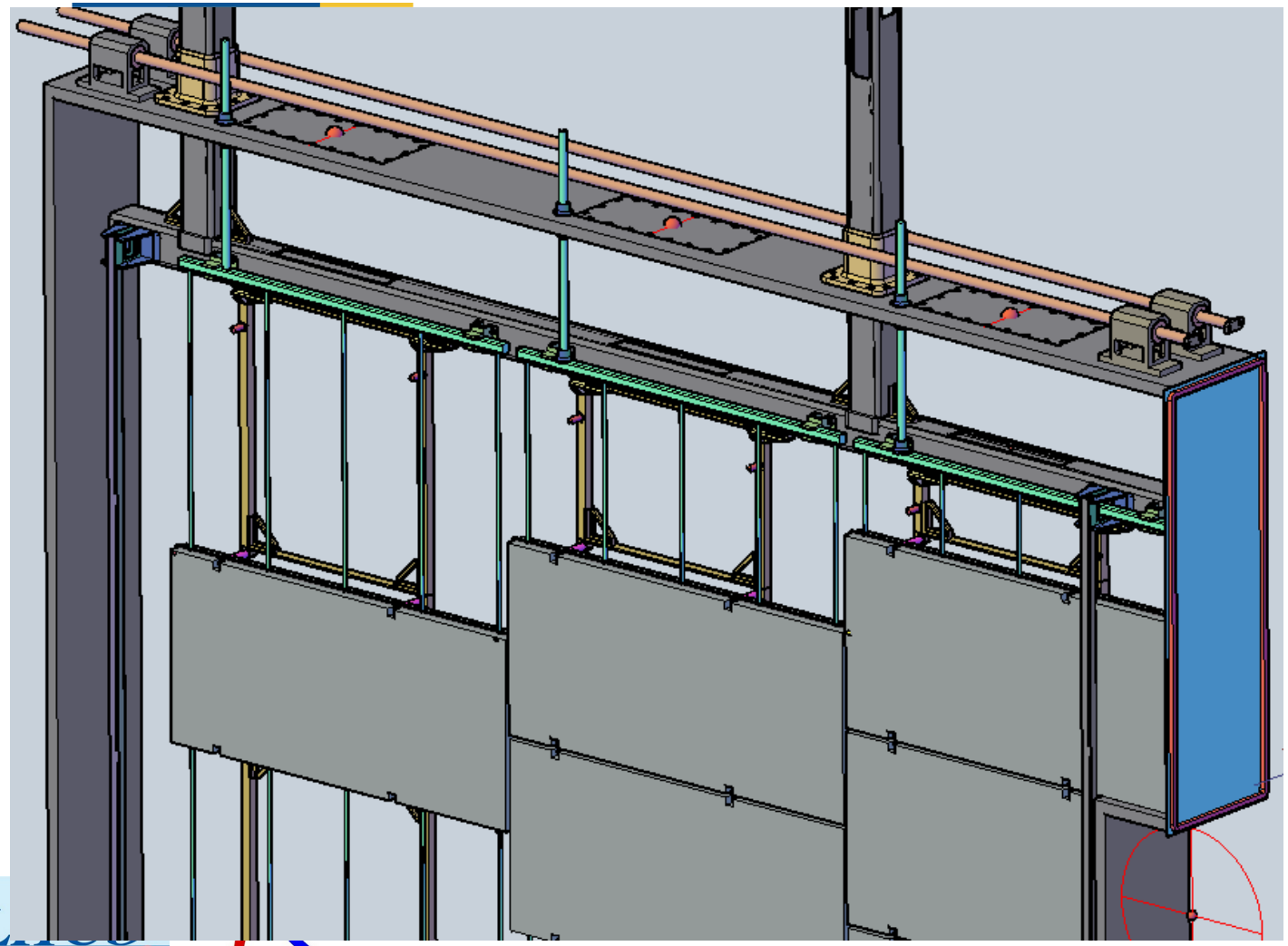


Cavern



- Pixel Layers grouped to safe insulation material (L0 and L5 stand alone)
- Pixel and Fiber separately movable

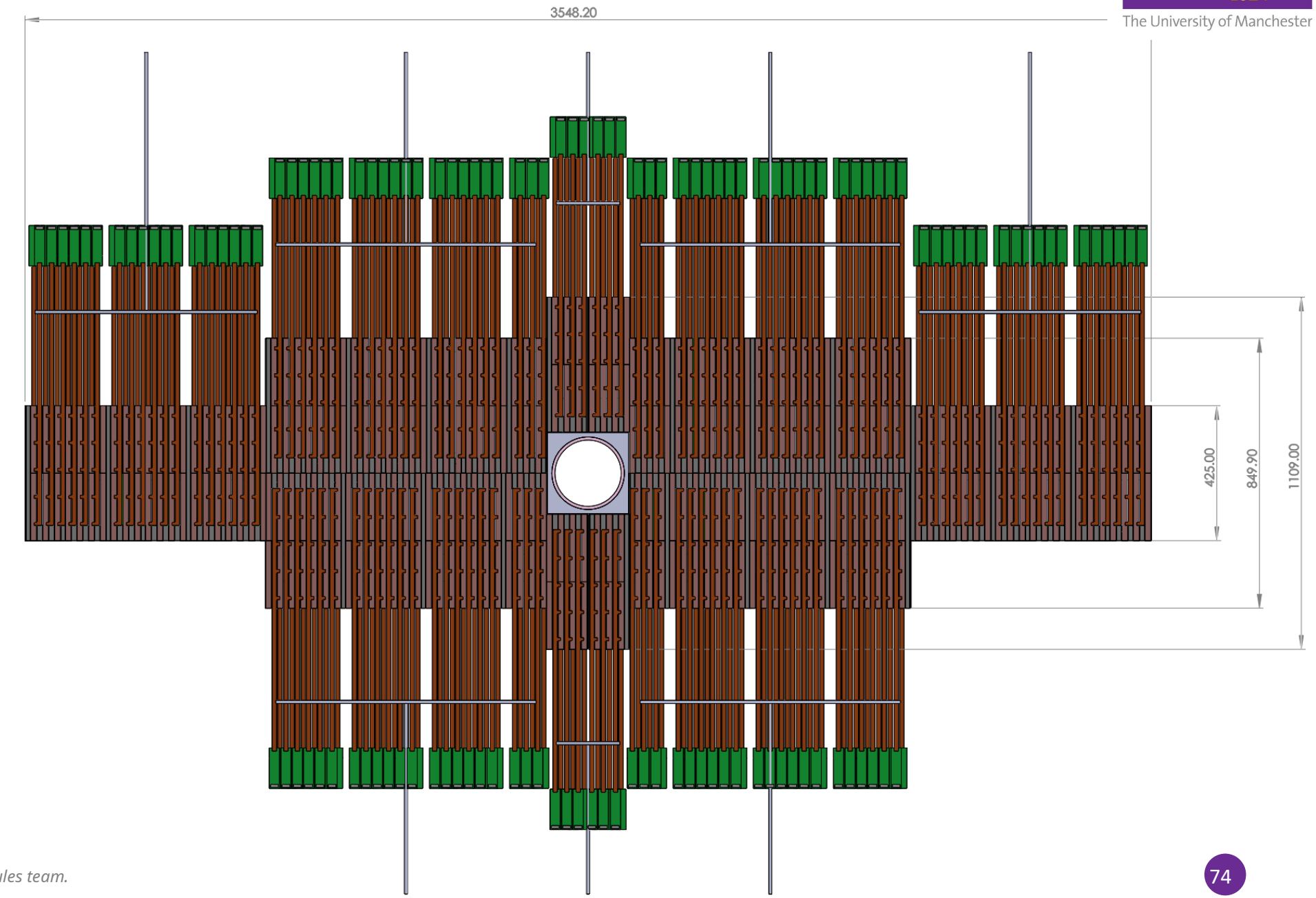
Box



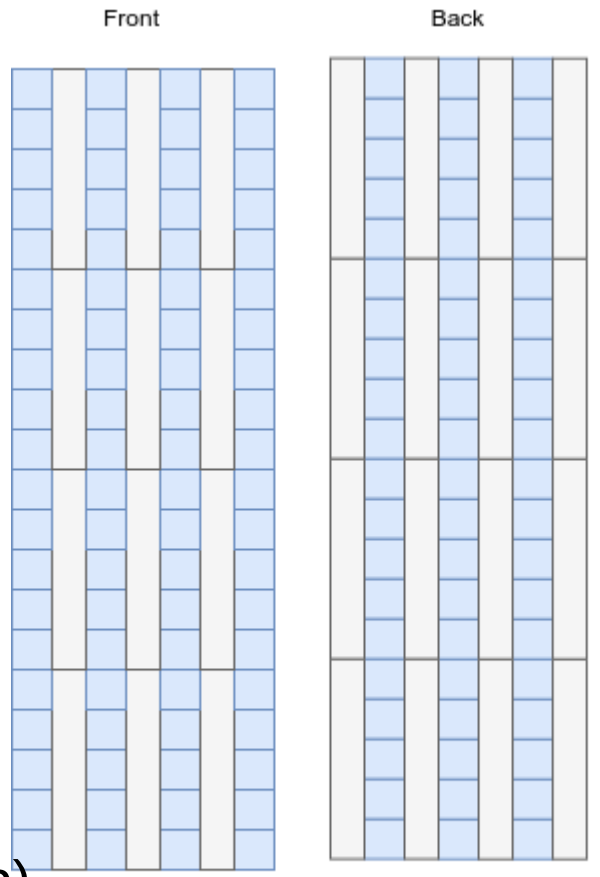
We have a pretty good idea how to do

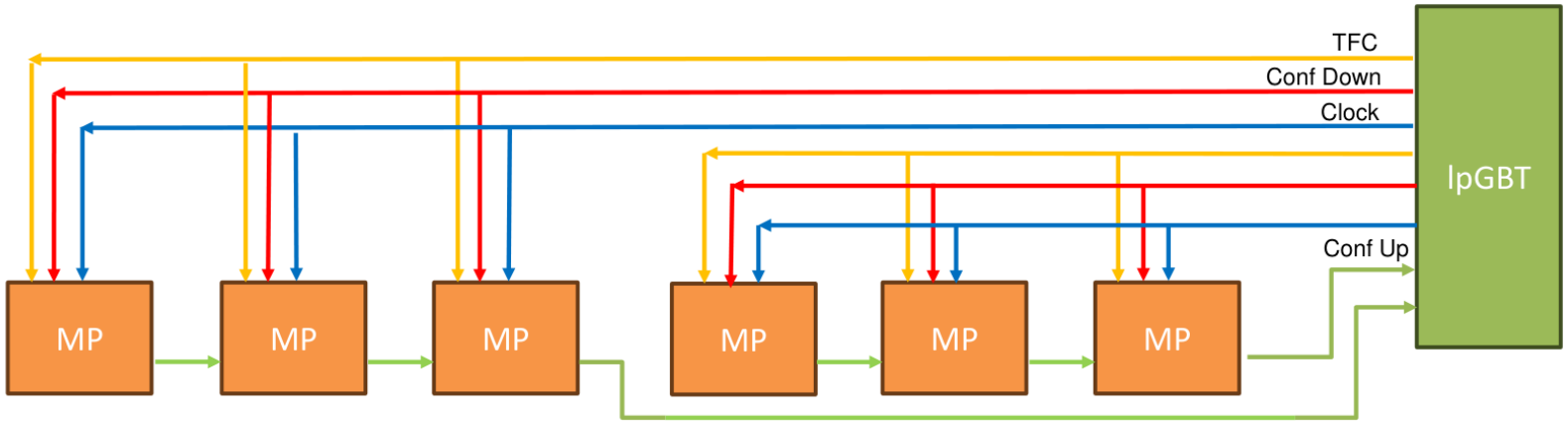
- Mounting
- Access
- Insulation
- Service Distribution
- Minimal adjustments for vertical modules
- See Trevor's Talk in Liverpool

- One module everywhere
- Will have symmetric services by alternating layer orientation
- No gap in x
- Only one central gap in the center at y=0 (2mm)
- “Baseline” for MP UP module discussions



Sensor Flex



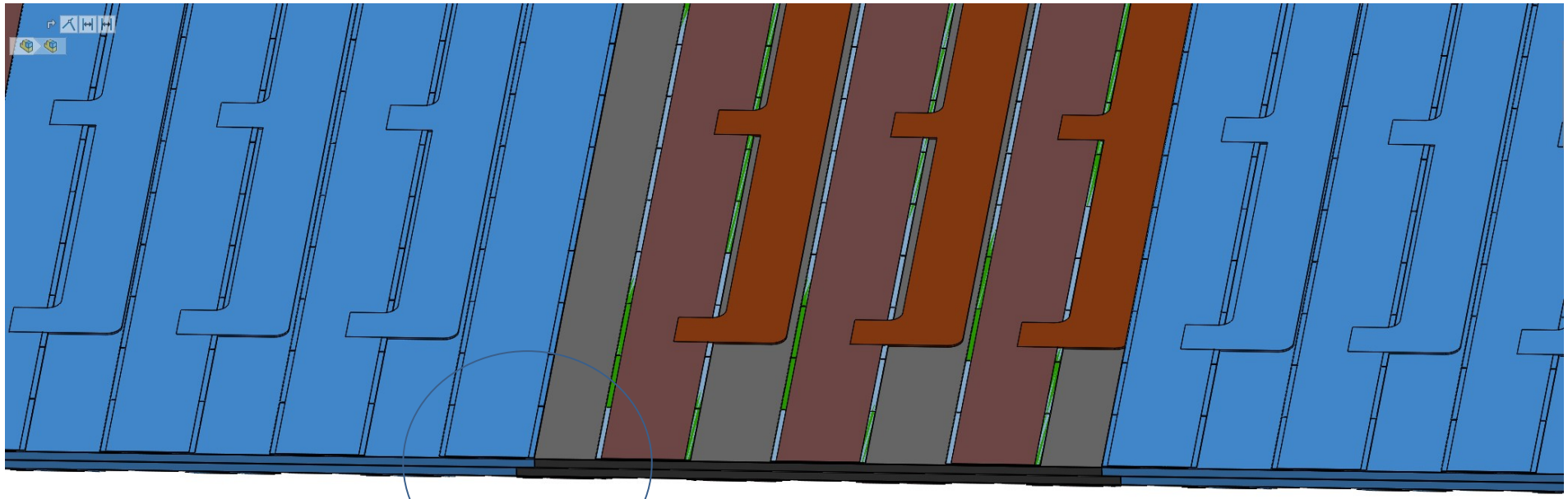


- 5 sensors would make one Sensor Flex (and configuration/clock group)
- Various data connections have to be possible (see Mike's last presentation)
- UP input maybe data concentrator chip for outer regions useful (less risk than integration into ASIC)
- Sensor connection and protection (Potting, thermal expention)
- Build with Au flex in mind we can use Cu as fallback
- 2 main options for HDI (lpGBT) position 50cm or 2.5m (probably a bit less due to space)

Specifications

Migthy-Pixel	
Pixel size (bending plane)	≦ 100 µm
Pixel size (non bending plane)	≦ 200 µm
Max. Particle Rate	17 MHz/cm²
Max. Hit Rate	34×10^{6} s^{-1} cm^{-2}
Max. length of data word	32
Overall efficiency	> 96%
In-time efficiency	> 99% within 25 ns
Noise rate (End of life)	≤ 400 kHz/cm²
Transmission rate	4 links of 1.28 Gbit/s each
NIEL	3×10^{14} neq/cm²
TID	40 MRad
Power Consumption	≤ 150 mW/cm²
MP Specification	< 200 µm

UP	
Pixel size in x	≦ 100 µm
Pixel size in y	≦ 100 µm
Max. Particle Rate	74 (34) MHz/cm²
Max. Hit Rate	150×10^{6} s^{-1} cm^{-2}
Max. length of data word	32
Overall efficiency	> 96%
In-time efficiency	> 99% within 25 ns
Noise rate (End of life)	≤ 400 kHz/cm²
Transmission rate	???
NIEL	3×10^{15} neq/cm²
TID	240 MRad
Power Consumption	≤ 300 mW/cm²
UP Specification	15



Remove all horizontal gaps between the modules
No easy solution for the vertical gap in the middle