High Speed Links for HEP

Versatile Link+ and the lpGBT

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Versatile Link+ Project

High-speed, radiation-tolerant optical links for (HL)-LHC experiments

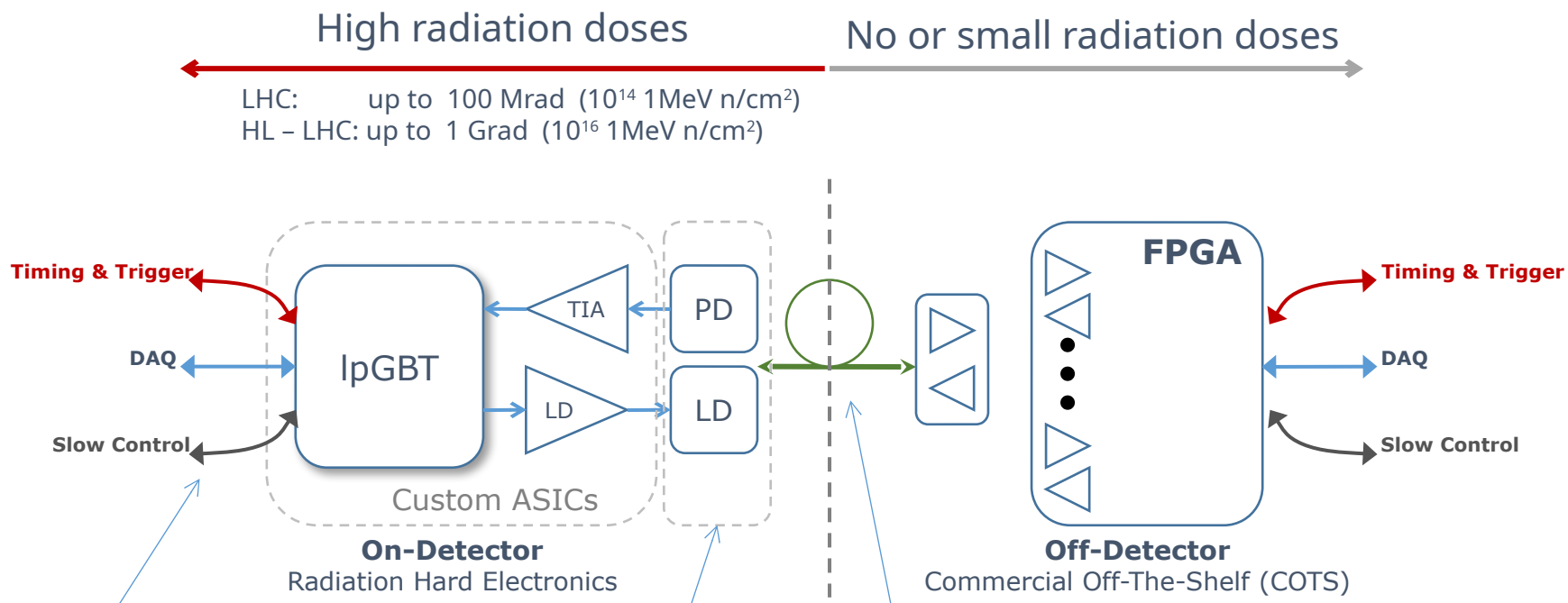
- Recurring challenge, similar needs in many detectors & experiments
- **Downlink (counting room to frontend):** Timing distribution, detector control, trigger distribution
- **Uplink (frontend to counting room):** Transport of acquired data for off-detector processing, storage, …

VL+ project: common development of ‘standardized’ link components

- Successor to Versatile Link project (GBTX, VTRx, …)
- One link for data plus TT&C (Timing, Trigger & Control)
- Project covers: rad-hard ASICs, front-end modules, passives, back-end support

Today: Introduction to VL+ links, focus on the lpGBT ASIC

Versatile Link+ Architecture



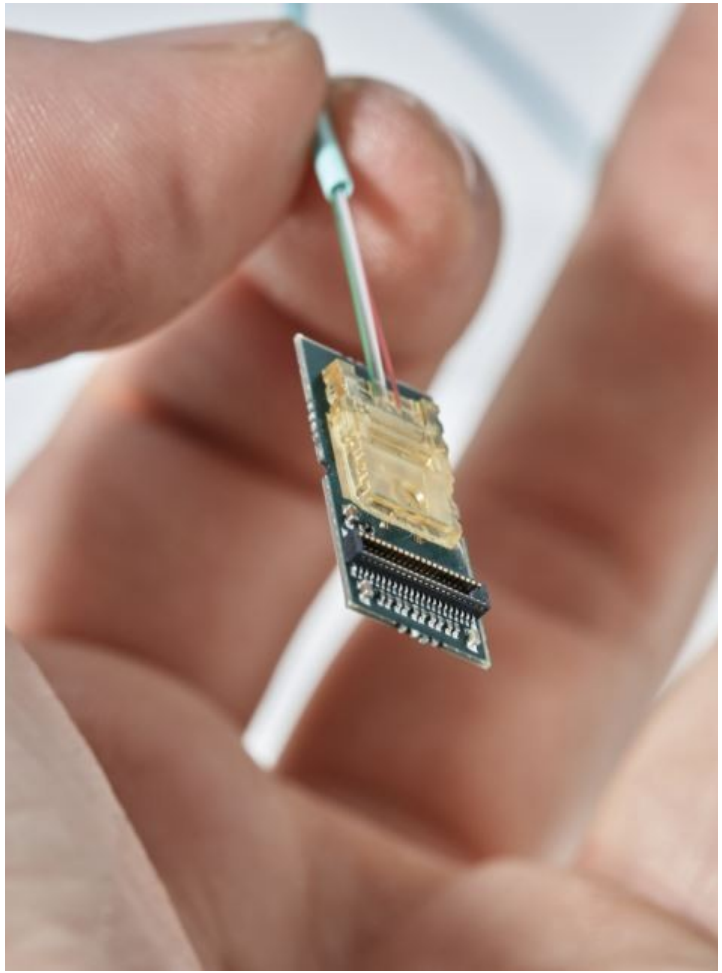
VTRx+ Optical Link Module

Off-the shelf optical modules (e.g. SFP, SFP+) not compatible with on-detector applications

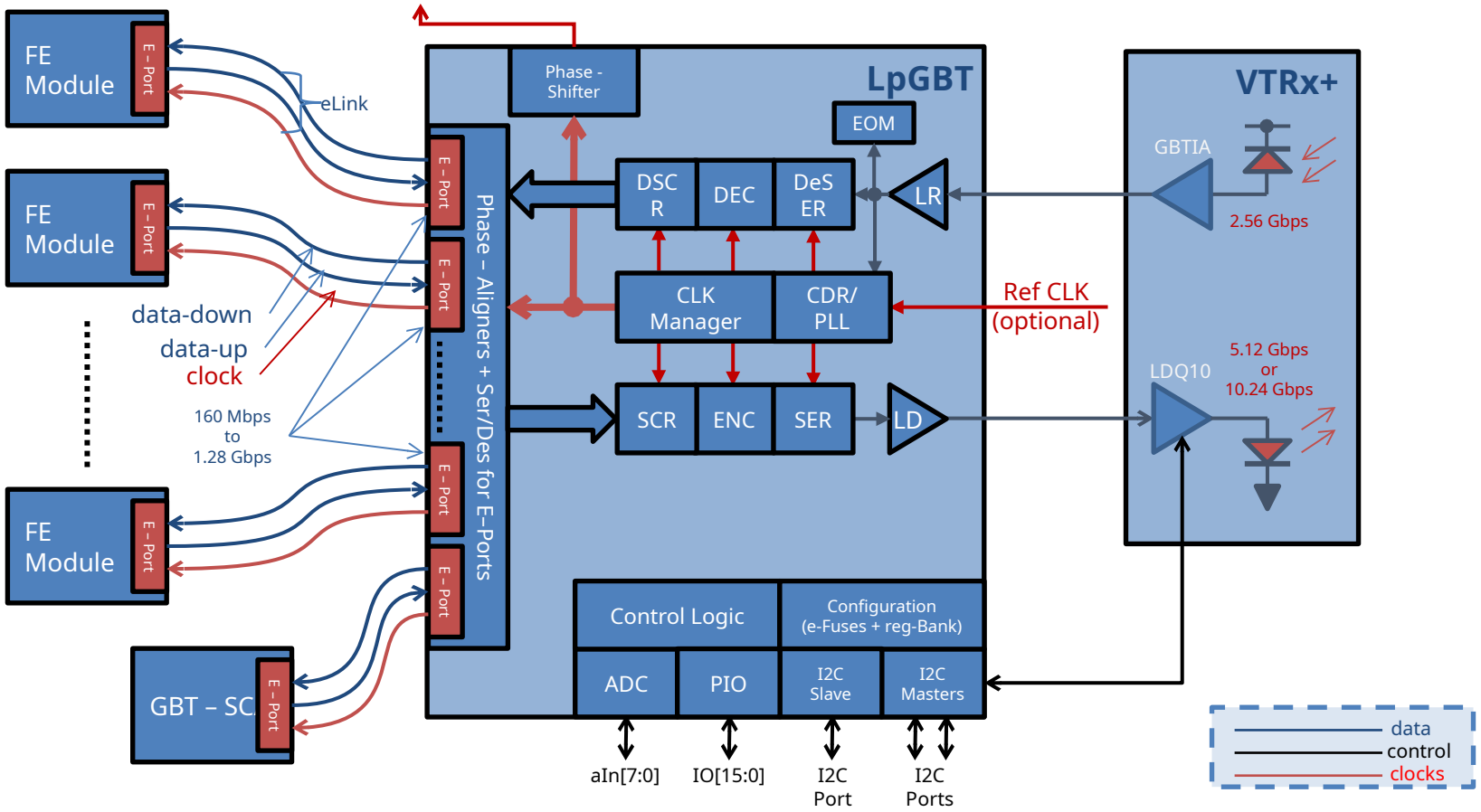
- Form factor, radiation tolerance

VTRX+: Custom Module - Key Specifications

- 850 nm multi-mode fiber, 4 (uplink) + 1 (downlink) channels, data rate compatible with lpGBT
- Miniaturized: 20x10x4 mm
- Pluggable: board-to-board connector (electrical), fiber pigtail
- Temperature range: –30 – 60°C
- TID: 1 MGy (100 Mrad), 10^{15} n/cm^2
- Electrical I/O compatible with lpGBT high-speed interfaces



lpGBT – Block Diagram Overview



lpGBT – Main Feature Set

High-speed links (back-end ↔ lpGBT)

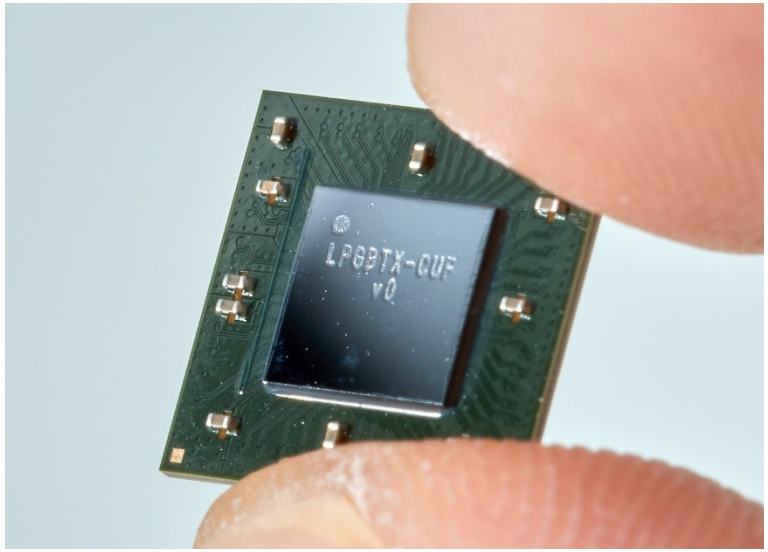
- Uplink: 5.12 or 10.24 Gb/s
- Downlink: 2.56 Gb/s

Electrical links (lpGBT ↔ front-end)

- Up to 28 (up) + 16 (down)links, 80 Mb/s - 1.28 Gb/s per link
- Phase alignment for data from front ends (automatic or manual)

Timing functionality

- Deterministic & fixed latency (for clocks & data, both directions)
- Frequency-programmable clock outputs (40 MHz – 1.28 GHz)
- Phase- and frequency-programmable clock outputs (50 ps step size)
- Low jitter (<5 ps rms)



Pin count: 289 (17 x 17)
Pitch: 0.5 mm
Size: 9 mm x 9 mm x 1.25 mm

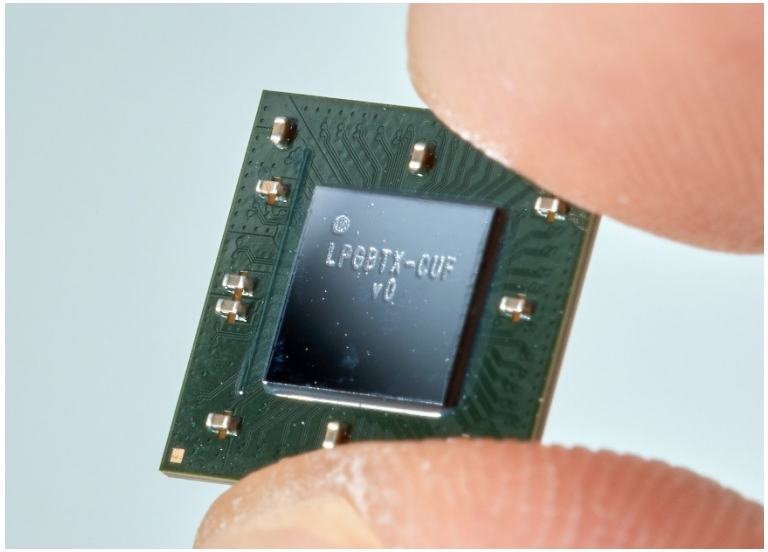
lpGBT – Main Feature Set

Experiment Monitoring & Control

- 3x I2C masters, 16 CMOS GPIOs
- Factory-calibrated analog subsystem (ADC, DAC, Reference)
- Extensible using external slow control ASIC (GBT-SCA)

Configuration

- Power-Up State Machine, Automated ROM start-up, Watchdog, BOR, …
- User configuration via optical link, I^2C or serial control channel
- READY & RESET signal generation for downstream ASICs



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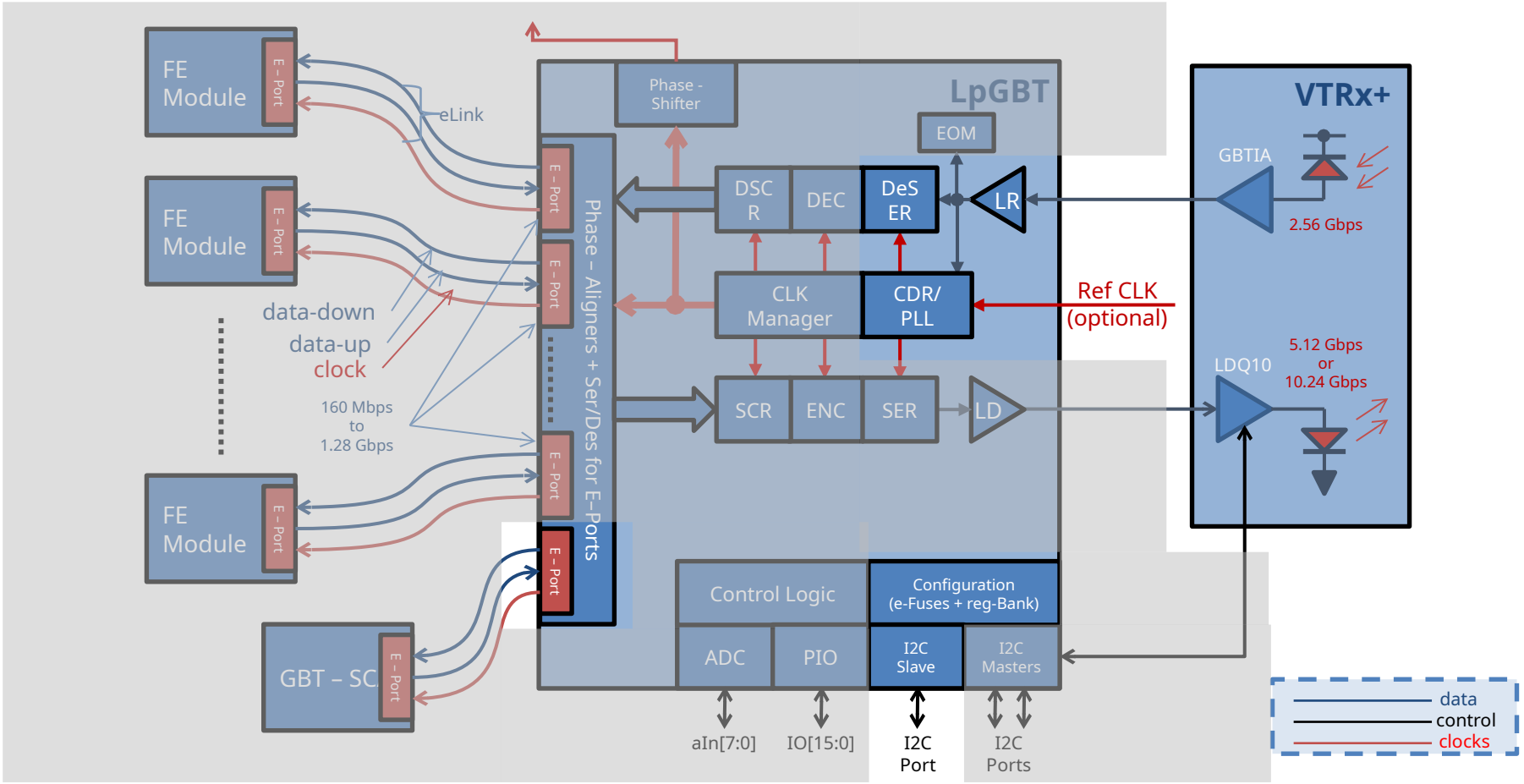


Configuration

Highly configurable ASIC

- Mode of operation (TX/RX/TRX), uplink data rate, FEC options, number/data rate of active electrical links, data phase aligner mode, number/frequency/phase of active clock outputs, PLL/CDR, DLLs, startup procedure, watchdogs, …

11 configuration pins, 320 registers need to be taken care of

- Configuration pins set the basic mode of operation, enough to establish communications
- Registers are used to customize behavior to a given application

Configuration is necessary, not optional!

Configuration

Key modes of operation

- Simplex Receiver (RX): High-speed downlink (2.56 Gb/s), electrical link transmitters – unidirectional data transmission
- Simplex Transmitter (TX): electrical link receivers, high-speed uplink (5.12/10.24 Gb/s) – unidirectional data transmission
- Transceiver (TRX): bidirectional eLinks, high-speed up- & downlink active

Timing reference depends on mode of operation

- Simplex RX & TRX: Clock recovered from high-speed downlink data
- Simplex TX: 40 MHz reference clock required (e.g. from another lpGBT)

Configuration

Three configuration ‘channels’ are available

- I^2C slave port – available in all modes (address: set by configuration pins)
- IC (internal control) channel via HS downlink – only available in TRX mode
- EC (external control) channel via dedicated ePort – only in simplex RX and TX mode

Previously, eFuses were also available to store the configuration

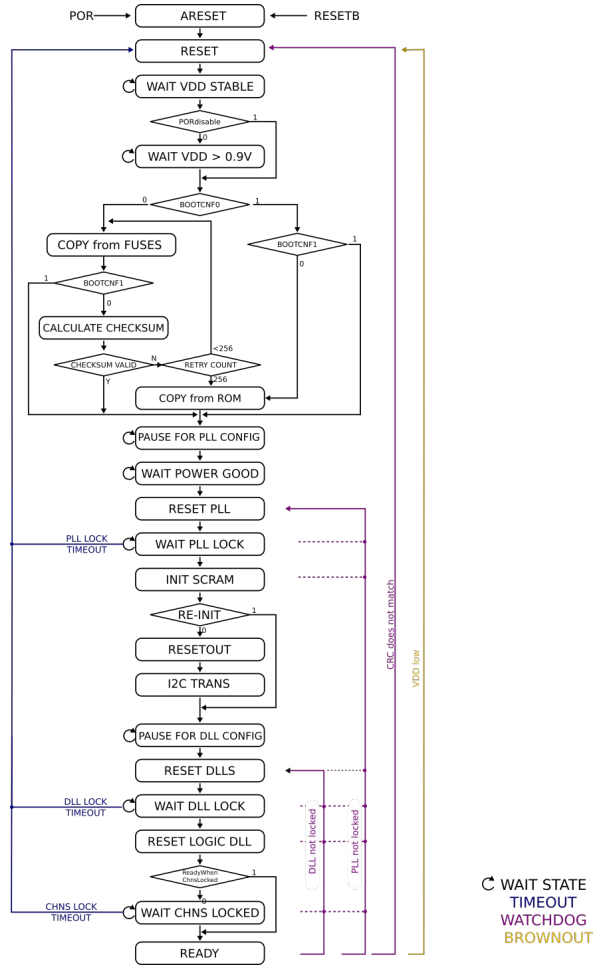
- Were found to be unreliable – strong recommendation not to use them!

Power-up State Machine

Dedicated power-up state machine (PUSM) coordinates start-up

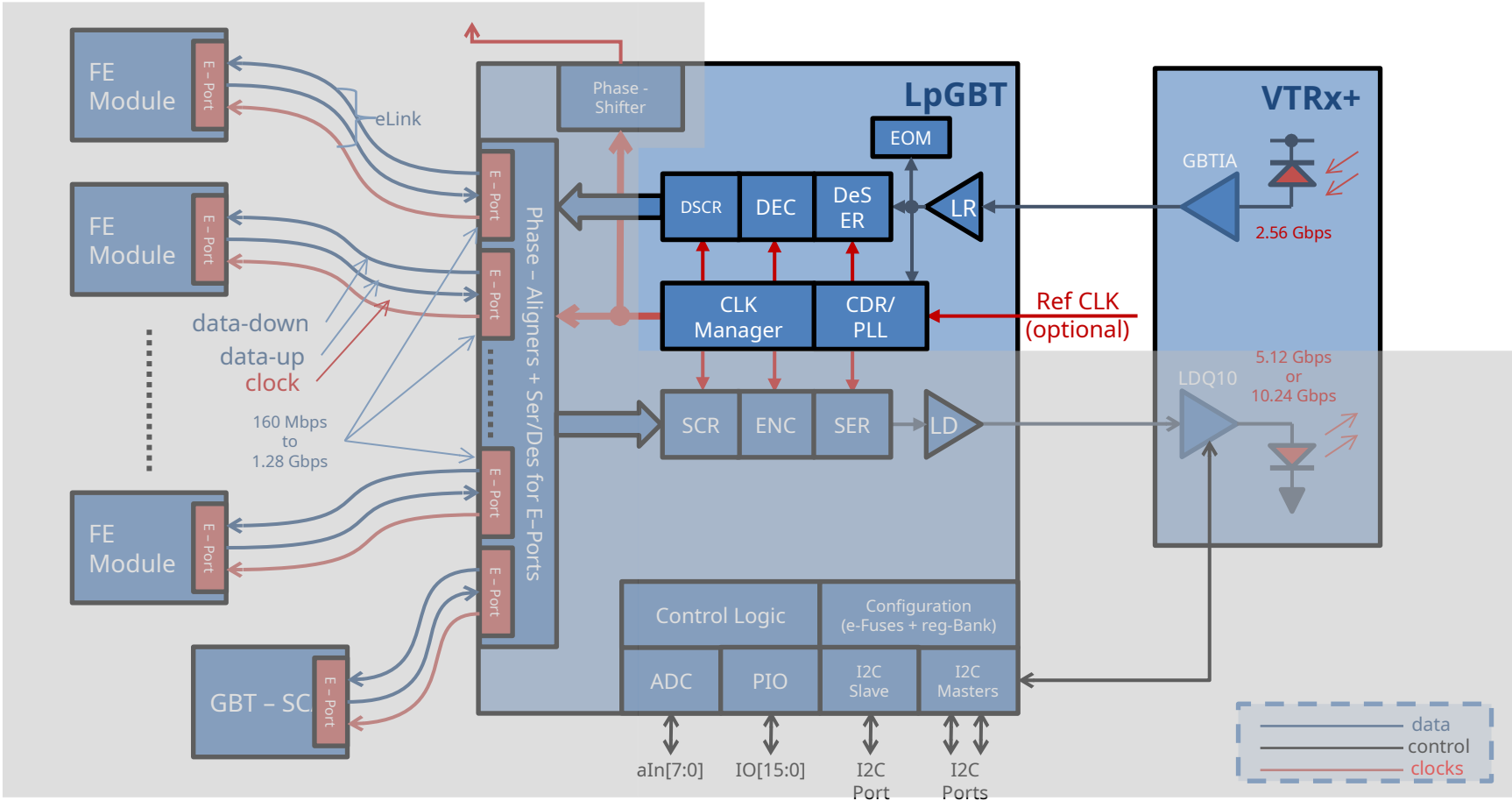
- Establishes stable supply voltage
- (If requested) loads configuration from ROM/eFuses
- Initializes PLL, CDR & DLLs correctly - as soon as user has completed their configuration
- If OK, asserts “READY” pin to signal correct operation
    - At this point, downlink & uplink are established and user data is being transmitted

Robustly designed, automatically recovers from abnormal situations during/after startup



PUSM State Diagram

High-Speed Downlink & Data Path



High Speed Downlink & Data Path

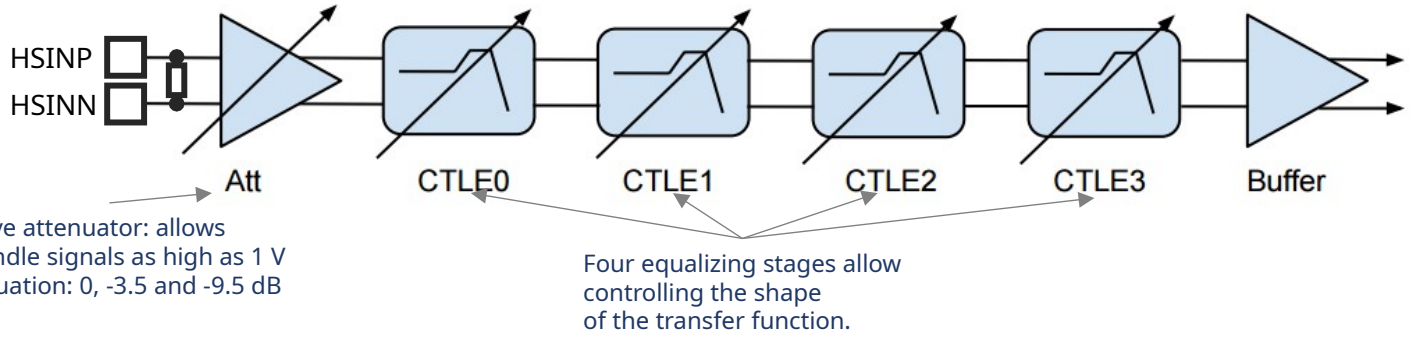
VTRx+ performs O/E conversion of 2.56 Gb/s downlink signal

- Electrical signal enters lpGBT line receiver
- Signal conditioning: equalization, clock & data recovery (CDR)
- Data path: Deserializer, frame aligner, deinterleaver, FEC decoder, descrambler
  - Details can be omitted - these are ‘transparently’ handled by the lpGBT FPGA firmware

Downlink frame: 64 bits @ 2.56 Gb/s = 25 ns long

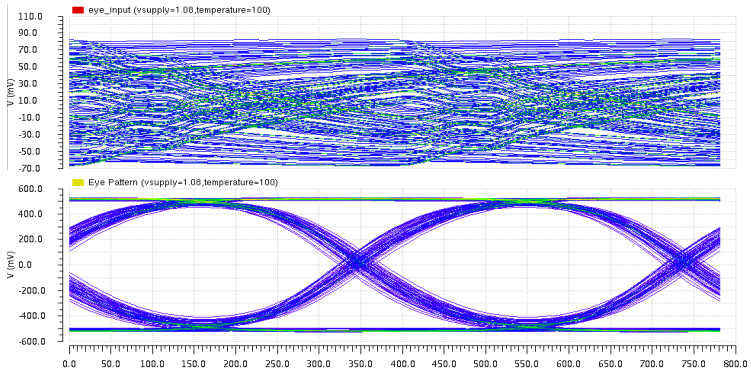
- Fixed frame header is used to synchronize the lpGBT’s internal 40 MHz clock
- All clocks are derived from this reference → deterministic latency

High Speed Downlink & Data Path



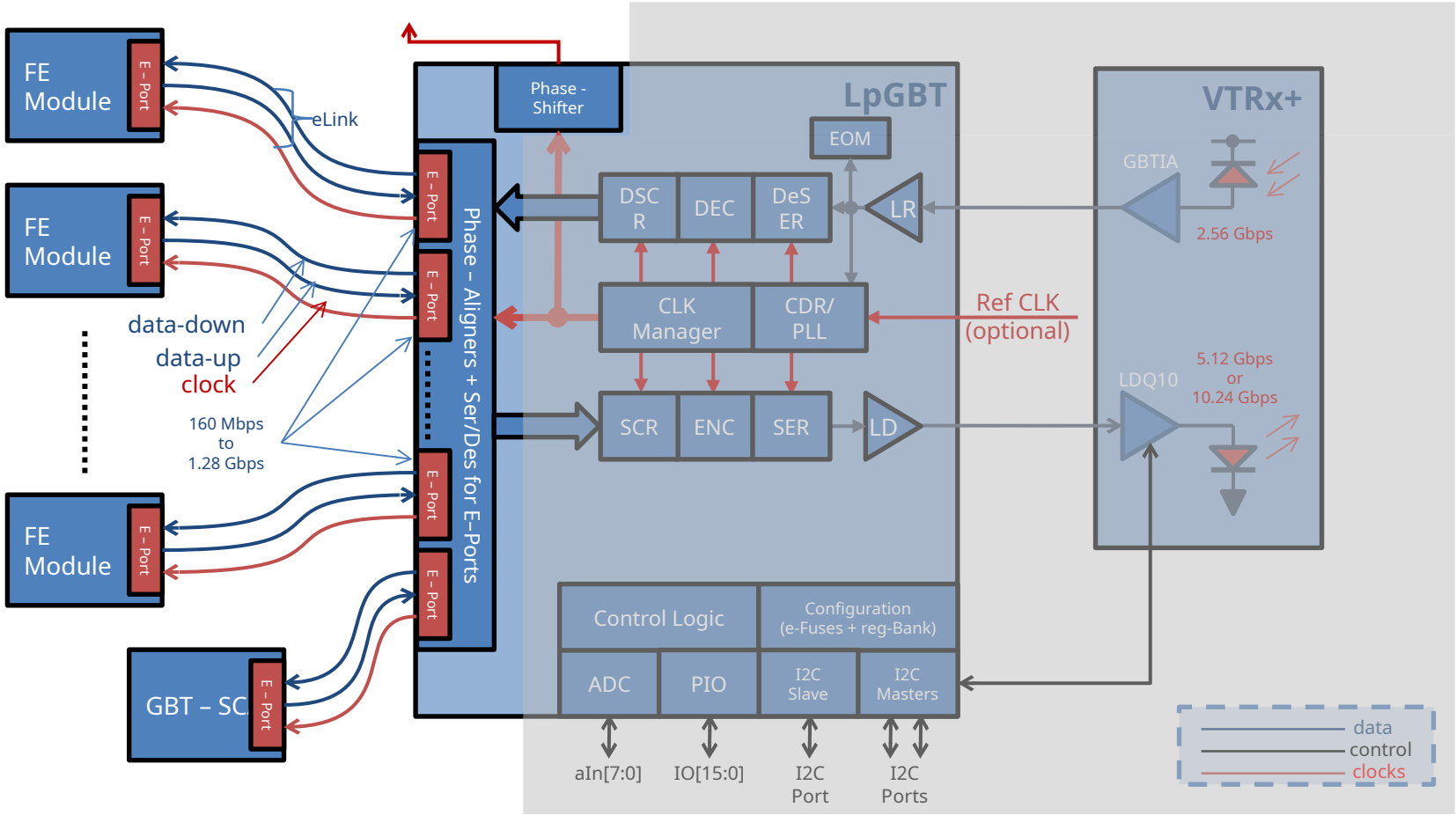
lpGBT includes a downlink equalizer

- To be used when downlink needs to pass a bandwith-limited channel
- Multi-stage design, allows setting poles/zeros to obtain best possible eye diagram
- Receiver eye can be monitored & adjusted using built-in “eye opening monitor”



Example: Equalization of Low Bandwidth Coaxial Cable

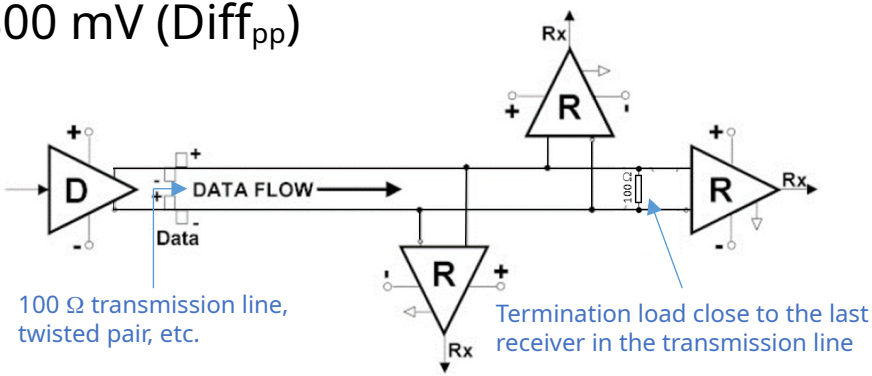
Electrical Front-End Links



Electrical Front-End Links

Electrical ‘standard’: CERN Low Power Signalling (CLPS)

- 100 Ω load impedance, point-to-point and multi-drop configurations
- Maximum data rate: 1.28 Gb/s
- Maximum clock frequency: 1.28 GHz
- Signal amplitude: 100 – 400 mV (SE_{pp}) / 200 – 800 mV ($Diff_{pp}$)
- Common mode: 600 mV (nominal)
- Built-in 100 Ω RX termination available



Electrical Front-End Links – ePorts

Electrical link building blocks in the lpGBT: ePorts – consisting of

- ePortTx: Transmitter link (lpGBT to frontend), 80 Mb/s – 320 Mb/s
- ePortRx: Receiver link (frontend to lpGBT), 160 Mb/s – 1280 Mb/s
- eClock: Frequency-programmable clock (lpGBT to frontend), 40 – 1280 MHz

Data is transmitted & sampled synchronously with the clock

- Only phase alignment required on receiving end of each link
- Flexible choice of data rate/frequency allows using source-synchronous links (e.g. SDR/DDR) or frontends with CDRs/PLLs

Electrical Front-End Links – ePortTx

Latency determinism drives layout of the data path

- Each bit transmitted across an eLink belongs to a specific bit in the downlink frame (frame is synchronous to bunch clock)

Segmented into groups of four links each: ePortTxGroups

- Data rate is set per group (80, 160, 320 Mb/s)
- Number of links in a group depends on the data rate
- ‘Mirror’ functionality can replicate data on ‘unused’ ePortTx

One extra link: EC output (80 Mb/s)

- Used for experiment control or lpGBT configuration

Output eLinks (downlink)			
Data rate (Mb/s)	80	160	320
Maximum number	16	8	4

Electrical Front-End Links – eClocks

Total of 29 eClocks available

- Fixed (deterministic) phase
- Frequencies: 40, 80, 160, 320, 640, 1280 MHz

Four additional phase-programmable clocks available

- Fully independent, same frequency range as eClocks
- Phase shifting: Coarse (781.5 ps) and fine (48.8 ps) phase shift resolution
- Can be shifted up to 25 ns (= one full 40 MHz period)
- *Note: If fine phase shifting is required, corresponding DLLs must be initialized!*

Same driving strength, preemphasis, polarity control available as for ePortTx

Electrical Front-End Links – ePortRx

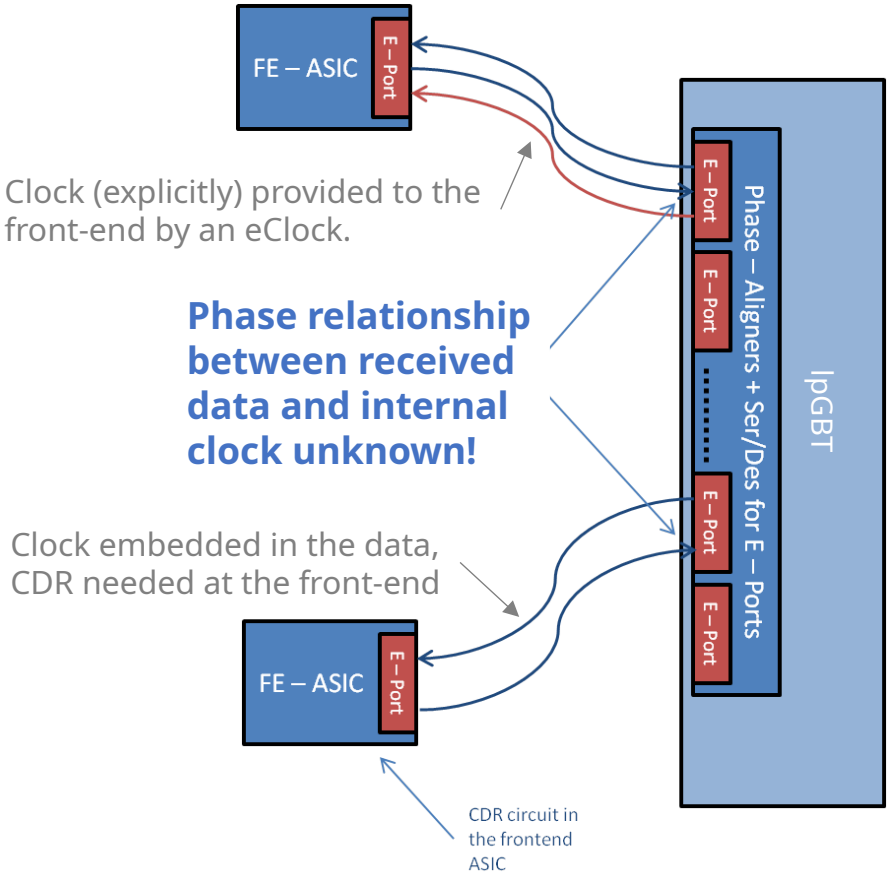
Similar to ePortTx: clustered into groups of links, however

- Number of groups depends on the uplink FEC code (FEC5 vs FEC12)
- Number of links per group depends on group data rate
- Available group data rate depends on uplink data rate (5.12 vs 10.24 GHz)

Rx/Tx data rates and clock frequencies can be set independently!

Input eLinks (uplink)												
Uplink data rate (Gbps)	5.12						10.24					
FEC code	FEC5			FEC12			FEC5			FEC12		
Group data rate (Mbps)	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Electrical Front-End Links – Rx Phase Alignment



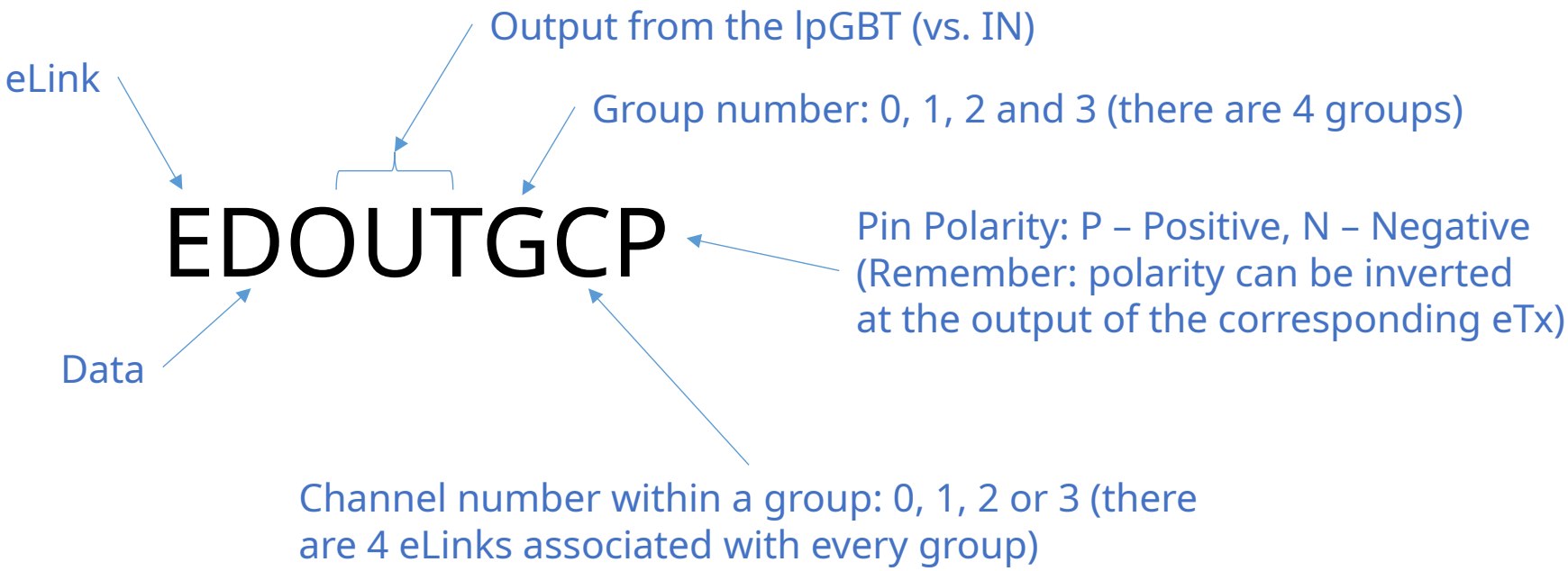
Cable & I/O delays: 'static' phase error between clock and data

- Each eLink might have a different offset
- Enforcing external clock/data relationships is not feasible

Solution: ePortRx phase aligner

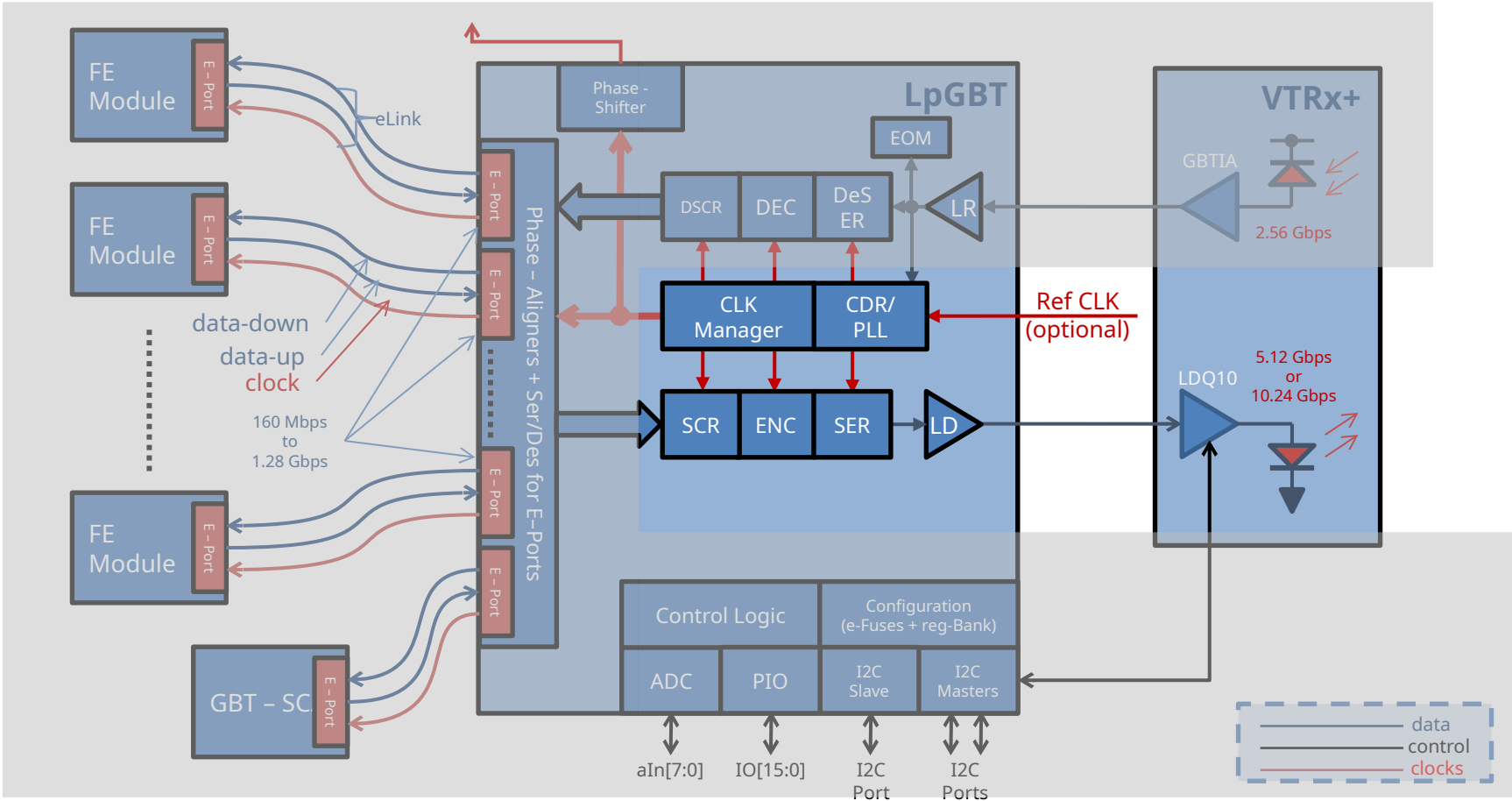
- Sub-bit delay of the incoming data, adjusted to sample in the middle of each data bit
- Operated manually (user) or automatically (one-shot or tracking)
- Must be done / set up separately for each link!

Electrical Front-End Links – eLink Naming



Example: EDOUT32N – eLink data output group 3 channel 2 negative polarity pin

High-Speed Uplink & Data Path



High-Speed Uplink & Data Path

Uplink data path processes the data received by the ePortRxGroups

- Scrambling, FEC encoding, Interleaving, Addition of Header, Serialization
  - Again, details can be omitted (mostly transparent to the user)
- Signal conditioning before exiting the lpGBT: line driver
  - Capable of driving a PCB transmission line, eventually reaching the VTRx+ input
- Finally: VTRx+ performs E/O conversion of 5.12 / 10.24 Gb/s uplink signal

Uplink frame: 128 b @ 5.12 Gb/s or 256 b @ 10.24 Gb/s = 25 ns long

- Again, allows synchronous transmission of eGroup data within each frame → deterministic latency

High-Speed Uplink & Data Path

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- Scrambling, FEC encoding, Interleaving, Addition of Header, Serialization
    - Again, details can be omitted (mostly transparent to the user)

Signal conditioning before exiting the lpGBT: line driver

- Designed to drive 100 Ω transmission lines
- Adjustable drive strength, preemphasis and signal inversion capabilities to optimize link performance
- Eventually: VTRx+ performs E/O conversion of 5.12 / 10.24 Gb/s uplink signal

Uplink frame: 128 b @ 5.12 Gb/s or 256 b @ 10.24 Gb/s = 25 ns long

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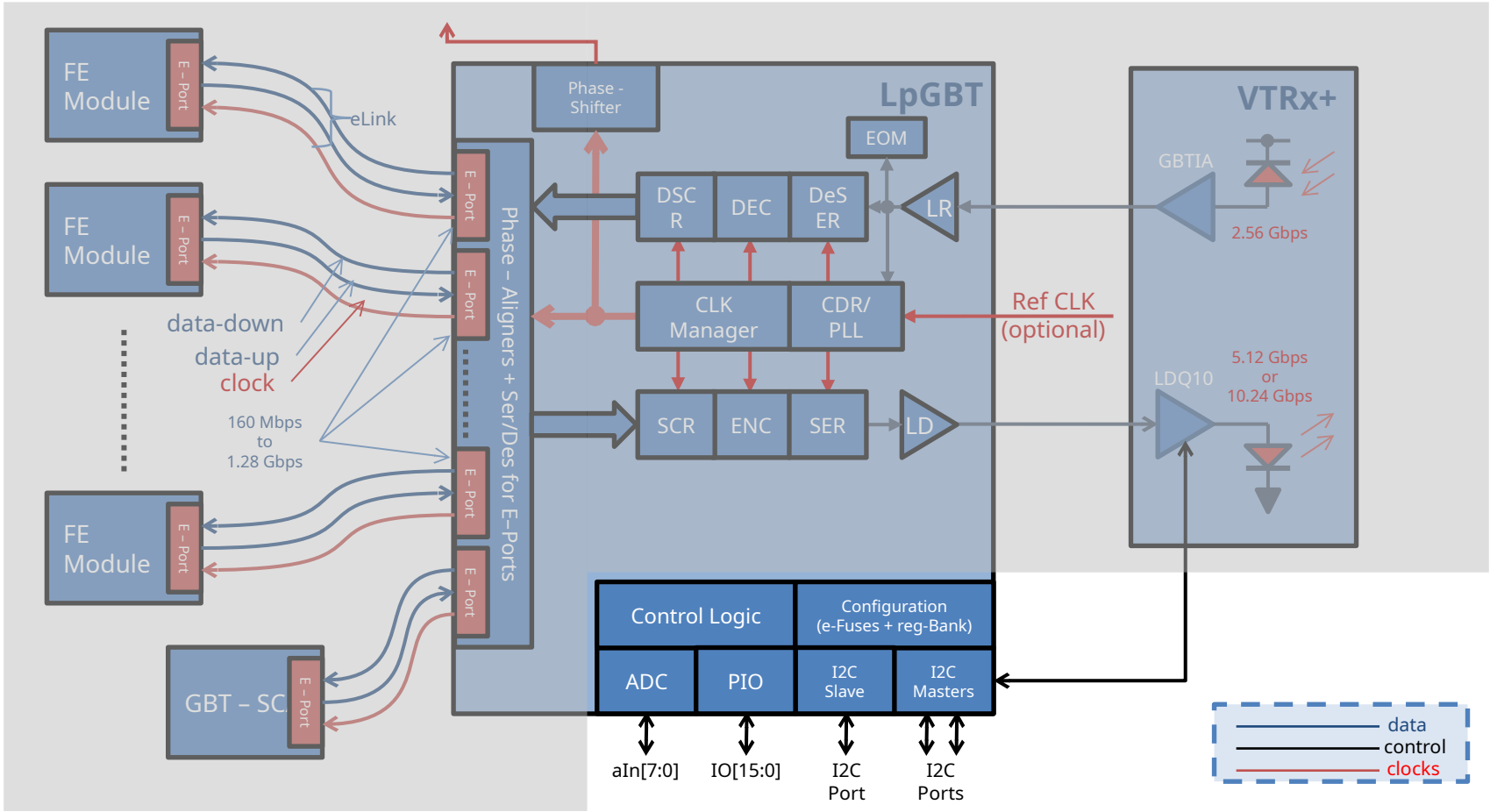
Slow Control & Monitoring Subsystem



Slow Control Subsystem

Various additional features for experiment control

- GPIO bank (16 bit)
  - Independent direction and drive strength control
  - Integrated pull up/down resistors
- RESET output
  - Allows resetting downstream ASICs as soon as lpGBT is ready
  - Programmable pulse duration
- Three I^2C masters
  - Supported bus speed: 100 kHz – 1 MHz
  - Used e.g. to configure VTRx+ laser driver (LDQ10)
  - Supports 7-bit and 10-bit addressing modes

Analog Subsystem

10 bit ADC and analog front-end

- Fully-differential SAR ADC core
- Voltage amplifier (x1 – x32)
- Sample rate up to 1 Msps
- 8 external channels (single-ended or differential), plus internal channels
- Internal channels: supply voltage monitors, on-chip temperature sensor

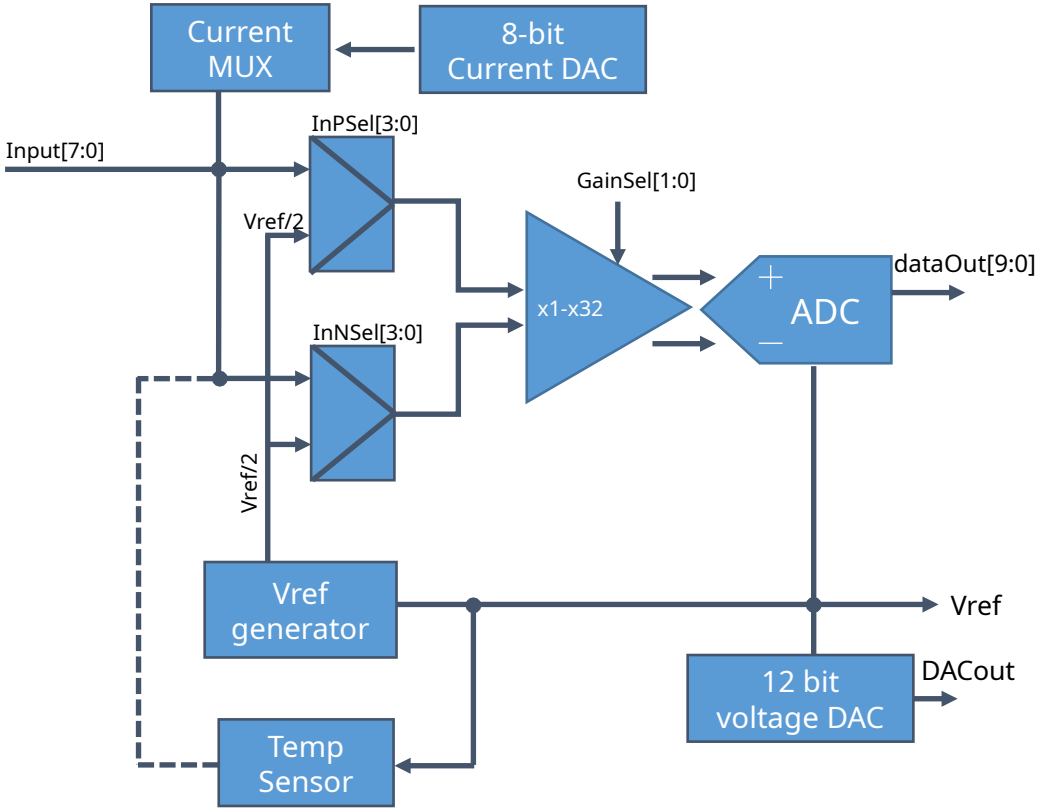
12 bit voltage DAC

- Single channel, referenced to on-chip 1V reference voltage generator

8 bit current DAC

- Can be internally connected to any of the ADC inputs – e.g. for PT1000 temperature sensing

Characterized and calibrated during production testing, per-chip calibration constant database available to users



lpGBT – Radiation Tolerance

lpGBT ASIC manufactured in 65 nm CMOS

- Technology very resistant to TID-effects, characterized for SEE
- Widely adopted for other HL-LHC ASICs

Protected against single-event effects (SEU, SET) by design

- Configuration, control logic, clock generation covered by TMR or RHBD methods
- Data links protected using forward error correction (FEC) – two modes available (tradeoff bandwidth/data protection)

SEE and TID response fully characterized (e.g. expected error rates, etc)

- TID response is being screened for all production lots, spec: 2 MGy (200 Mrad)

System Integration Support

lpGBT model: Behavioral ASIC simulation model

- Models all important configuration/data transmission aspects of the lpGBT, generally clock-cycle accurate
- Some functionality not included (e.g. pre-emphasis/equalization, analog I/O, …)

lpGBT-FPGA: Open source FPGA IP core

- Implements data encoding/decoding, configuration links, etc
- Can be included in FPGA back-end systems, compatible with various FPGA families
- Provides transparent user data bridge, configuration access, etc

lpGBT control library: Python-based driver library

- Reference implementation, to be integrated or adapted by users

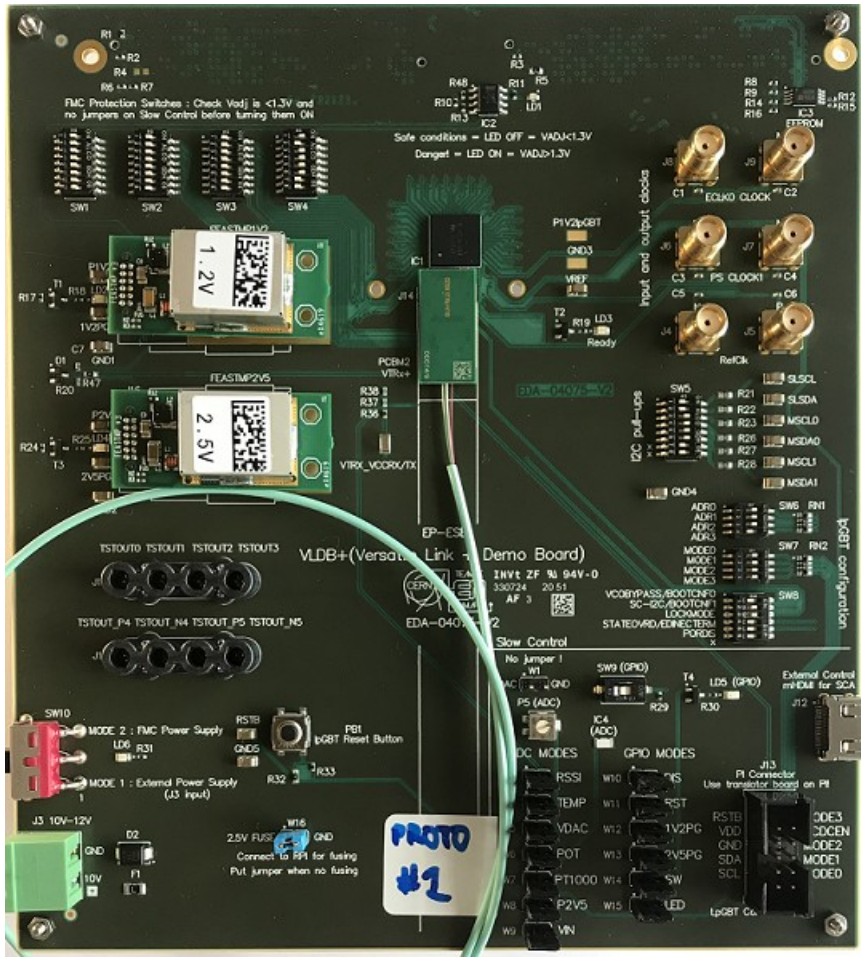
Support forum/mailing list for users, place for discussion: https://lpgbt-support.web.cern.ch

- User base ~ 500 people, dedicated support team for following up issues

VLDB+

Demonstrator board for VL+

- ‘Batteries-included’ demonstrator board for full system
- On-board: lpGBT, VTRX+, rad-tol DC/DC regulators
  - Access to clock & data in/outputs, analog and digital I/O
  - HPC FMC connectors for prototyping with FEB or FPGA development kits
- More information: https://vldbplus.web.cern.ch/
- Demo board in the room to show around!
- Comes with Raspberry Pi-based control toolkit
  - Live demonstration: https://pigbt.web.cern.ch/



Resources

lpGBT manual: https://lpgbt.web.cern.ch **or** https://cds.cern.ch/record/2809058/

lpGBT model: https://gitlab.cern.ch/lpgbt/model/lpgbt_model

lpGBT-FPGA documentation: https://lpgbt-fpga.web.cern.ch

lpGBT / VL+ ordering information: https://ep-ese.web.cern.ch/project/lpgbt-and-versatile-link

VLDB+ documentation, ordering information: https://vldbplus.web.cern.ch

Versatile Link+ project: https://cern.sharepoint.com/sites/project-Versatile-Link-Plus/

Communications ASICs overview: https://gbtproject.web.cern.ch/gbtproject/

Note: Access to some of these pages is guarded by eGroups, can be granted on request

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