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SI LAB Silizium Labor Bonn

FTD

ATLAS EXPERIMENT

13.03.2024 MASTER COLLOQUIUM

STUDY OF TID RADIATION EFFECTS AND CHARACTERIZATION OF THE ITKPIXV2 READOUT CHIP FOR THE ATLAS ITK PIXEL DETECTOR UPGRADE

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OUTLINE

1 Introduction to ITkPixV2

2 Initial chip testing

3 Wafer probing

4 Irradiation

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INTRODUCTION INTO THE ITKPIXV2 READOUT CHIP

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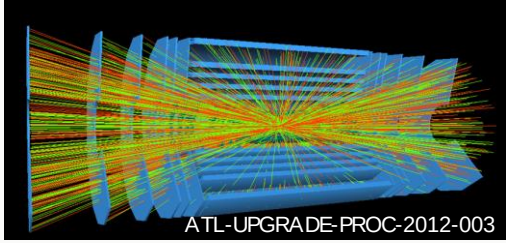
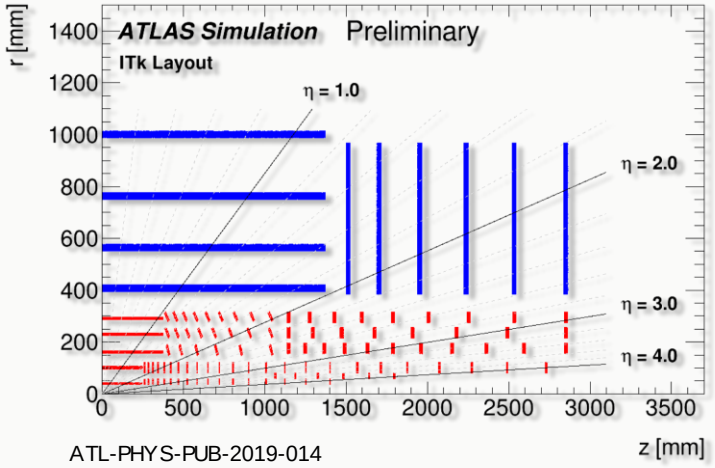
ATLAS PHASE-II UPGRADE



- To cope with **increased instantaneous luminosity** of upcoming HL-LHC upgrade:
- Many parts of the ATLAS detector have to be developed from ground:
  - New all-silicon tracking detector (ITk) with 5 barrel layers of pixel detectors
  - Features of new detector:
    - An increased spatial resolution
    - Higher bandwidth
    - Better radiation hardness

→ **New pixel readout chip** was designed



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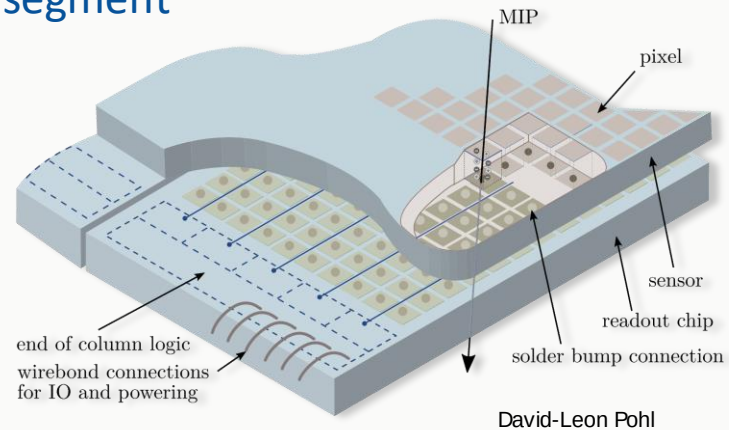
HYBRID PIXEL DETECTOR

- Tracking detector consisting of two parts:
  - Charged particles cause ionizing radiation in **silicon sensor**
    - PN-junction gets depleted to build up a drift field
    - Drifting electrons and holes generate signal at pixel segment
  - These signal get processed in dedicated **readout chip**
    - Individual Front ends connected via "bumps"
    - Performs amplification, digitization, transmission
- R&D happens separately from another:

  → development easier, but hybridization complicated



David-Leon Pohl

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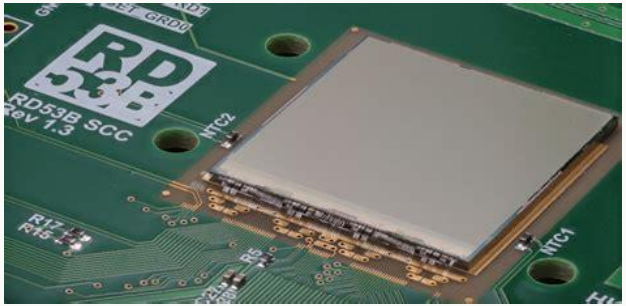
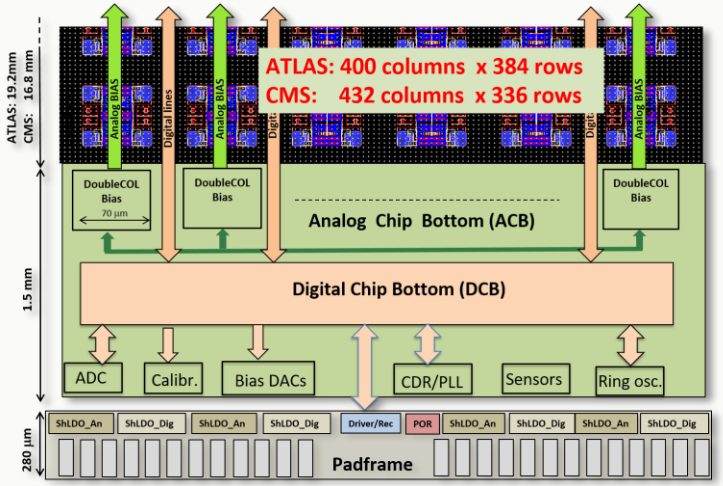
ITKPIXV2 READOUT CHIP



- The readout chip essential part of a hybrid pixel detector
- It has a size of 20mm x 21mm with 384 x 400 pixels (with a pixel bump pitch of 50 µm)
- Mixed-signal chip with analog amplification, discrimination and digital data processing
- Internal data handling is central part of the chip:

  → Rated for hit rate of 3 GHz/cm^2, trigger rate 1 MHz
- Its equipped with power regulators designed to be operated in a serial powering chain

  → Cooling sets narrow power budget



CERN-RD53-PUB-19-002

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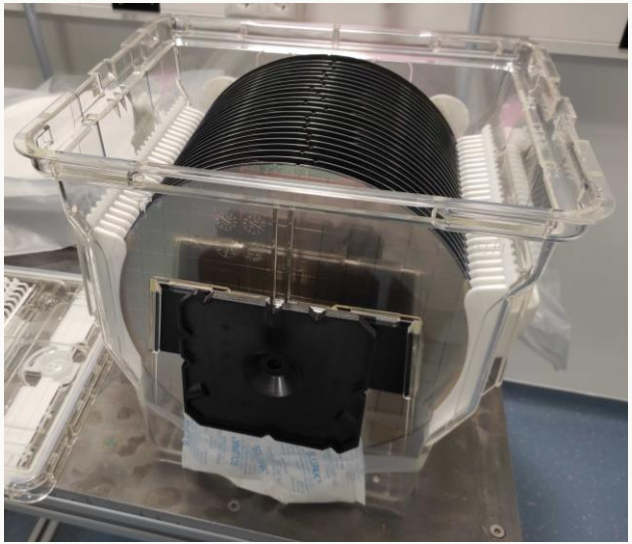
TIMELINE

- 2017/2018: Testing of prototype chip (RD53A) started
- 2020: First full-scale chip ITkPixV1 arrived, pre-production started
- 2023: Production chip ITkPixV2 submitted in April
  - In July first small batch arrived
    → **First tests on wafer level** / preparing probe routine
  - In September first production batch arrived
    → Started **production on wafer level**
  - Oktober – November: **TID irradiation** campaign
- 2024-2026: Module production



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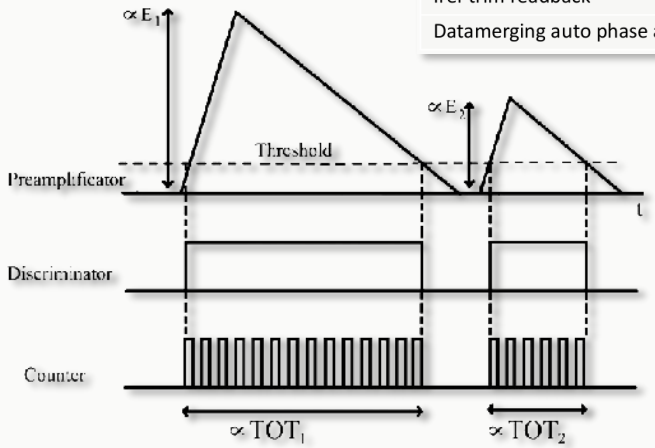
INITIAL CHIP TESTING

INITIAL RECEPTION

- Chip started up perfectly:
  - Good power consumption
  - Basic scans successful
- Confirmed bugfixes:
  - ToT and pToT working
  - Data Merging phase alignment
  - Many other small changes...
- No new major bugs found effecting detector operation

Feature	Tested
Power consumption	✓
Register R/W	✓
Iref trim	✓
Vref trim	✓
Tuning	✓
Digital scan	✓
Analog scan	✓
Threshold scan	✓
Datamerging	✓
Monotonic ToT at 80 MHz	✓
PToT working	✓
T/B RPOLY resistors	✓
Iref trim readback	✓
Datamerging auto phase alignment	✓



2011 Phys. Med. Biol. 56 1947

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CHARACTERIZATION

- The FEs can be characterized by performing threshold scans
  e.g. after tuning the pixel thresholds to a certain threshold like 1000 e^-, 2000 e^-
- Configuration of analog front end depends on the needs of each layer in detector
  - Compromise: performance <-> power consumption
- Register settings where specified for each layer
  - They control the preamplifier gain and reset current of the analog front ends of each pixel
- This was performed for each layer setting with nominal supply voltage VDD = 1.2 V and with reduced supply voltage of 1.1 V

Layer	Target Thr.	Thr. disp.	Noise
L0	1k e^-	27 e^-	38 e^-
L0	2k e^-	33 e^-	38 e^-
L1	1k e^-	26 e^-	39 e^-
L1	2k e^-	33 e^-	41 e^-
L2-4	1k e^-	21 e^-	32 e^-
L2-4	2k e^-	32 e^-	34 e^-

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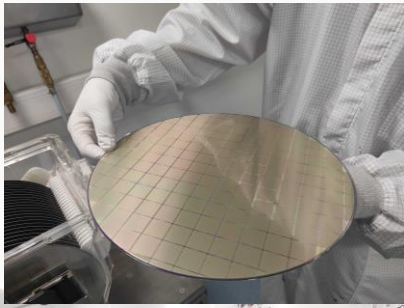
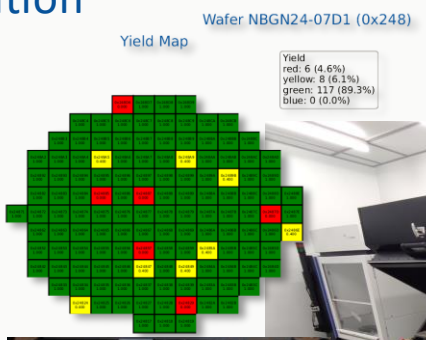
WAFER PROBING

INTRODUCTION OF WAFER PROBING

- To save unnecessary production cost:
  - All dies are first tested on wafer level in probe station
  - Wafers send for hybridization with yield map →
- Probing procedure:
  - Wafer position / height calibrated up to few µm
  - Probe card used to contact the 200 pads of chip
  - Each die individually tested: basic functionalities
  - Optimized to one day / wafer





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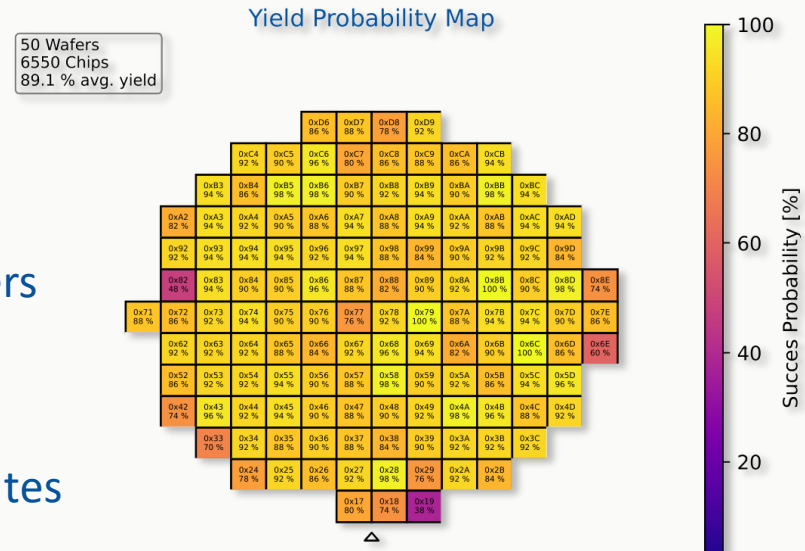
STATUS OF WAFER PROBING

- Yield of predecessor chip: 80 %
- Problems on DAQ side solved: yield 60 % → 90 %
- Probing time was reduced to 21 h
- Together with Glasgow we probed the first 100 wafers for the production of ATLAS ITk Pixel modules
- The remaining probing sites where also supported progress was shown towards qualifying as probing sites
- Together, up to 700 wafers will be probed for building ATLAS ITk Pixel tracker



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IRRADIATION

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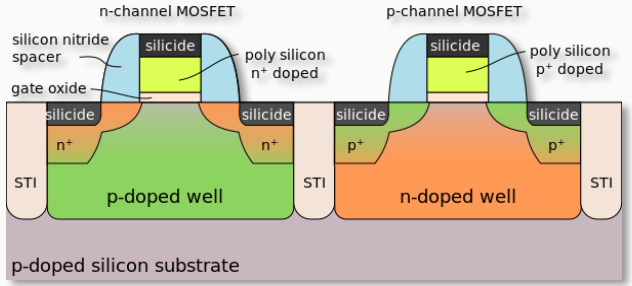
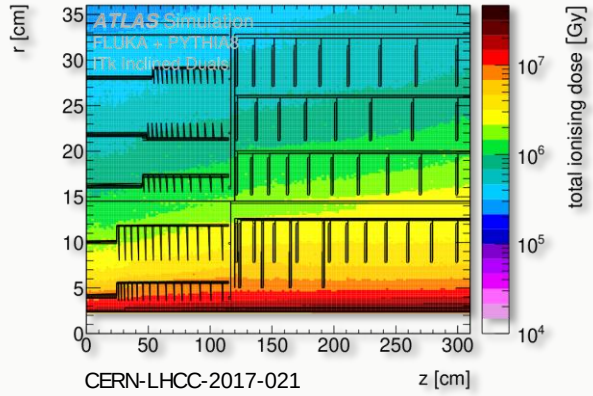
TID DAMAGE



https://commons.wikimedia.org/wiki/File:LDD-MOS_transistor_-_CMOS_with_STI.svg

- Total Ionizing Dose: measured in rad (100 rad = 1 Gy)
- Charged particles cause ionization also in the SiO_2 of readout chip
  - In: gate oxide + shallow trench isolation oxide between transistors
  - The holes from the electron-hole pairs may get trapped → positive charge in SiO_2
- Transistor properties affected (> 600M transistors)
  - E.g. threshold, but also gate delays in logical cells
- Innermost layers of ATLAS Pixel tracker will see up to 1 Grad of TID until end of lifetime (including 1.5 safety factor)
- Bulk damage only plays secondary roles for CMOS chip



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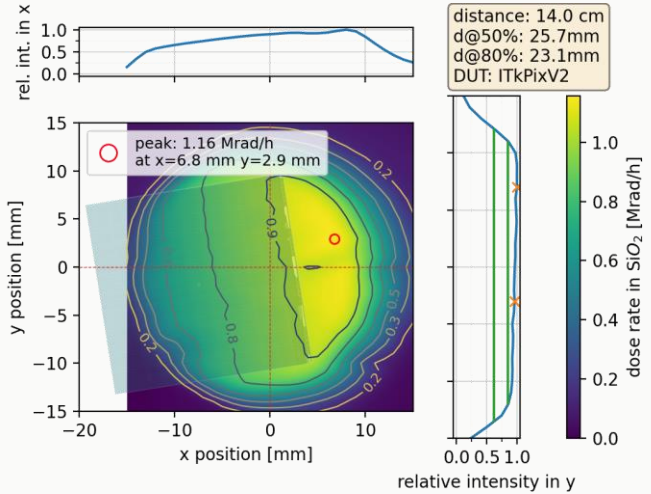
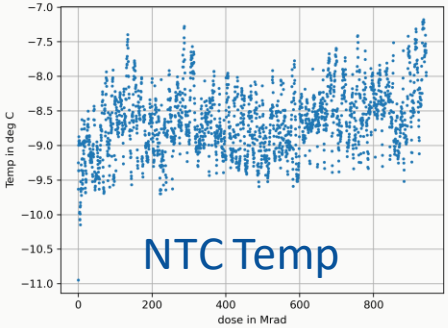
IRRADIATION SETUP

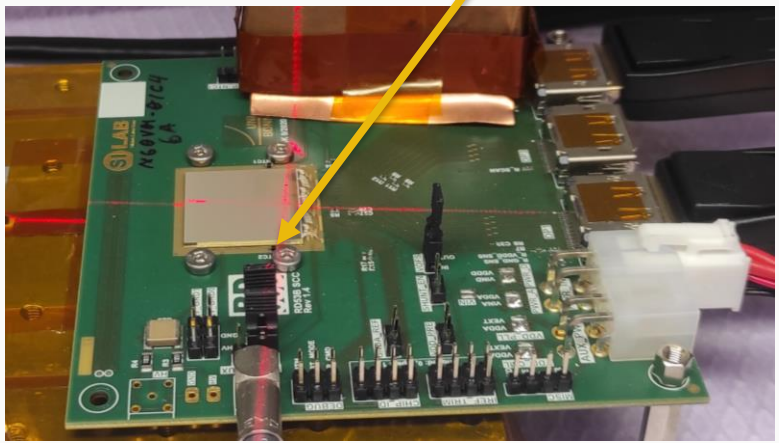
- Confirm the radiation hardness of ITkPixV2
- Testing up to 1 Grad TID using X-Rays:
  - Tube: tungsten target, 40 kV, 50 mA, 150 µm Al filter
- Beam profile determined with calibrated diode
- Non-homogenous profile:
  - Chip bottom positioned into flat spot
  - Pixel matrix irradiated partially
  - High rate irradiation in 6.5 weeks
  - Incorporating losses in Al layers: 0.85 Mrad/h



IRRADIATION PROCEDURE

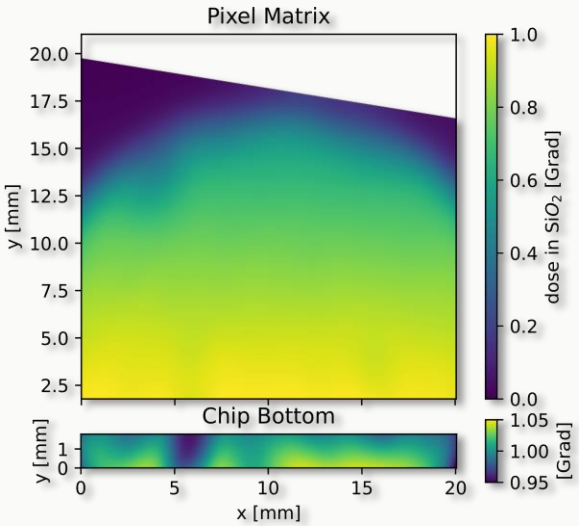


- During irradiation:
  - Chip powered (shunt mode), and cooled with chiller at maximal capacity
  - Monitoring all voltages, currents, environmental data, ring oscillators
  - Keep chip busy with analog scans in between
- Between Irradiation steps: (of increasing size)
  - Calibration of Regulators, ADCs, IV curves...
  - Threshold tuning and characterization
- Before / After:
  - Additional temperature calibration



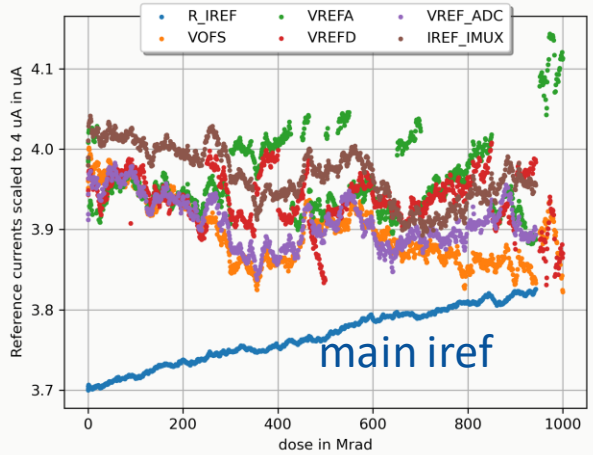
IRRADIATION OVERVIEW

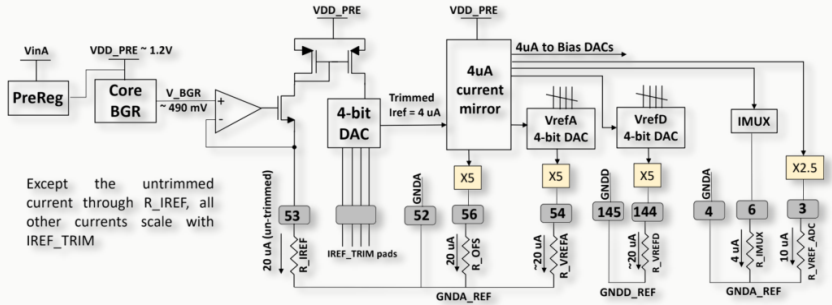
- After a rough preparation: irradiation ran almost without problems
  - But: 942 Mrad → reference ground got broken
    - Failure of SMU, effects some data, on backup slides
- Chip working perfectly after 1 Grad in chip bottom
- Further results divided into measurements related to:
  - Power regulator
  - Chip periphery
  - Pixel Matrix



REFERENCE CURRENTS

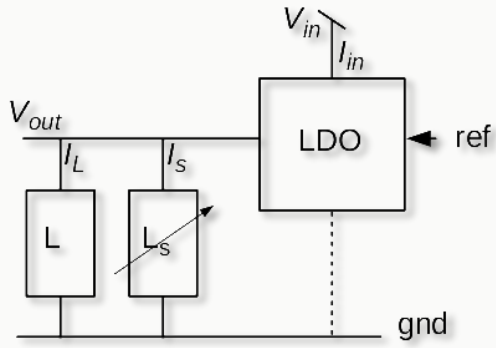
- Power regulators and chip periphery rely on references
- Main reference generated from band gap reference
  - TID effects cause main iref (blue) to drift up
- All other references derived using current mirrors
  - In tuning circuit: references get more unpredictable
- In case of VrefA and VrefD
  - Compensable with dedicated DACs

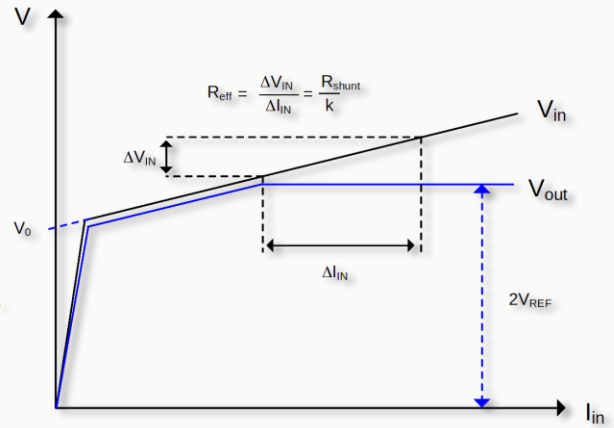




SLDO POWER REGULATORS

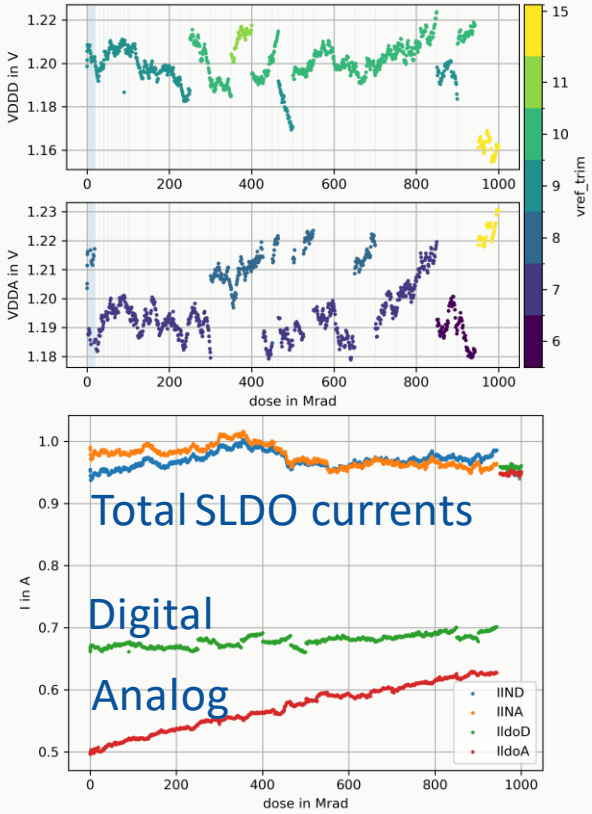
- Shunt Low Drop Out regulator
- Generates output voltage VDD based on reference Vref
- Input current split to load (chip) and shunt resistor (controlled)
- Shunt load regulated to achieve input characteristics →
  - Given by offset Vofs and slope Rshunt/k
  - Vofs tuned to 1 V, k factor designed to be 1000
- In detector:
  - One current sourced to chain of such regulators





SLDO POWER REGULATORS

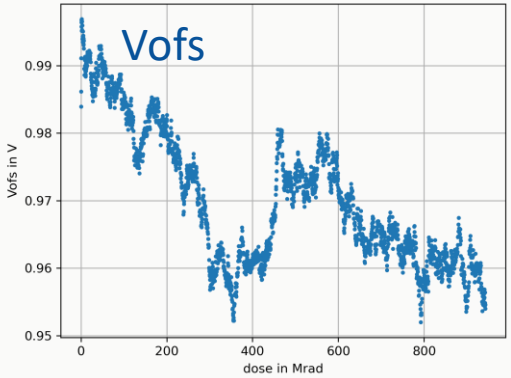
- Supply voltages trimmable to 1.2V within 2 %
- Current consumptions:
  - Digital consumption relative constant
  - Analog consumption increased by around 20 %
    - Compensable with FE configuration
- Additional current overhead is consumed:
  - Designed overhead: 10 %
  - Effective load variation: < 5%

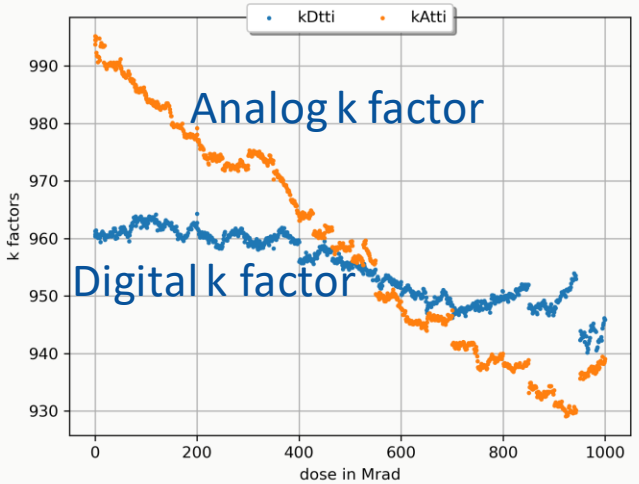


SLDO POWER REGULATORS

- Regulator input characteristics depends on:
  - Vofs:
    - Generated from reference currents
    - But shared on module

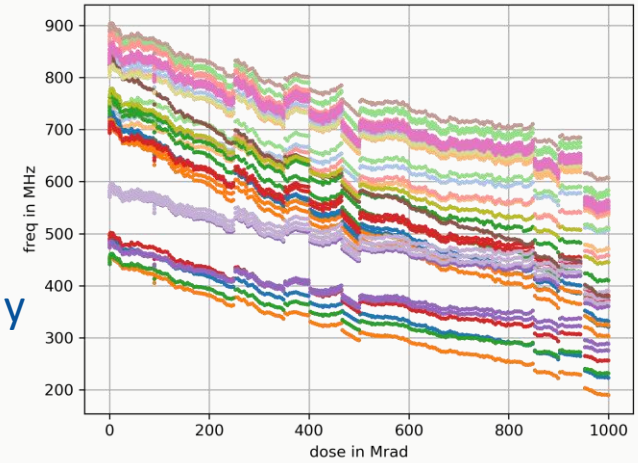
      → does not generate current imbalance
  - k-factor
    - Property of each individual regulator (quad module: 8 regulators in parallel)
    - Can generate current imbalance between chips
    - But: < 10 % still in budget

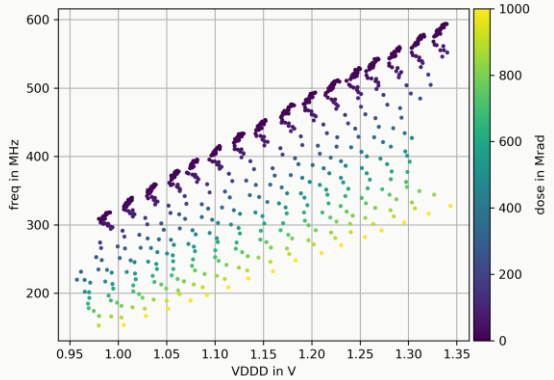




RING OSCILLATORS 1

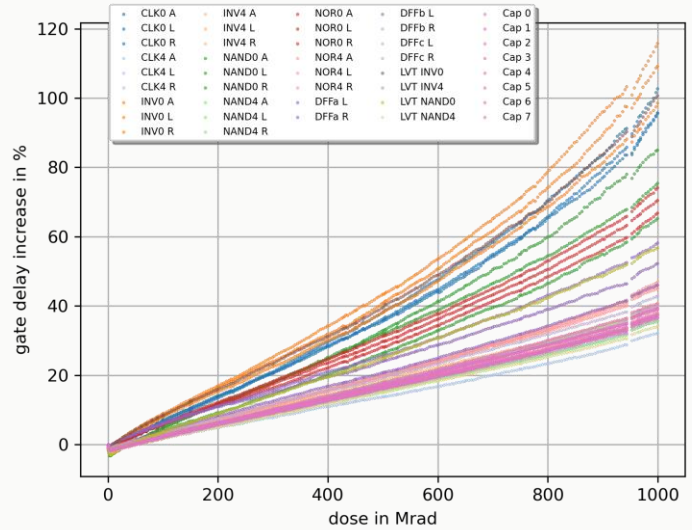
- Ring oscillators as radiation monitors:
  - Chain of inverting logic cells
  - Frequency depends on supply voltage, length, gate delay
  - Gate delay depends on TID
- Different types (total: 42) monitored continuously
  - Frequencies need to be corrected for VDDD dependency
  - Calibration performed between irradiation steps →

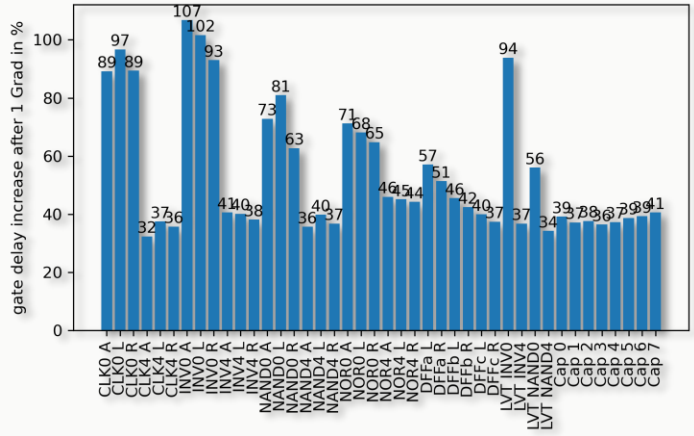




RING OSCILLATORS 2

- From corrected data: increase of gate delay →
- Results depend on driver strengths of logic cells:
  - Cells with strength of 4 only see increase by factor 1.4
  - Cells with strength 0:
    - Low power
    - Smallest footprint
      - Greatly affected from isolation oxide
- Still noticeably below gate delay increase of factor 3



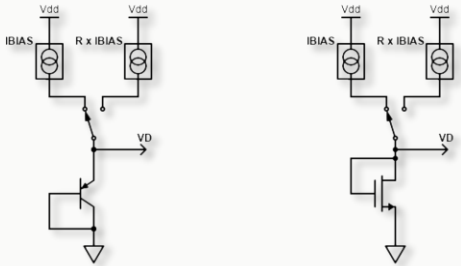


RADIATION / TEMPERATURE SENSORS

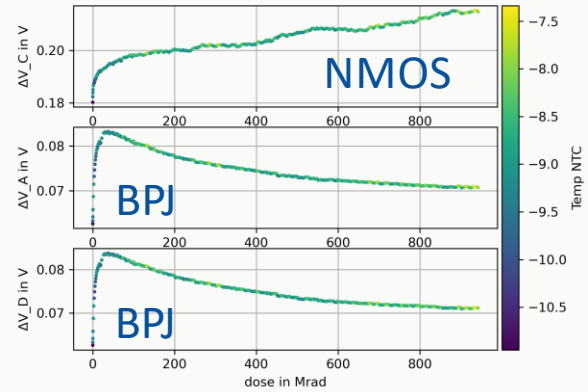
- BPJ and CMOS transistors can be used as temp sensors
- Temp. from volt diff for two bias current with ratio R:

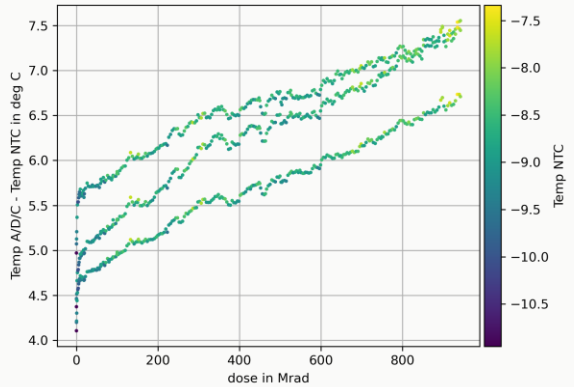
$$\Delta V_D = V_D(R \times I_{bias}) - V_D(I_{bias}) = N_f \times \frac{k_B T}{q} \times ln(R)$$

- BPJs very sensitive to TID / bulk damage: good rad sensors →
- TID also effects temperature readout:



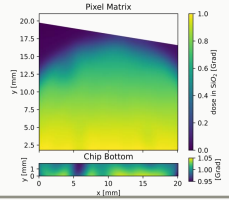
$T_{Diode} - T_{NTC}$ →

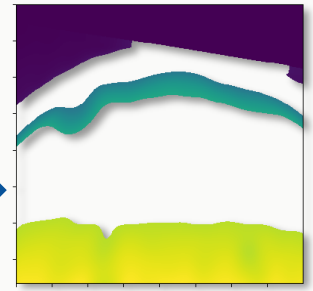




OVERVIEW OVER PIXEL MATRIX RESULTS

- Between each irradiation step:
  - Threshold scan with untuned chip
  - Threshold scan with initial tuning
    - All pixels tuned to 1k e⁻ thr before irad
  - Threshold scan after tuning
    - All pixels tuned to 1k e⁻ thr again
- Results based on threshold / noise map
  - Given for 3 groups based on final dose:

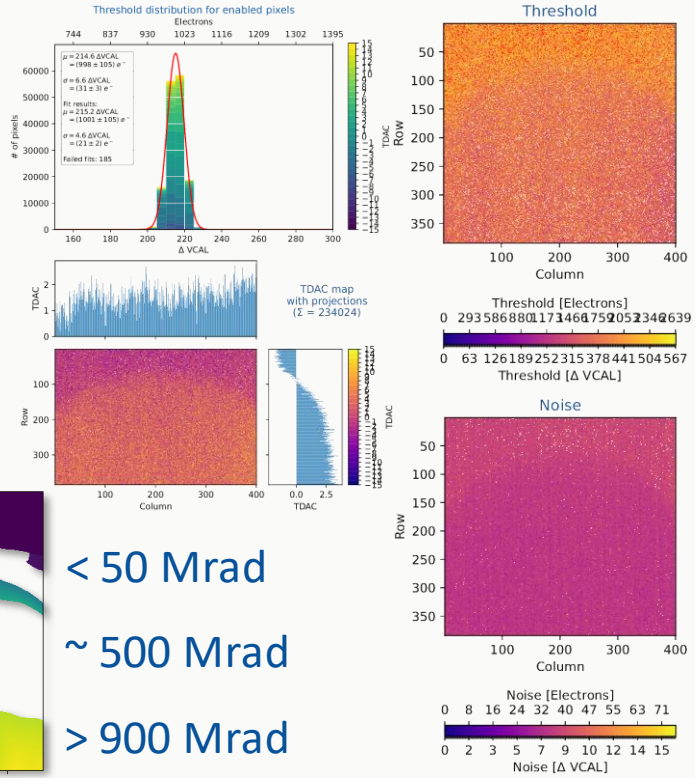




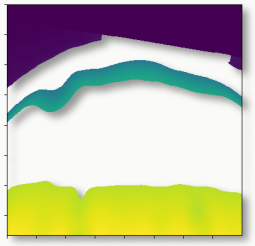
< 50 Mrad

~ 500 Mrad

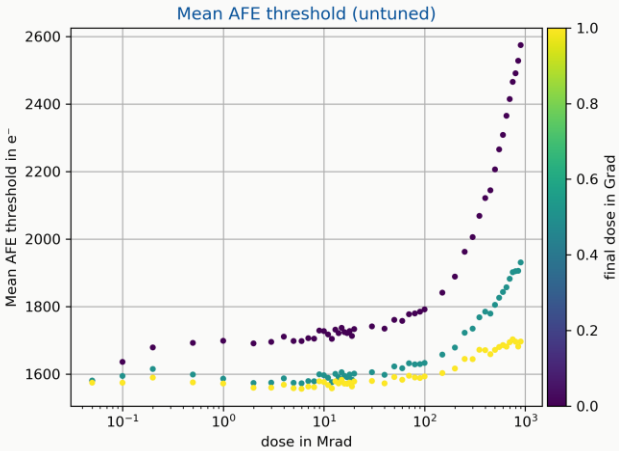
> 900 Mrad

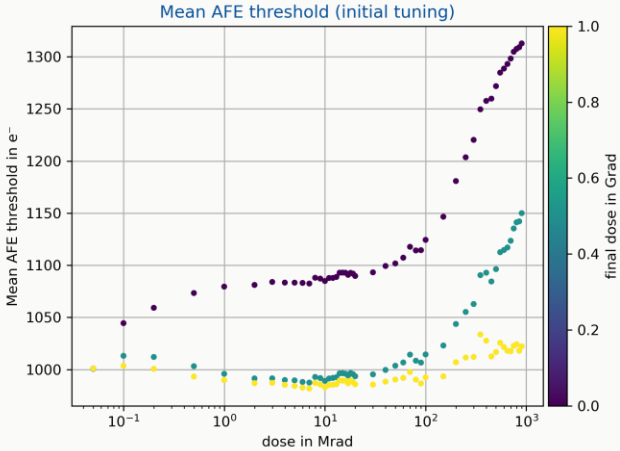


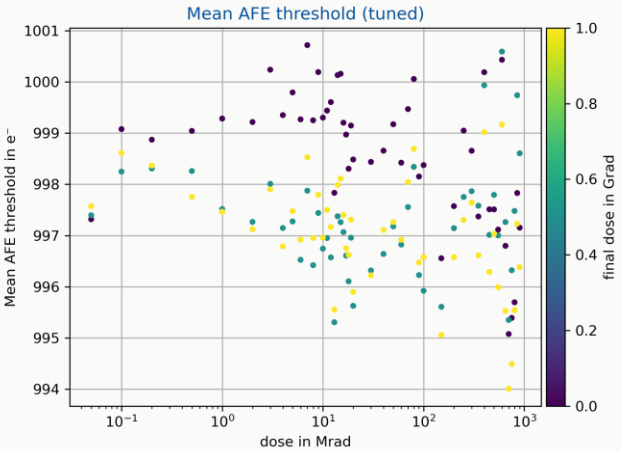
MEAN PIXEL THRESHOLD



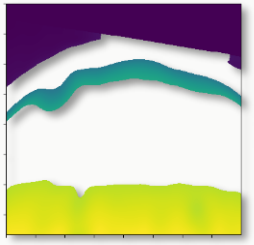
- Global threshold almost not effected by TID: if pixel dose matches dose in chip bottom
  - Bias voltages generated in chip bottom → Threshold runs away for unirradiated pixels
- Threshold still re-trimmable up to few e^- for all doses



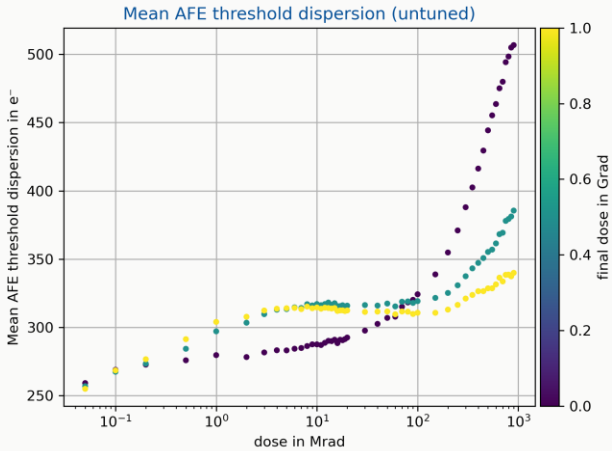


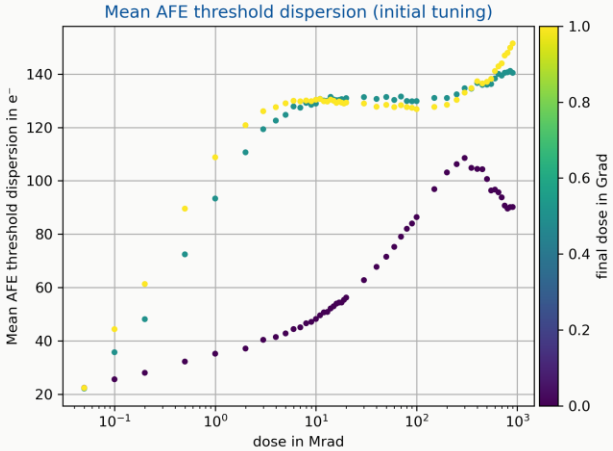


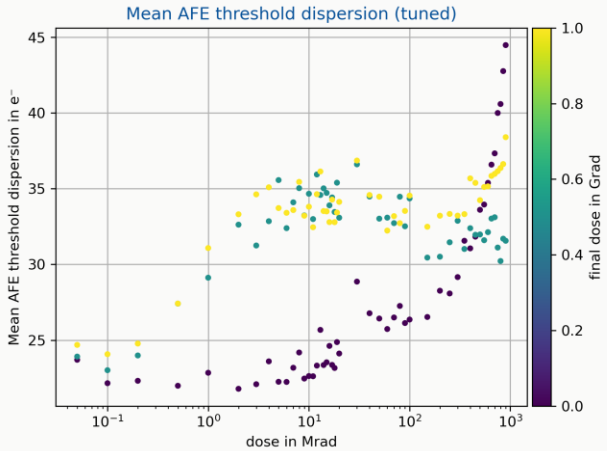
PIXEL THRESHOLD DISPERSION



- Threshold dispersion increased with dose in each individual pixel
- Threshold still re-trimmable → threshold dispersion after irradiation slightly increased
  - Range of trimming limited, also global threshold suboptimal (non-homogeneous irad)







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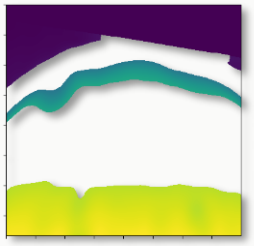
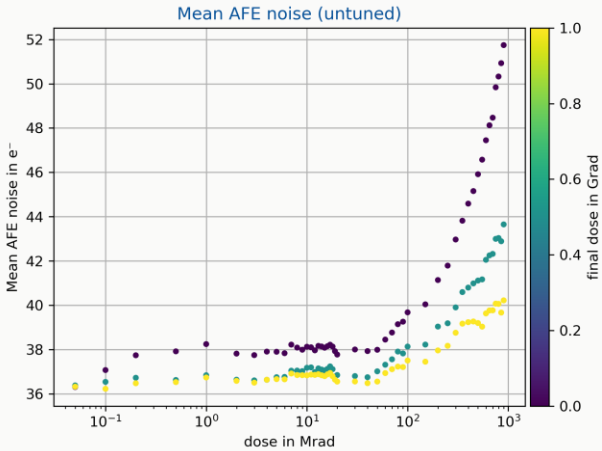
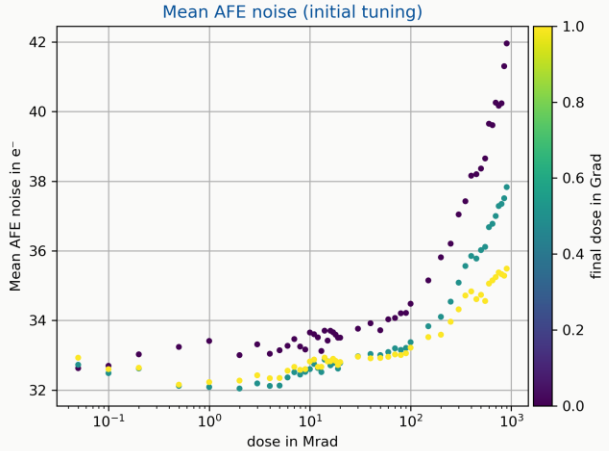
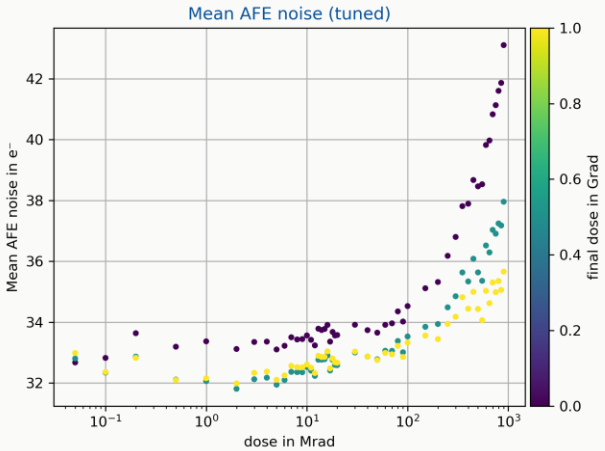
PIXEL NOISE



- FE noise almost unaffected by TID
- Slight increase (10 %) after 100 Mrad
  - Could be related to increased global biases







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CONCLUSION

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CONCLUSION / OUTLOOK

- The production version of the ATLAS readout chip ITkPixV2 was successfully tested
- The readout chip shows a good tolerance for radiation damage up to 1 Grad of TID
  - On-chip regulators are still able to ensure stable operation
  - Digital logic continues to process the immense amount of data
  - Analog pixel circuitry can still keep up with the specs
- These measurements contributed to a final qualification of the readout chip
- This initiated the final production of pixel modules

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THANK YOU FOR YOUR ATTENTION!

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BACKUP

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DISCOVERED CHIP BUGS

- Only few minor bugs where discovered in the ITkPixV2:
  - Default values of registers for the serial data transceivers yield unstable link
    → Can simply be re-configure after a reset
  - Data Merging feature meant for reducing the number our readout channels:
    - There is a 5 % chance that the circuit will lock to the data
      → A changed reset scheme can prevent this problem
- For both issues there are simple work around, which do not effect detector operation

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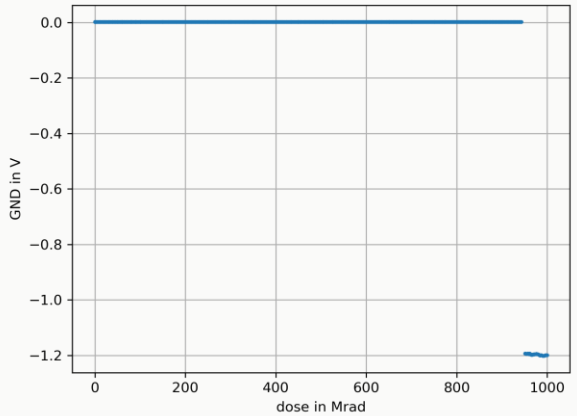
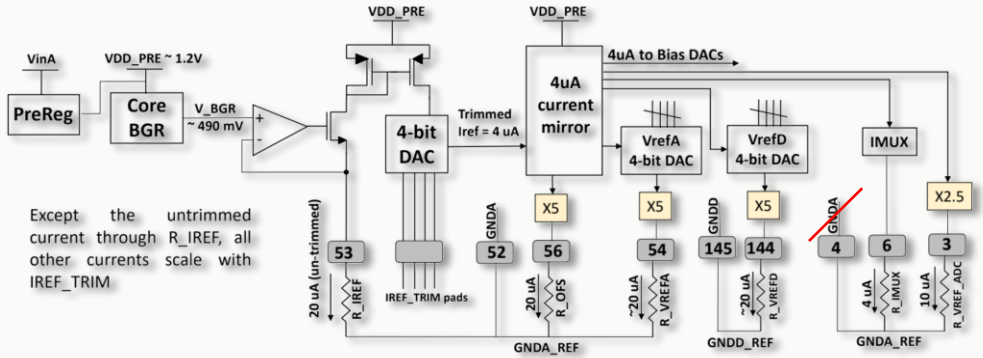
INITIAL PROBLEMS DURING WAFER PROBING

- Wafer Probing initially struggled with 3 yield drivers:
  - Power regulators not starting up correctly in some instances
    - Both power domains have to start up simultaneously
  - Data merging sometimes requiring a power cycle of the chip
    - Related to chip bug
  - Occasional corrupted / missing words in digital / analog scans
    - Related to instability of power railed: parasitic effects from probe card
- All fixed

ISSUES WITH GNDA_REF

- At 942 Mrad: failure of SMU killed internal connection from GNDA_REF to GNDA
- But all voltages measured relative to this voltage e.g. →
- Can be corrected to some degree, but:
  - also VREF_ADC affected
  - IMUX mostly unusable
  - Analog monitoring board unhappy
- I had to continue irradiating:
  - Could only fix after irradiation





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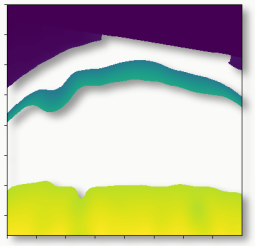
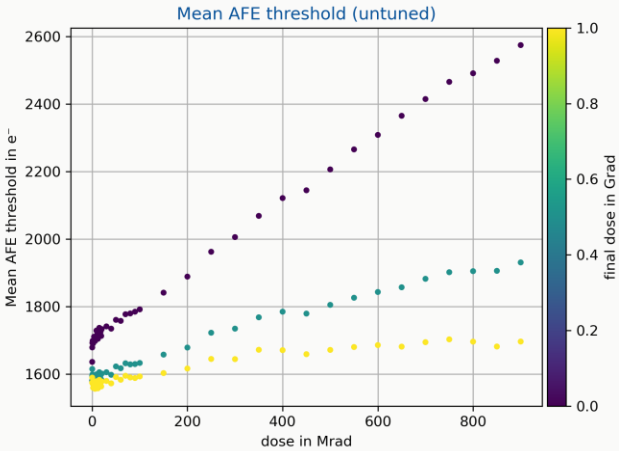
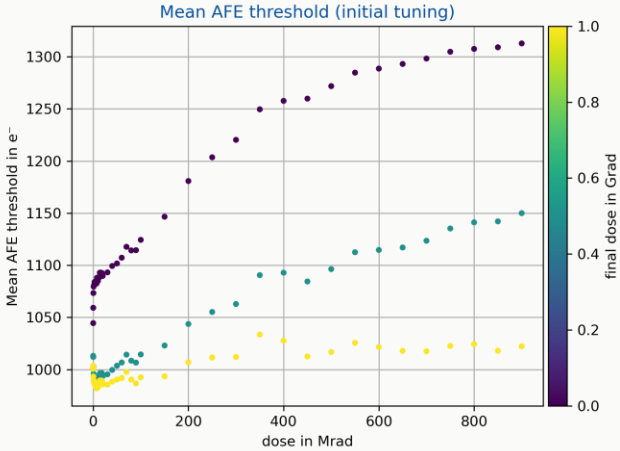
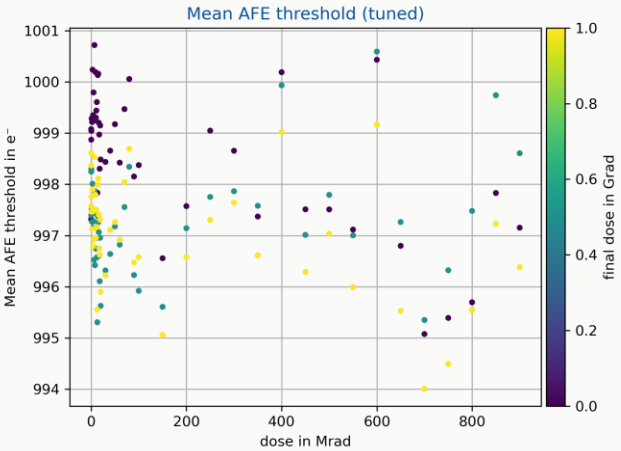
MEAN PIXEL THRESHOLD (LINEAR SCALE)



- Global threshold almost not effected by TID: if pixel dose matches dose in chip bottom
  - Bias voltages generated in chip bottom → Threshold runs away for unirradiated pixels
- Threshold still re-trimmable up to few e^- for all doses







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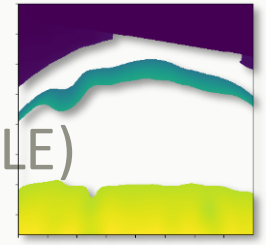
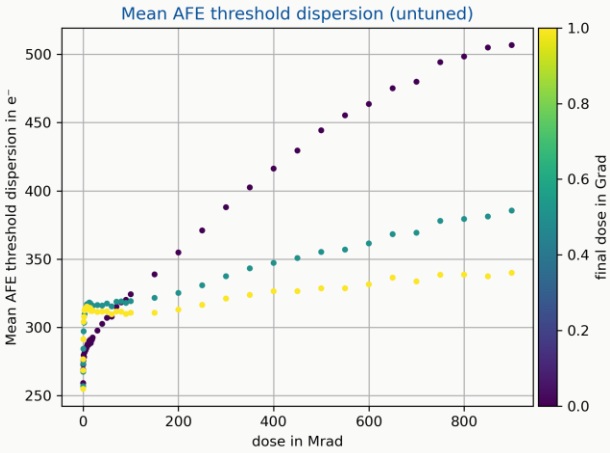
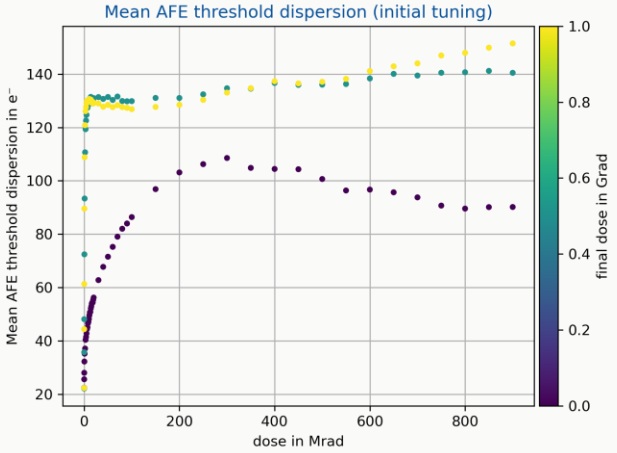
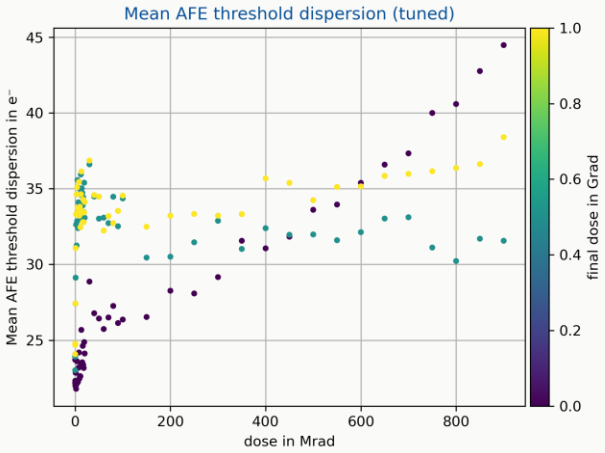
PIXEL THRESHOLD DISPERSION (LINEAR SCALE)



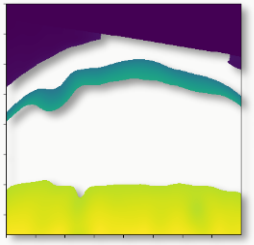
- Threshold dispersion increased with dose in each individual pixel
- Threshold still re-trimmable → threshold dispersion after irradiation slightly increased
  - Range of trimming limited, also global threshold suboptimal (non-homogeneous irad)







PIXEL NOISE (LINEAR SCALE)



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