

MASTER-COLLOQUIUM 17.11.23

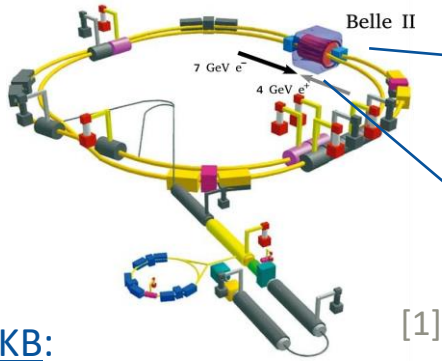
PXD EMERGENCY SHUTDOWN SIMULATION

Paula Scholz



- 1 Motivation
- 2 Transmission Line Theory
- 3 Cable Models & Parameter Measurements
- 4 Simulation of Full Setup

SUPERKEKB AND BELLE II

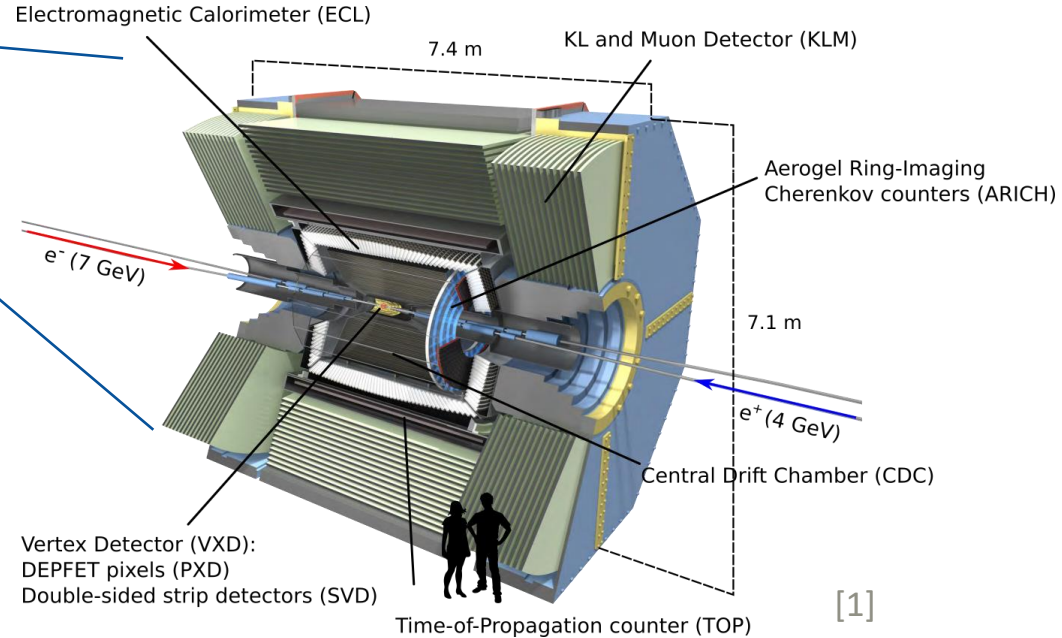


- SuperKEKB:

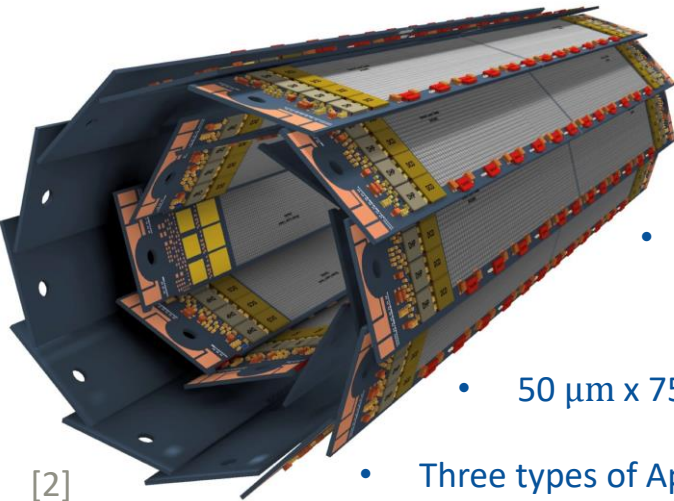
- Asymmetric e^+e^- collider
- Peak luminosity $L = 4.7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$

- Belle II:

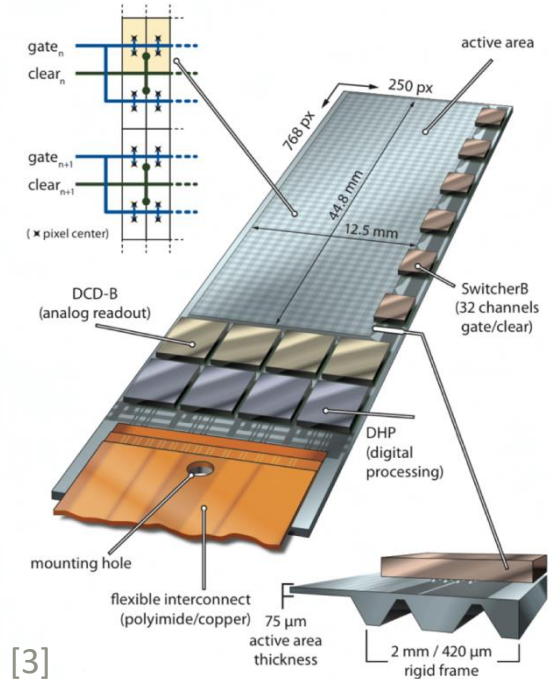
- Contains vertex detector including pixel detector



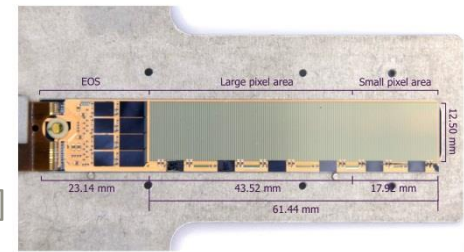
BELLE II PIXEL DETECTOR (PXD)



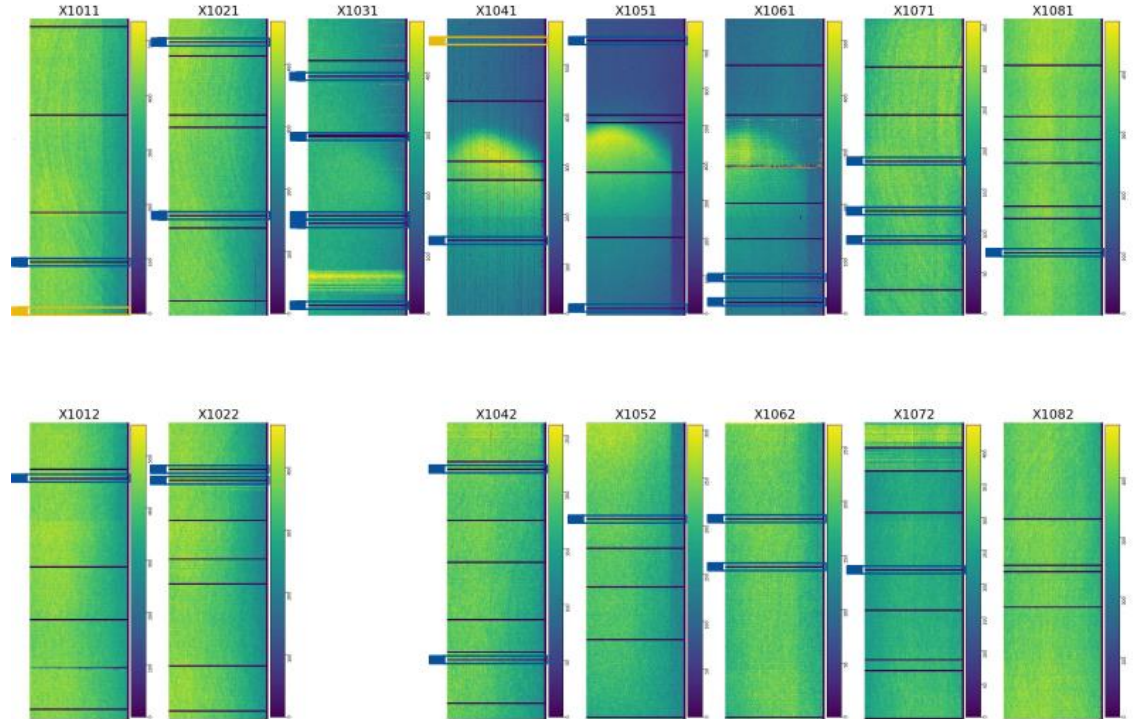
- PXD: two layers of DEPFET modules at radii of 14 mm and 22 mm
- 50 μm x 75 μm pixels thinned to 75 μm
- Three types of Application Specific Integrated Circuits (ASICs) are responsible for readout:
 - DCD, DHP, **Switchers**



MOTIVATION

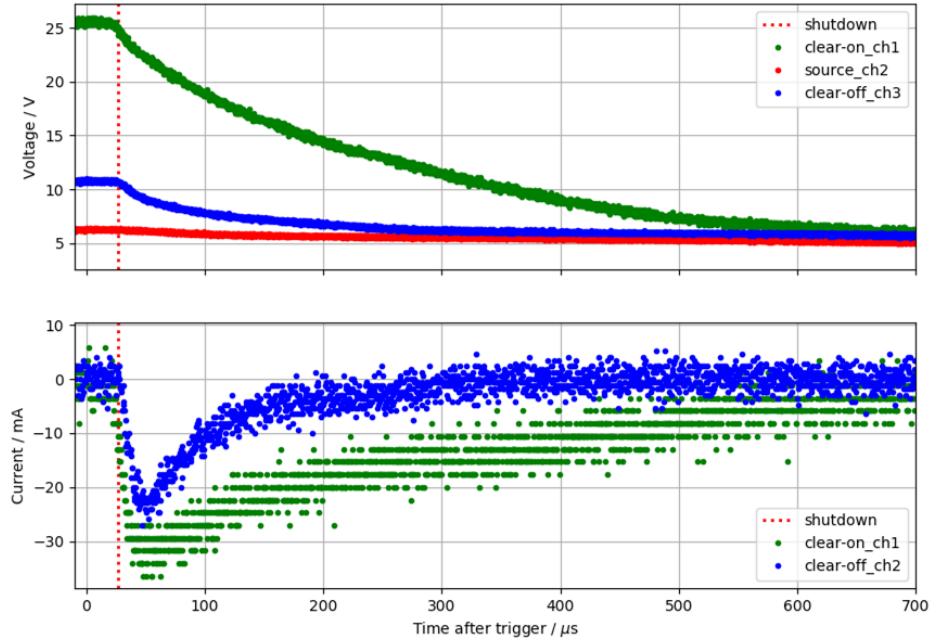


- Switchers **vulnerable** to large radiation
- Example: Beam loss event in 2020
 - Estimated dose: 500 rad for PXD1 in 40 μ s
 - Increased number of **inefficient rows**
 - In total 89 inefficient rows \rightarrow efficiency drop of 3%
 - blue flags: freshly emerged inefficient rows
- Damage can be prevented when Switchers are turned off
- \rightarrow Shutdown as fast and safe as possible



REGULAR SHUTDOWN

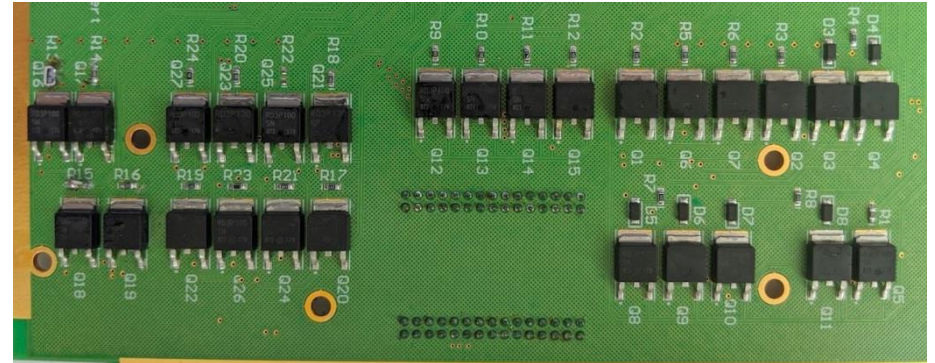
- Regular shutdown applied at PXD1:
 - Switch off power
- Example: Shutdown of Switcher voltages
- **Long discharge time** due to capacitors
 - Shutdown time in ms-range



[4]

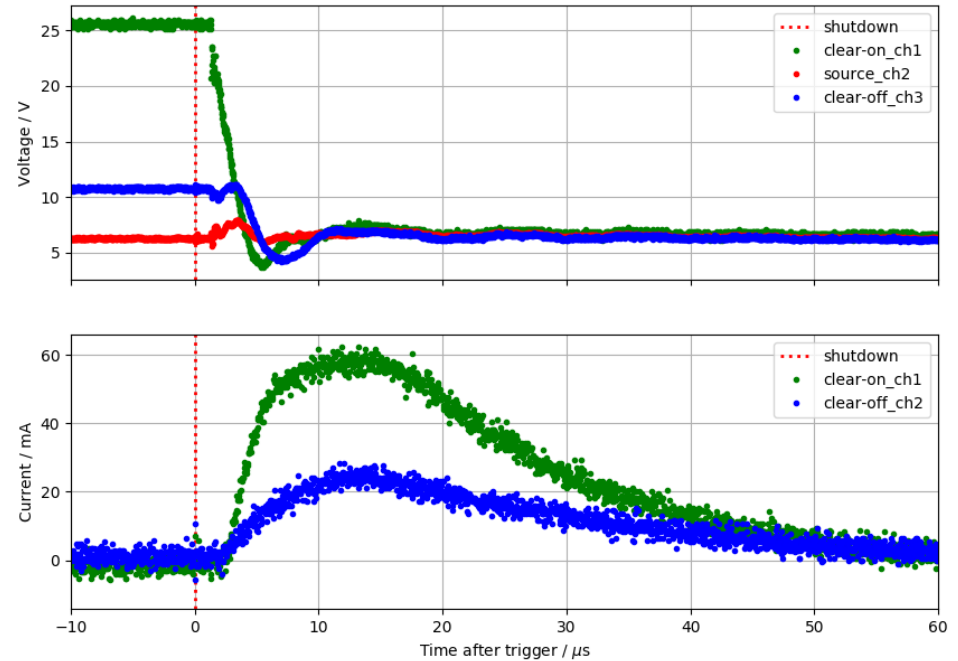
FAST SHUTDOWN BOARD

- Idea:
 - Short all channels with FET to respective ground
→ **Active pull-down**
 - Add resistor to influence pull-down time
- Problem: Required resistor values unclear yet



FAST SHUTDOWN MEASUREMENT

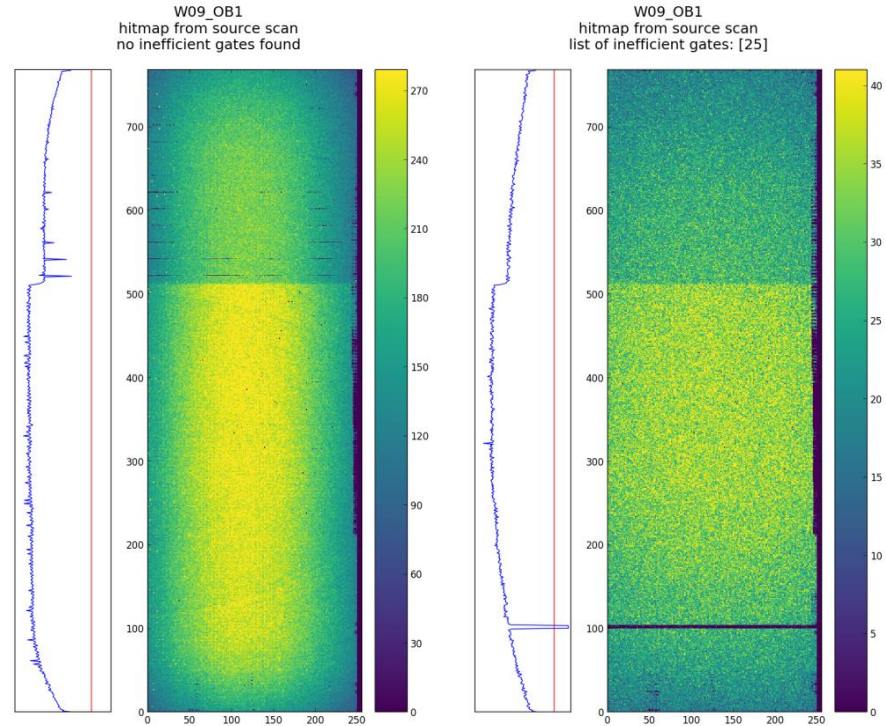
- Example: Shutdown of Switcher voltages (Clear On/ Clear Off), **measured at Power Supply level**
- $R_{clear\ on} = 0\ \Omega$, $R_{clear\ off} = 0\ \Omega$
- $V_{clear\ on}$ drops below $V_{clear\ off} \rightarrow$ violation of shutdown sequence



[4]

RESULTS FROM FAST SHUTDOWN

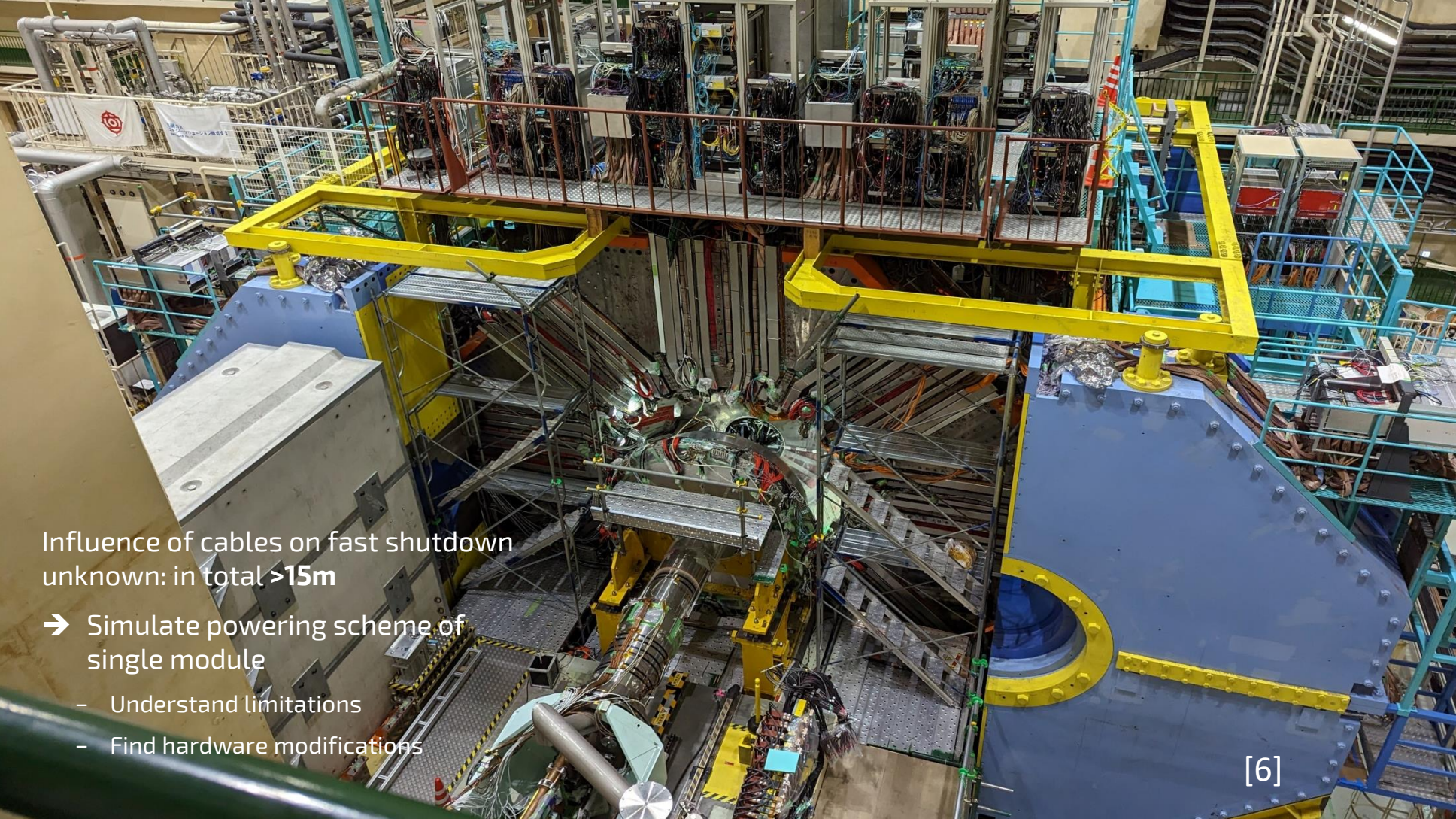
- Testing of **fast shutdown** board resulted in high Switcher currents
- Example:
 - Compare hitmaps before and after using fast shutdown board
 - Detected **inefficient rows**
- If done wrongly:
 - Fast shutdown has **same effects** as a beam loss event
- Testing on module is harmful



Before fast shutdown

After fast shutdown

[5]

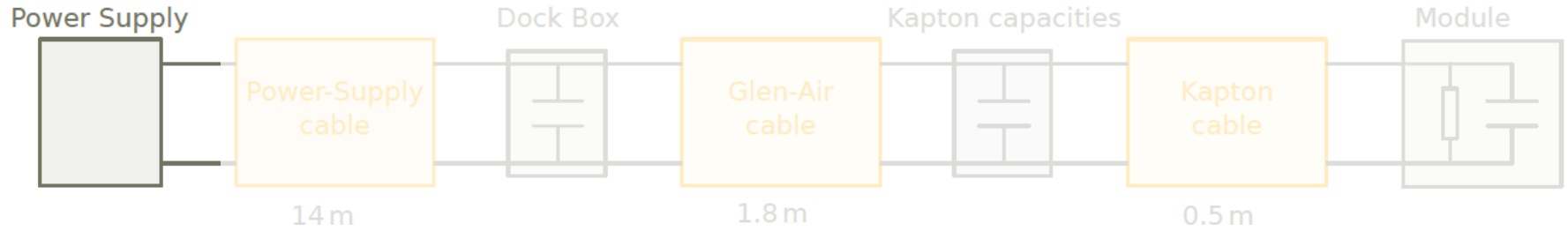


Influence of cables on fast shutdown
unknown: in total >15m

→ Simulate powering scheme of
single module

- Understand limitations
- Find hardware modifications

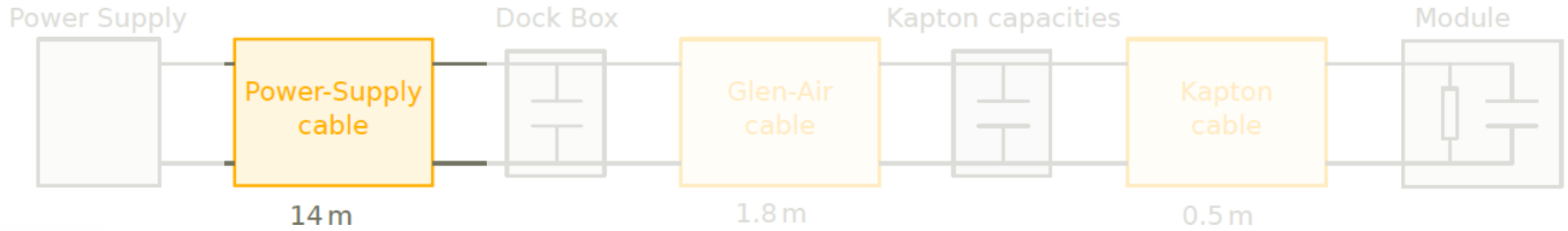
SIGNAL PATH



[1]

- 23 different voltages required for operation
- DC/DC converters
- Dedicated power-up and power-down sequence

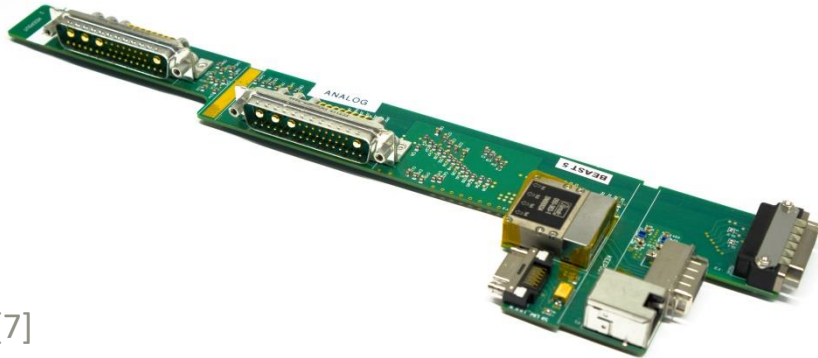
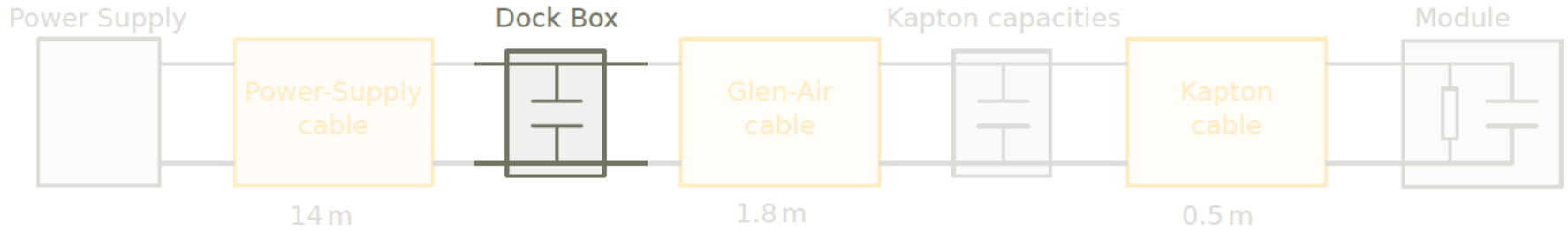
SIGNAL PATH



- Two Power-Supply cables (PS-cables)
- 30 conductors with four different wire gauges (given in AWG)

[7]

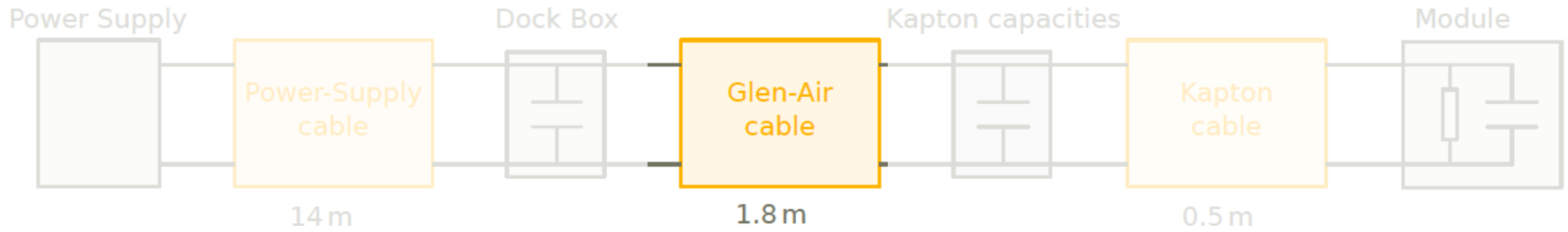
SIGNAL PATH



- Joins power cables and data cables
- Decoupling capacitors on almost every line

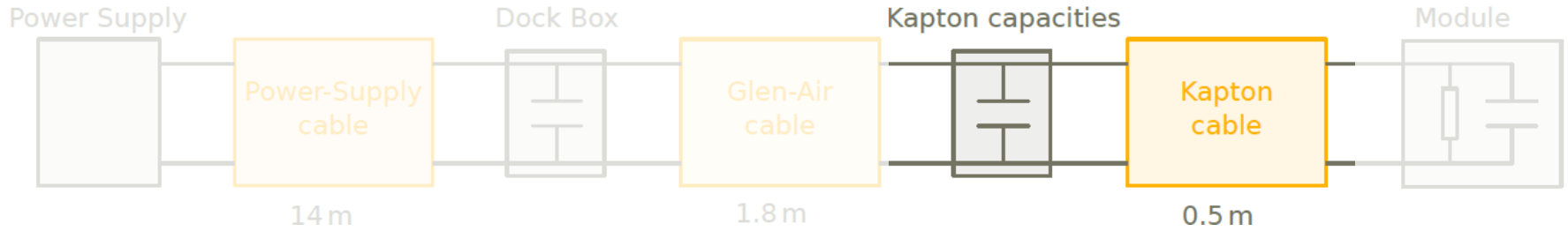
[7]

SIGNAL PATH



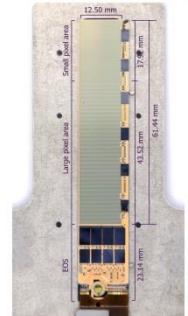
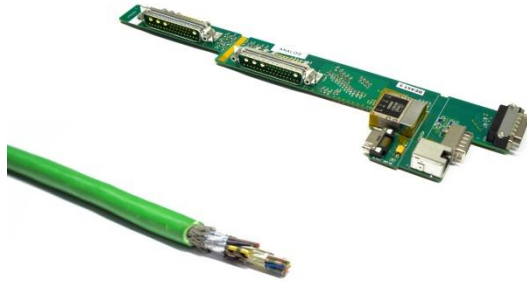
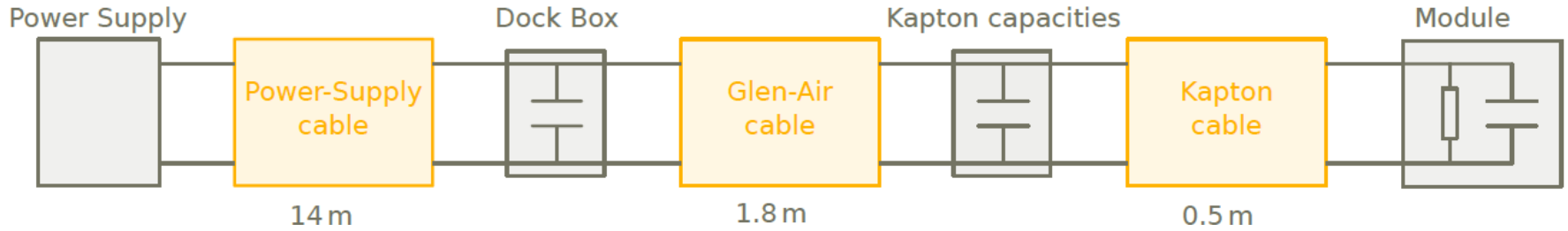
- Glen-Air cable (GA-cable): 51 identical cores
- Terminates in Patch Panel (PP)

SIGNAL PATH



- Kapton flex cable
- Rigid PCB area with capacitors to ground lines
- Attachment to module via wire bonds

SIGNAL PATH



[1]

CABLE CHARACTERISTICS

- Characteristics proportional to cable length:

Resistance

- DC –Resistance
- Skin-effect $\propto \sqrt{f}$
- Proximity-effect $\propto \sqrt{f}$
- **No phase shift** between current and voltage

Inductance

- Mutual inductance
 - Magnetic field of neighbouring conductors
- Self inductance ($\propto \sqrt{f}$)
 - Magnetic field within the conductor
- **Phase shift** between current and voltage

Capacitance

- Conductors store charge and discharge it when opposed to AC
- **Phase shift** between current and voltage

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Inductance

- Mutual inductance
 - Magnetic field of neighbouring conductors
- Self inductance ($\propto \frac{1}{\sqrt{f}}$)
 - Magnetic field within the conductor
- **Phase shift** between current and voltage

Capacitance

- Conductors save charge and discharge it when opposed to AC
- **Phase shift** between current and voltage

CABLE CHARACTERISTICS

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Inductance

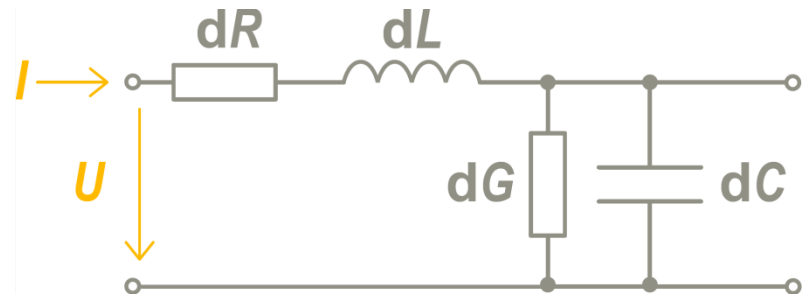
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Capacitance

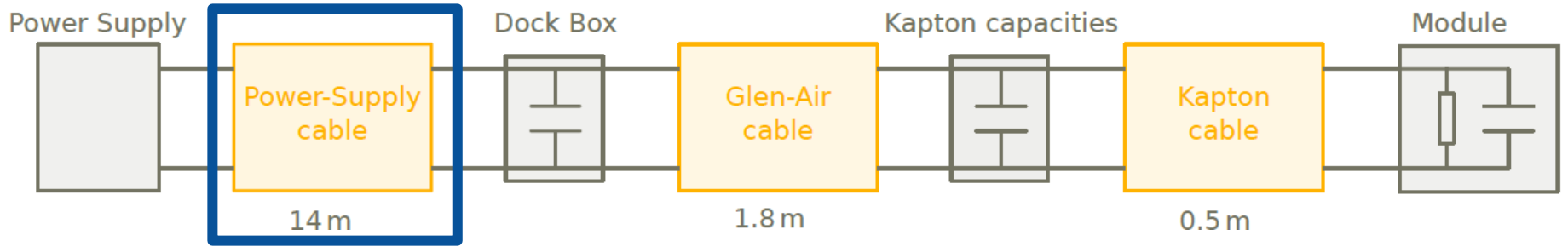
- Conductors save charge and discharge it when opposed to AC
- **Phase shift** between current and voltage

TRANSMISSION LINE THEORY

- Equivalent circuit diagram of a cable
 - dR , dL , dG and dC per **cable segment dl**
 - Complete cable: cascade of equivalent circuit diagrams
- **Impedance:** relation between *complex* voltage and current
- $Z = \sqrt{\frac{i\omega \cdot L' + R'}{i\omega \cdot C' + G'}}$ where $X' = \frac{X}{l}$

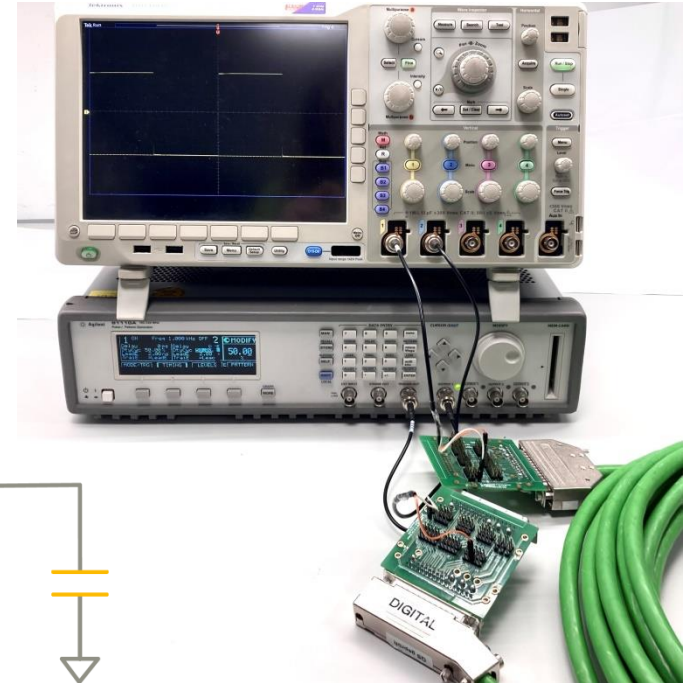
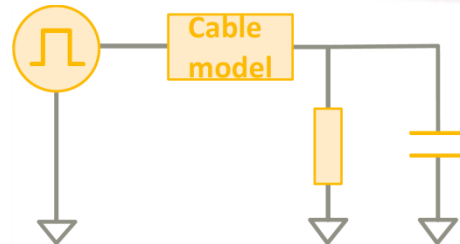


CABLE MODEL



SIMULATION VERIFICATION

- Comparison with **measurement** to verify
 - **Falling edge** of a squared pulse
 - Function generator used for creating squared pulse
 - View transmitted signal on oscilloscope
- Verify each cable segment **individually**
- For quantification:
 - Compute **difference in voltage** between simulation and measurement data
 - Both data sets are interpolated linearly



CABLE MODELS

Ltline

→ LTSpice

- Inductance
- Capacitance
- DC-Resistance

Simple Line

→ HyperLynx

- Impedance
- Delay time
- DC-Resistance

S2spice

→ LTSpice

- S-Parameters

S-Parameter

→ HyperLynx

- S-Parameters

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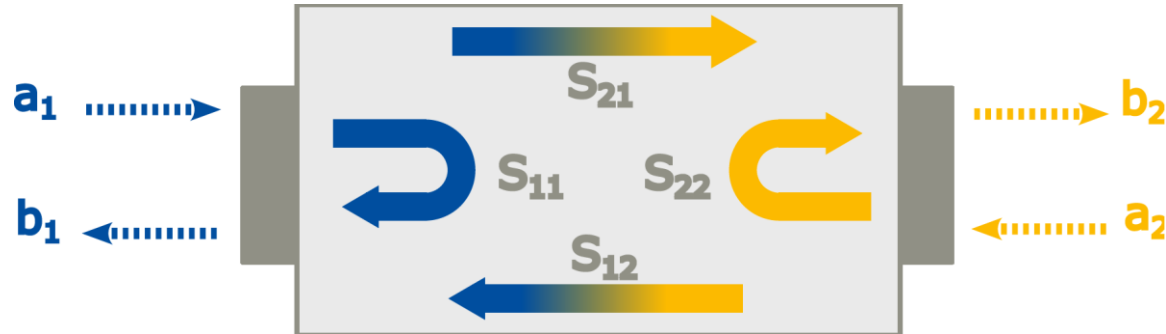
- S-Parameters

S-PARAMETERS

- Describe electrical behaviour of cable
- Measure **incoming** (\vec{a}) and **outgoing** (\vec{b}) wave for various frequencies
- Magnitude and phase information
- 2-port measurement:
 - Port 1: Cable Input
 - Port 2: Cable Output

$$S_{11} = \frac{b_1}{a_1} \quad S_{12} = \frac{b_1}{a_2}$$

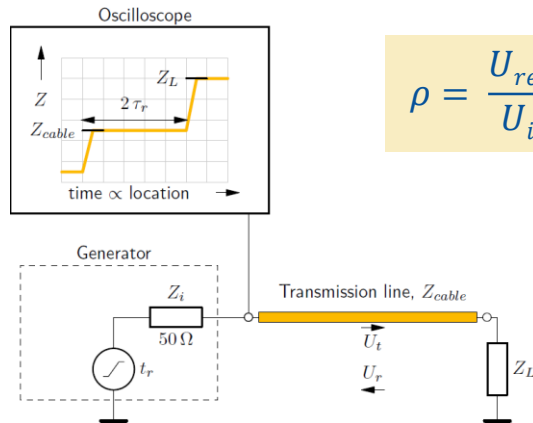
$$S_{21} = \frac{b_2}{a_1} \quad S_{22} = \frac{b_2}{a_2}$$



TIME DOMAIN REFLECTOMETER (TDR) VS VECTOR NETWORK ANALYSER (VNA)

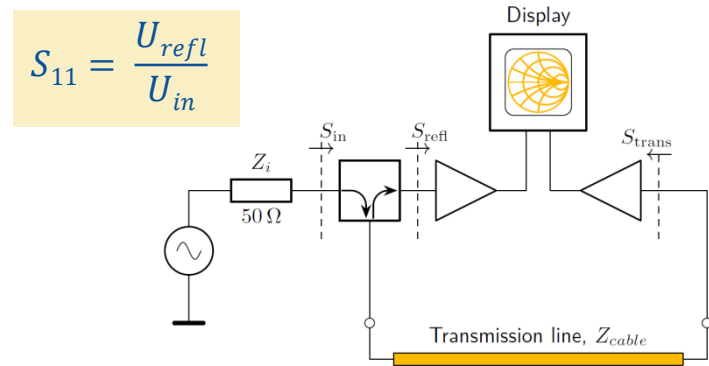
TDR

- **Time** domain → Fast Fourier Transform
- Reflection at open cable end (and transmission)
- **Step** signal as stimulus
- Measures reflection coefficient ρ

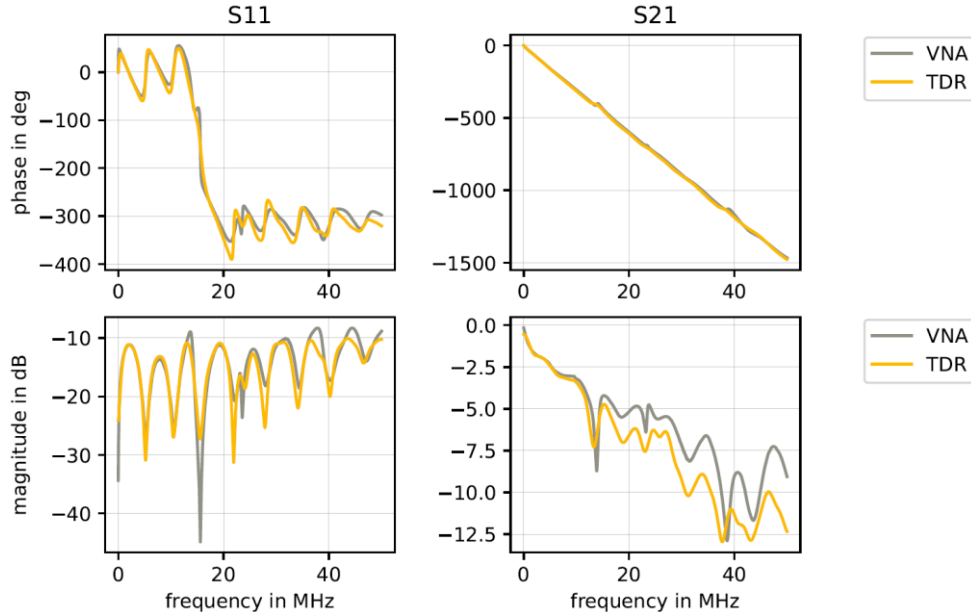


VNA

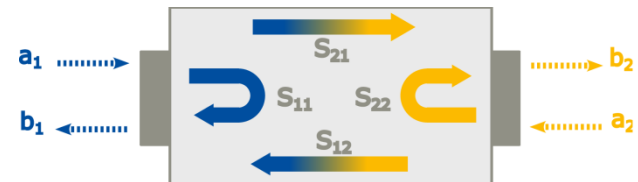
- **Frequency** domain
- Reflection and transmission
- **Sine** wave as stimulus
- Measures S-parameters



TDR VS VNA: S-PARAMETERS

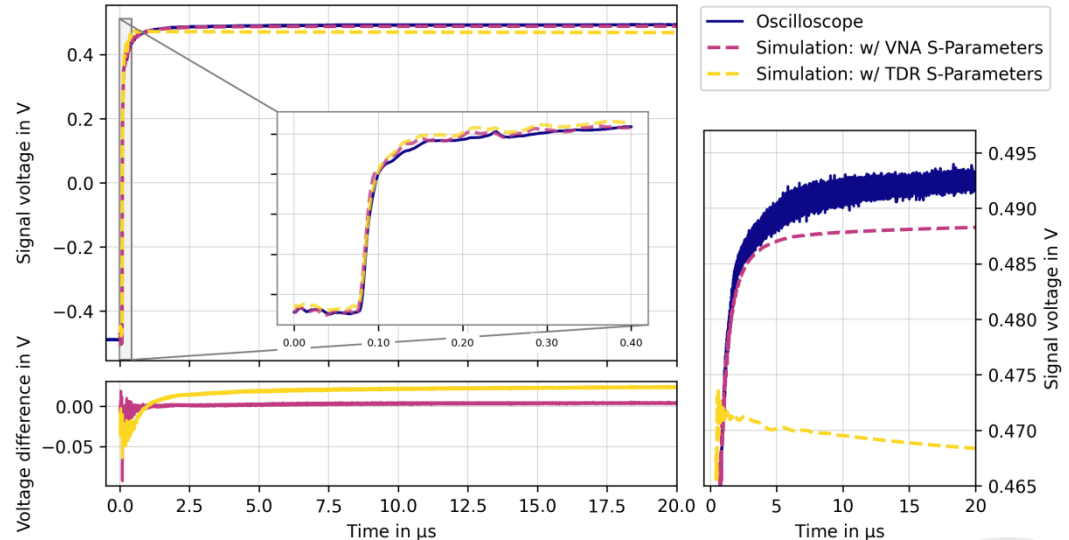


- Example for 26 AWG-line in PS-cable
- Reflection measurement (S11):
 - Slight **shift in phase**
- Transmission measurement (S21):
 - Magnitudes diverge
 - **Higher dampening for TDR S-parameters**



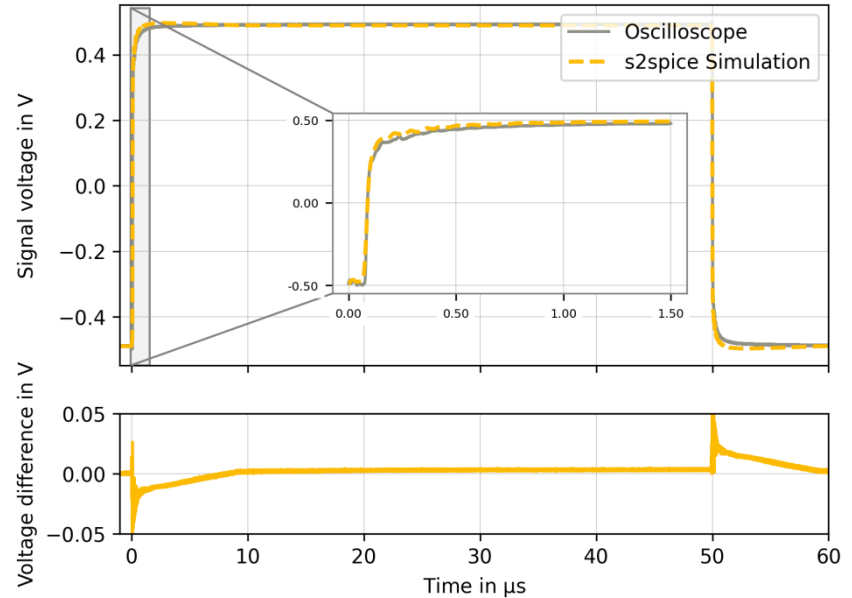
S-PARAMETER SIMULATION: TDR VS VNA

- Simulation of Bulk-line in PS-cable
- HyperLynx S-parameter model in simple transmission setup
- Good agreement in **rising edge** for both measurements (TDR and VNA)
- **Amplitude differs** by ~20 mV
- Higher damping for TDR-measurement
- Physical setup is **better described by VNA S-parameters**



S2SPICE MODEL

- No direct possibility to include S-parameters in LTSpice → Create own cable model
 - Based on **voltage dependent voltage sources**
 - On first glance: good match with physical setup
 - Average voltage deviation (0-40 μs): 3.94 mV
 - On second glance: deviation in result **with change in simulation time**
 - Could also be observed with a single voltage dependent voltage source
- Only suitable if simulation can be verified and simulation time can be adjusted flexibly



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Simple Line

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S2spice

→ LTSpice

- S-Parameters

S-Parameter

→ HyperLynx

- S-Parameters

R_{DC} , L & C VALUES

- **Four-wire sensing for DC-resistance**
- Extract inductance and capacitance from **S-parameter** measurement
- Result: **frequency dependent values** per length unit
- Example: different lines of PS-cable
 - \uparrow AWG \Rightarrow \downarrow cross section
- For cable model: **average** over frequency

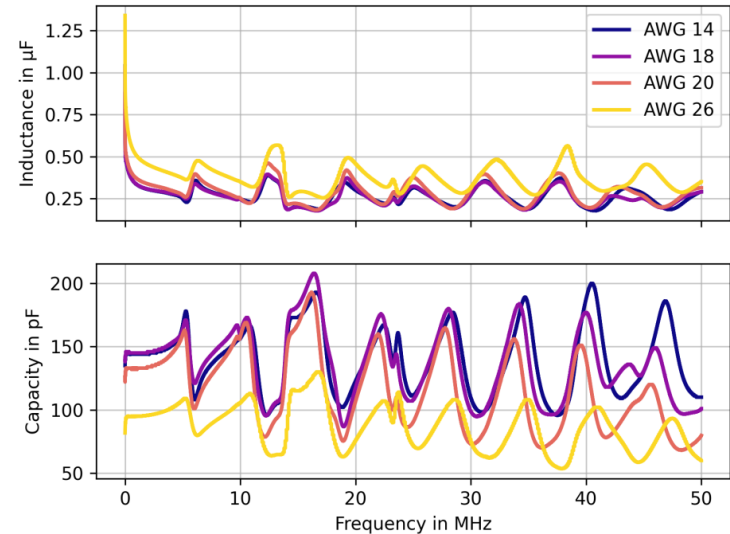


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For comparison: **two-wire system** (radii r , distance d)

$$L' = \frac{\mu}{4\pi} + \frac{\mu}{\pi} \ln\left(\frac{d}{\sqrt{r_1 r_2}}\right)$$

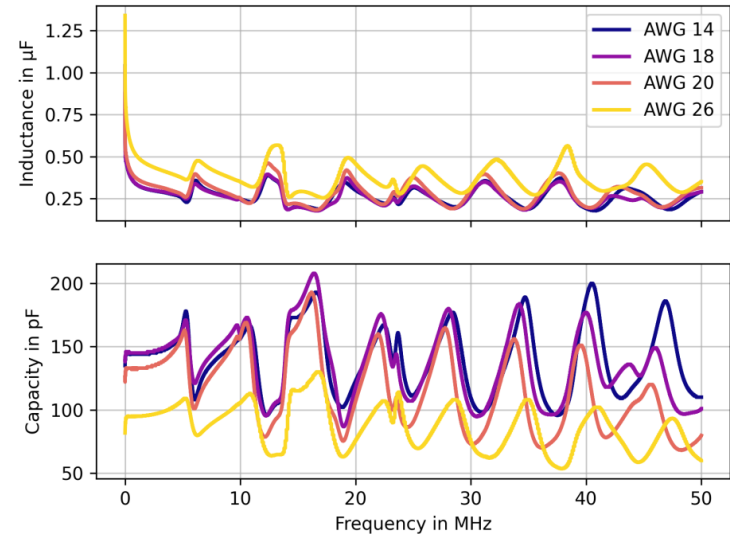
[8]

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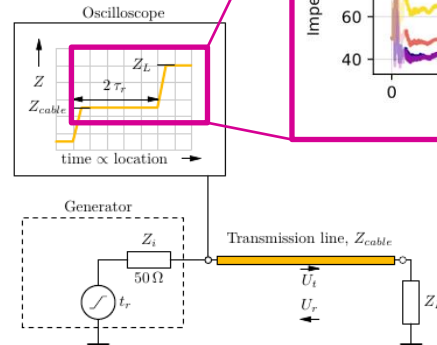
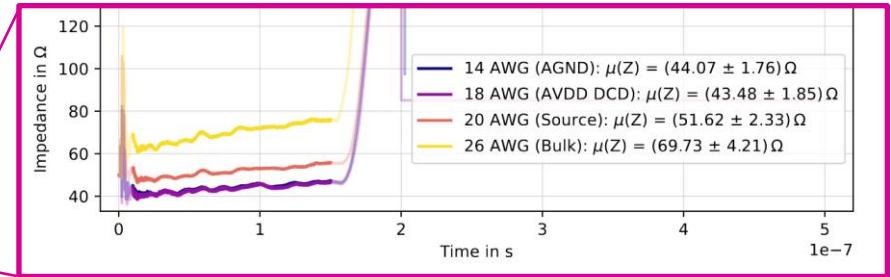
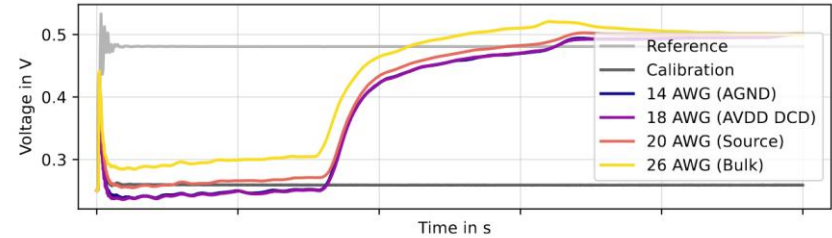
For comparison: **plate capacitor** (area A , distance d)

$$C = \frac{\epsilon A}{d}$$

[9]

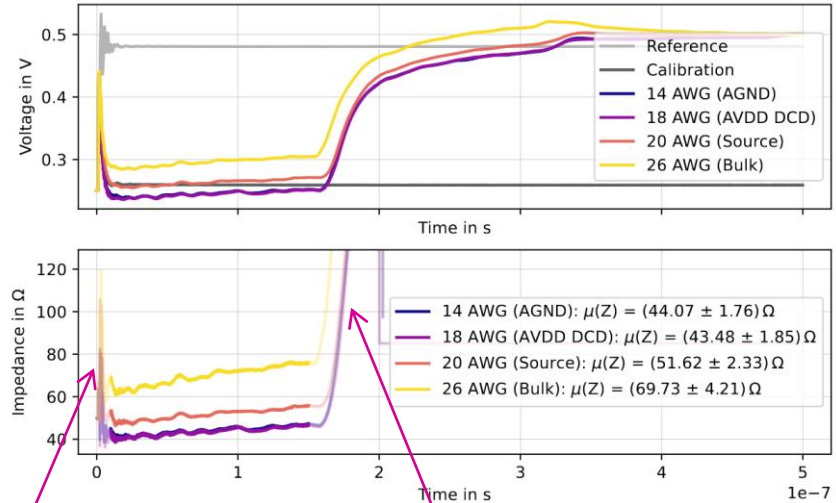
DELAY TIME AND IMPEDANCE

- Needed for Simple Line model
- Use **TDR**: reflection at open cable end
- **Impedance profile**: view cable as cascade of cable segments
 - Reflection at cable connection
 - Average over cable length
 - Rise in impedance due to DC-resistance
- **Delay time**: $\tau_l = (75.5 \pm 0.5) \text{ ns}$



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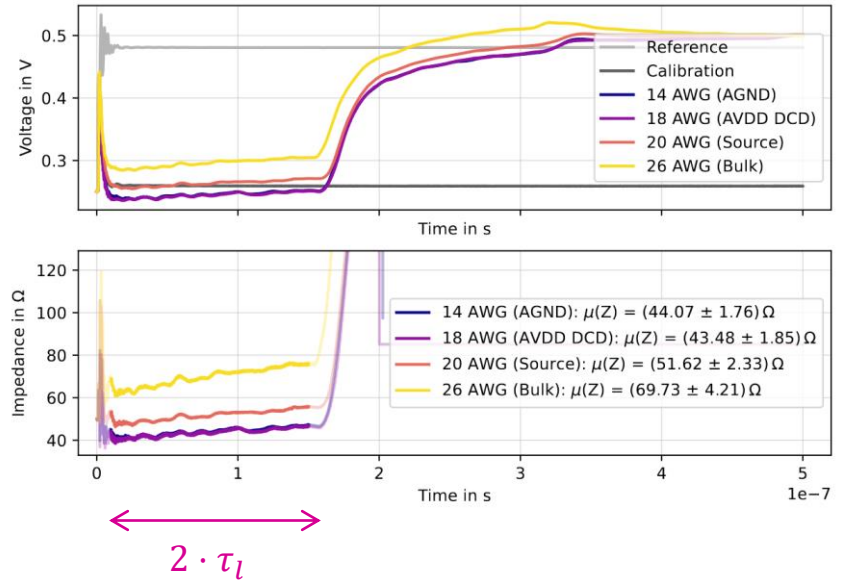


Reflection at cable connection

Open cable end

DELAY TIME AND IMPEDANCE

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LTSPICE LTLINE & HYPERLYNX SIMPLE LINE MODEL

- Simulation model using measured parameters
- **Rising edge** is not captured accurately
- **BUT** looking at nanosecond regime
- Average voltage deviation (not including falling edge)
 - Ltline: 3.11 mV for 0-40 μ s
 - Simple Line: 3.38 mV for 0-40 μ s

Ltline

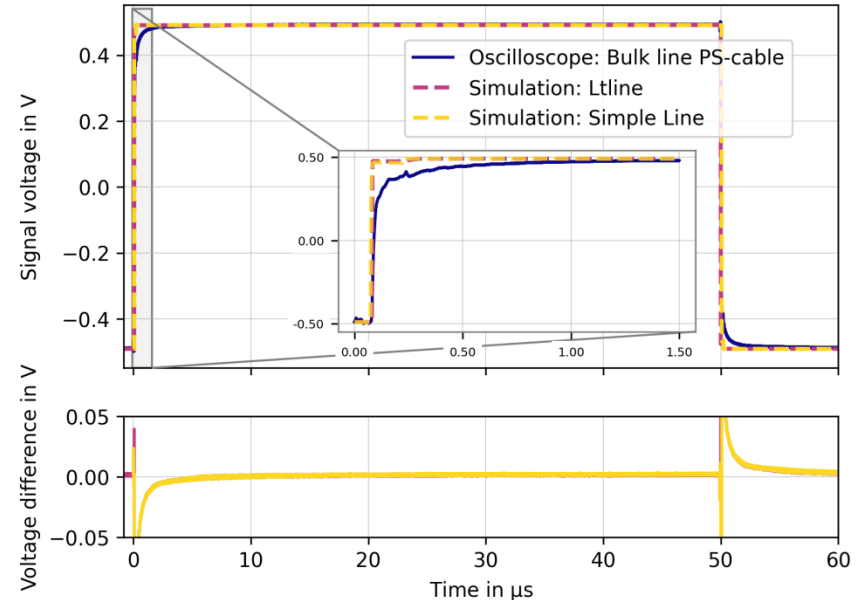
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- Inductance
- Capacitance
- DC-Resistance

Simple Line

→ HyperLynx

- Impedance
- Delay time
- DC-Resistance

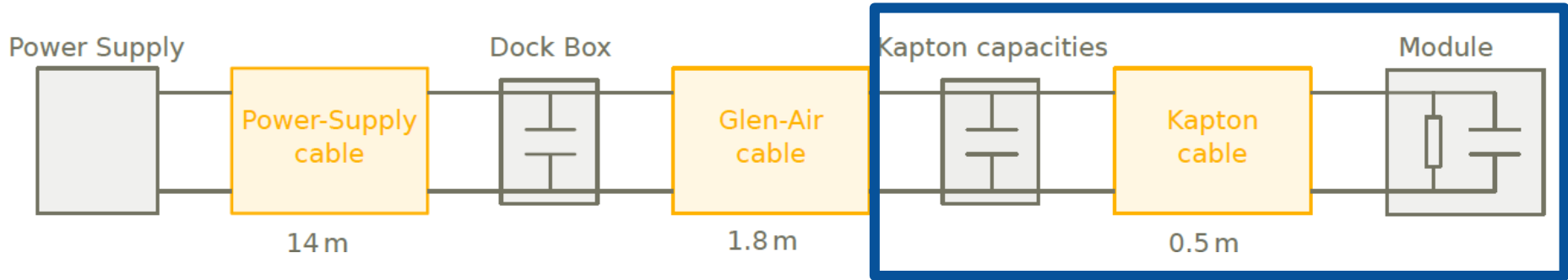


SIMULATION METHODS

LTSpice: Ltlime model	HyperLynx: Simple Line model	LTSpice: s2spice model	HyperLynx: S-parameter model
<ul style="list-style-type: none"> • Frequency independent values as input 	<ul style="list-style-type: none"> • Frequency independent values as input 	<ul style="list-style-type: none"> • Frequency dependent S-parameters 	<ul style="list-style-type: none"> • Frequency dependent S-parameters
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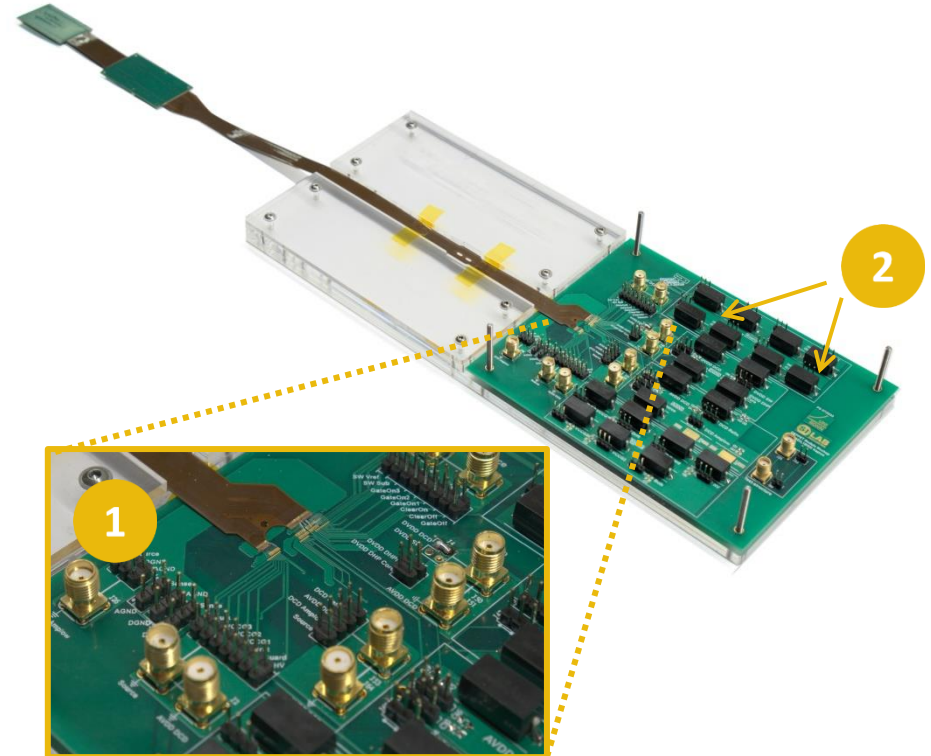
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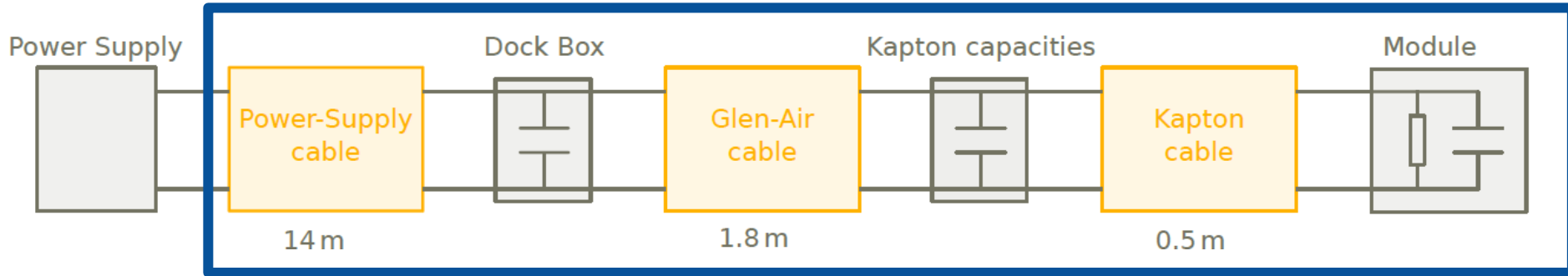
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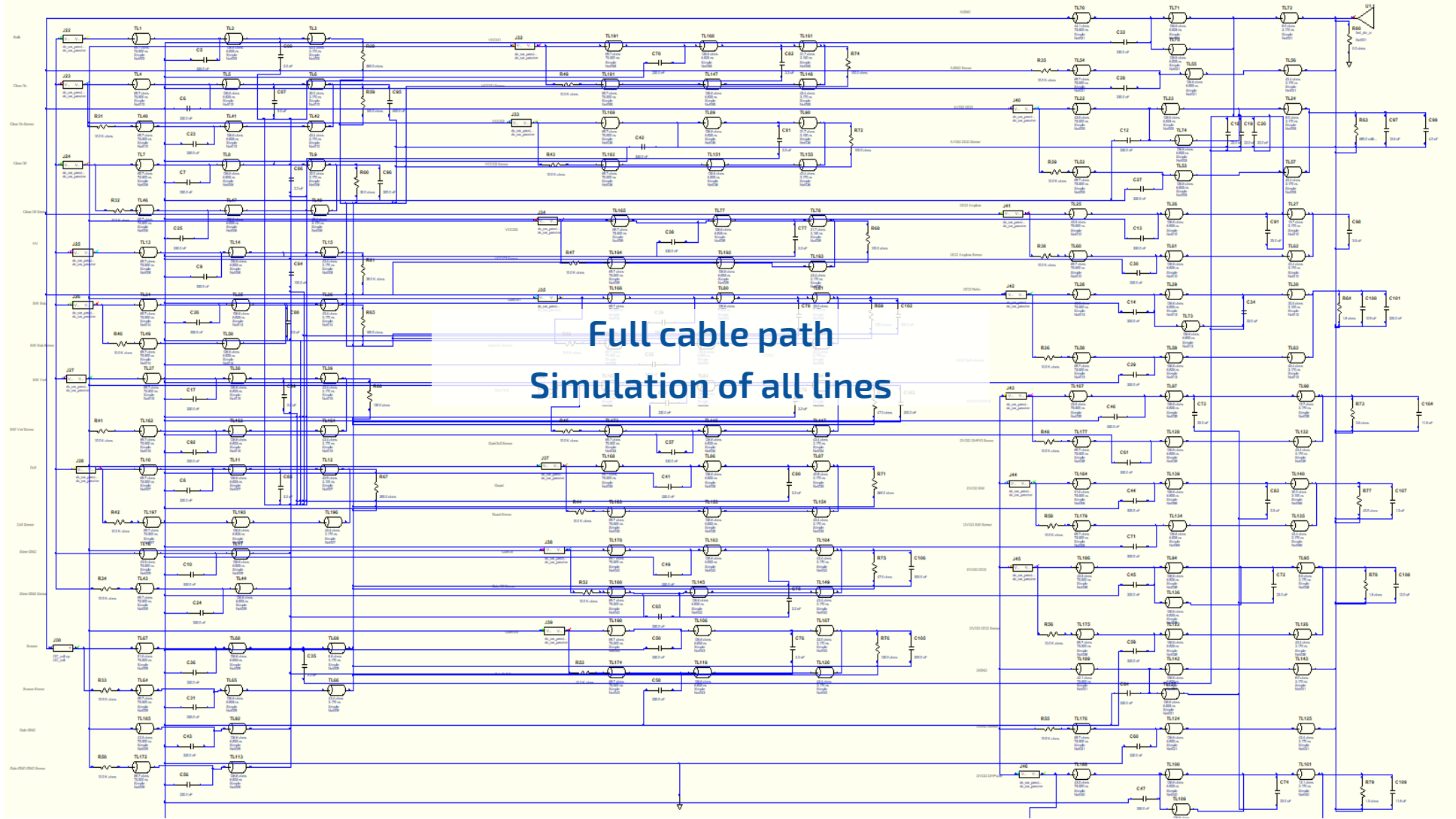
MODULE MOCKUP

- Verification of simulation: **Module mockup PCB**
 - Connection to all of the lines of Kapton (1)
 - Wire bonding necessary
 - Module mockup (2)
 - Resistors and capacitors mimic module properties after the Kapton connection



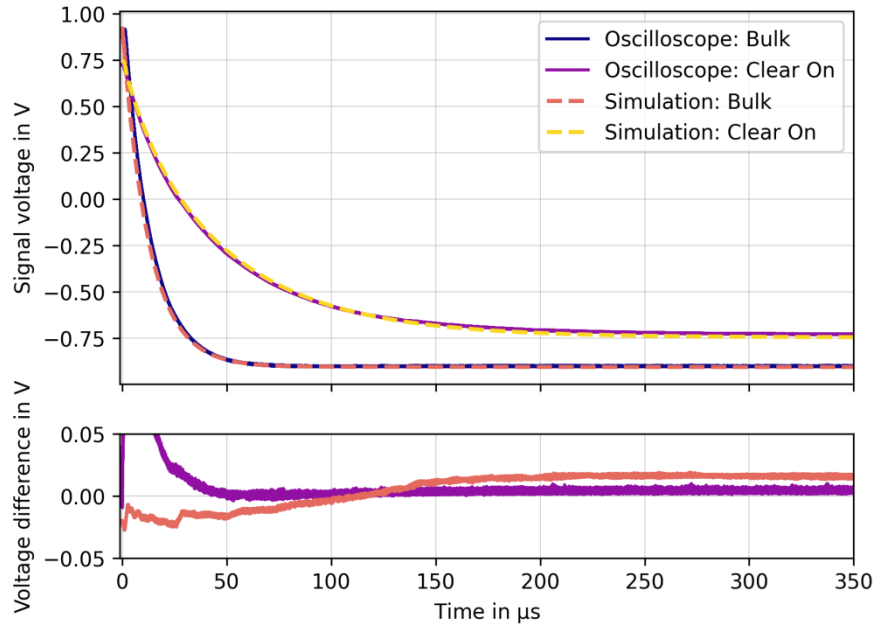


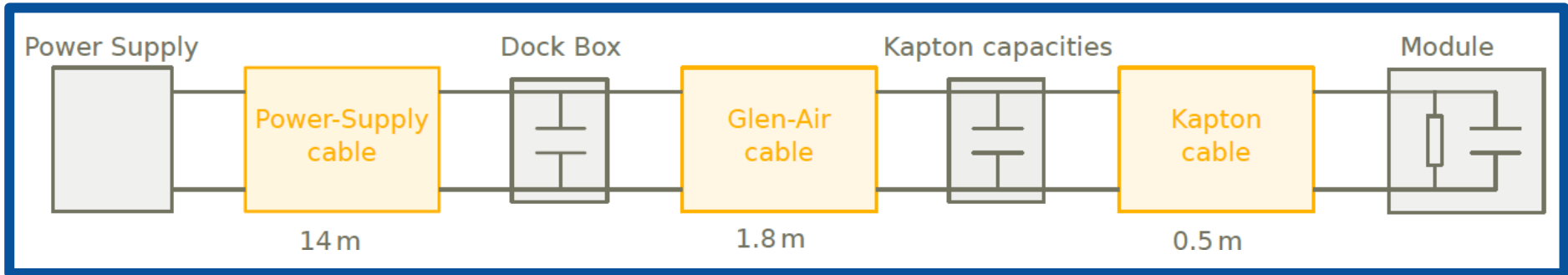
Full cable path
Simulation of all lines



FULL CABLE PATH: POWERING OF TWO LINES

- Not only powered lines need to be simulated because of **capacitive coupling**
- Replication of load with custom made PCB
- Average voltage deviation:
 - Bulk line.: 8.7 mV
 - Clear On line: 13.26 mV

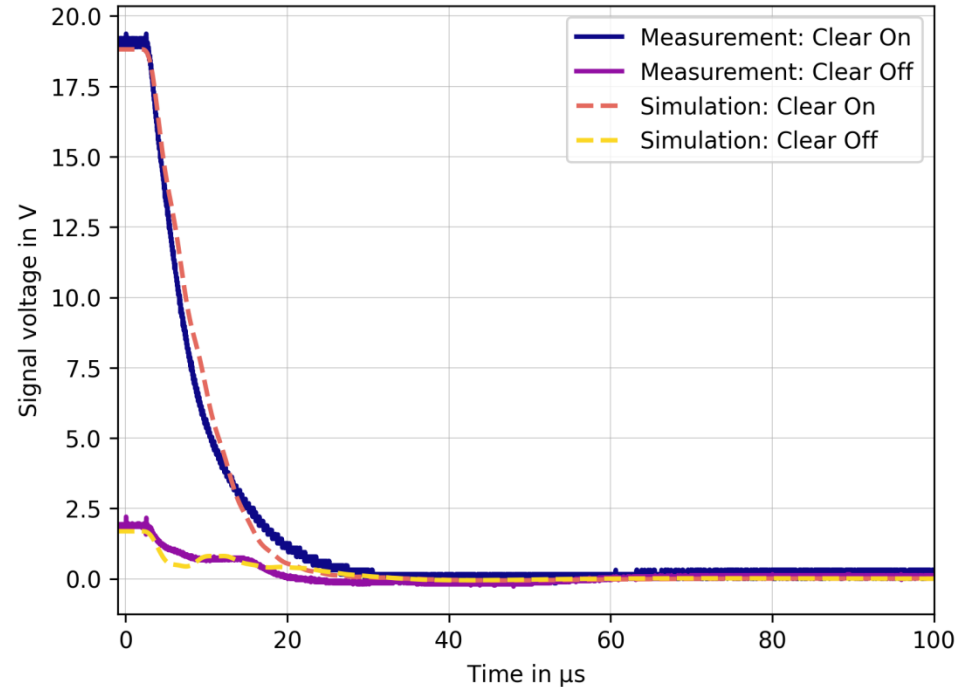
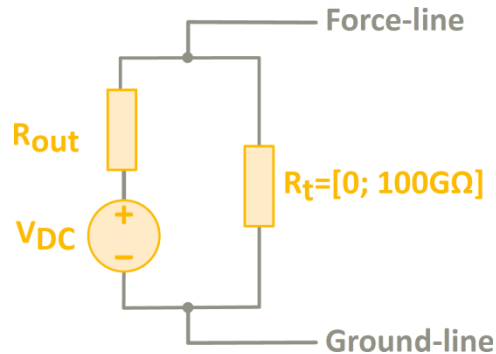




SHUTDOWN PROCEDURE

ACTIVE SHUTDOWN

- Active shutdown → **short** force and ground line
- Simulate by **time dependent resistor** which switches from $100\text{ G}\Omega$ to $0\ \Omega$



SUMMARY AND CONCLUSION

- Goal is **prevention of switcher damage** in beam loss events
- Fast shutdown → avoid power-down sequence violation
- Testing of **different cable models**
- Promising results of full simulation with **Simple Line model**
 - Physical measurement can be replicated by simulation
- $V_{clear\ on} < V_{clear\ off}$

→ Use Simulation to determine optimal resistance value on Fast Shutdown Board

THANK YOU!

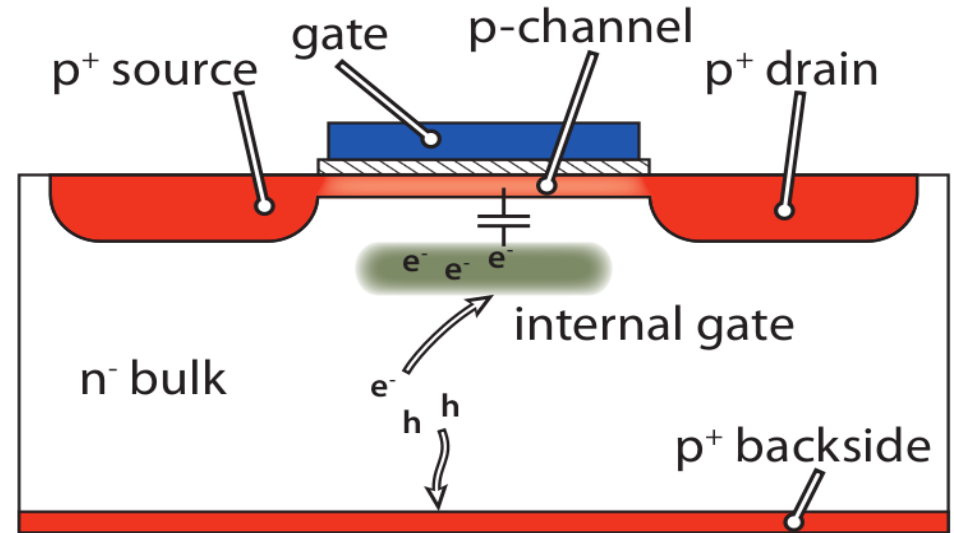
SOURCES

Number	Slide	Description	Source
[1]	3, 11, 16	Super KEKB, Belle II	P. Ahlburg. Development of a Laboratory Readout System for DEPFET Pixel Detector Modules and Investigation of Radiation Backgrounds at the SuperKEKB Accelerator
[2]	4	Picture Belle II	F. Müller. „Characterization and Optimization of the Prototype DEPFET Modules for the Belle II Pixel Vertex Detector“. PhD thesis. Ludwig-Maximilians-Universität München, 2017
[3]	4	Picture DEPFET Pixel	M. Koch. „Development of a Test Environment for the Characterization of the Current Digitizer Chip DCD2 and the DEPFET Pixel System for Belle II Experiment at SuperKEKB“. PhD thesis, Uni Bonn, 2011
[4]	5,6,8	Fast Shutdown Studies	Jannes Schmitz. „Irradiation Burst Studies on Belle II PXD Module Components“. Master’s thesis. Rheinische Friedrich-Wilhelm-Universität, 2020
[5]	9	Hitmap Fast Shutdown	P. Leitl

SOURCES

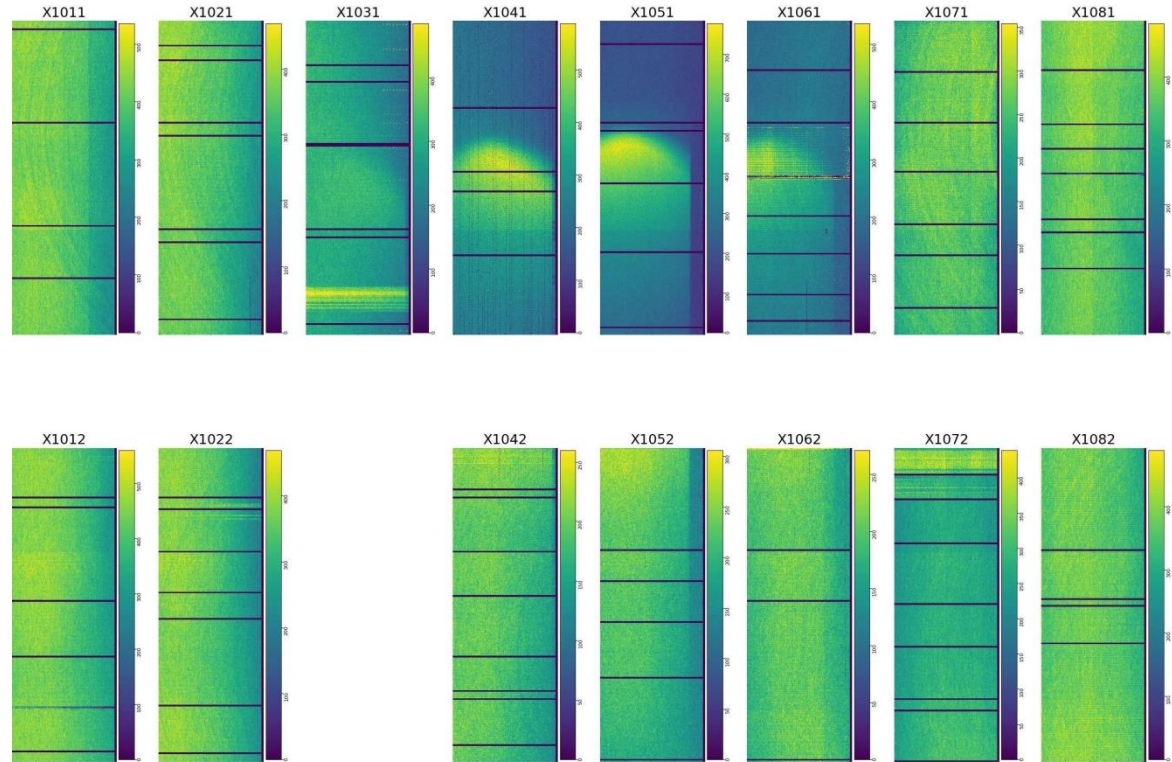
Number	Slide	Description	Source
[6]	10	Photo Belle II	B. Paschen
[7]	12, 13	Photo PS-Cable Fast Shutdown	C. Bospin
[8]	32	Inductance formula	H. Katzier. „Elektrische Kabel und Leitungen“. Eugen G. Leuze Verlag, 2015
[9]	33	Equation formula	M. Albach. „Elektrotechnik“. Pearson Education, 2011

- Size : 50 x 55 x 75 μm^3
- P-channel MOSFET on depleted Bulk
- n^+ -doped internal gate
- n^+ -doped Clear
- \rightarrow detection of particles and amplification



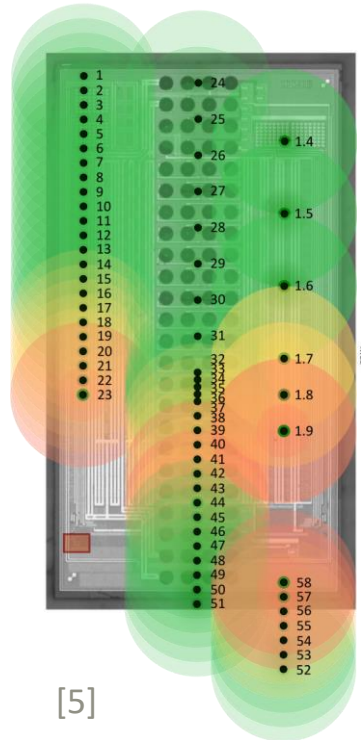
AFTER BEAM LOSS EVENT

- 89 inefficient Switcher channels (→ 89x4 matrix rows)
- 15 modules of inner layer: 192x15=2880 Switcher channels

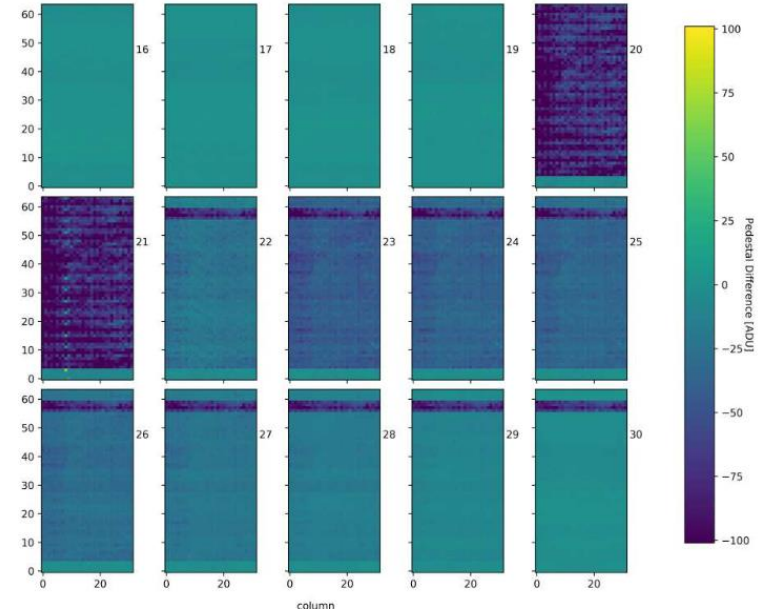


CONFIRMATION OF RESULTS

- Irradiation with electron beam
- Fine scan of ASIC area
 - July 2020 with H5029
 - Colour coded measurement points
 - red => permanent damage
- Raw data difference of 15 raw frames during injection
 - Second to last Switcher channel is damaged permanently
- Switcher only vulnerable when turned on



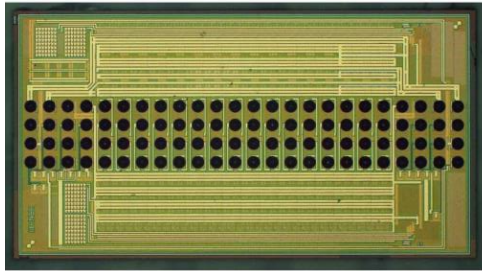
[5]



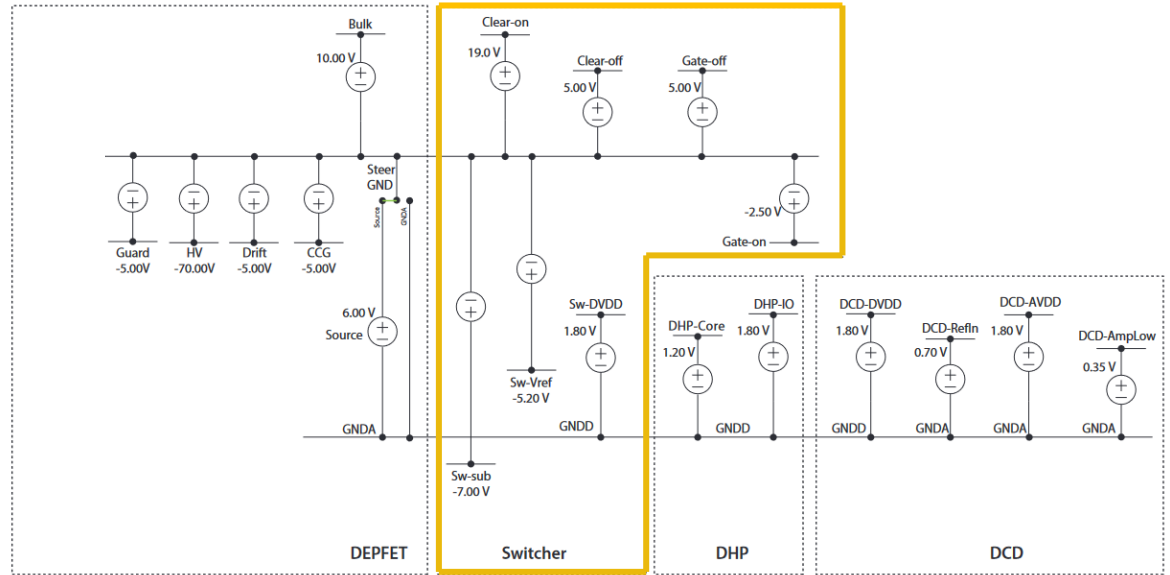
[6]

POWERING SCHEME

- Dedicated power-up and power-down sequence
- Range between +19V and -7V
- Switcher switches between high voltages



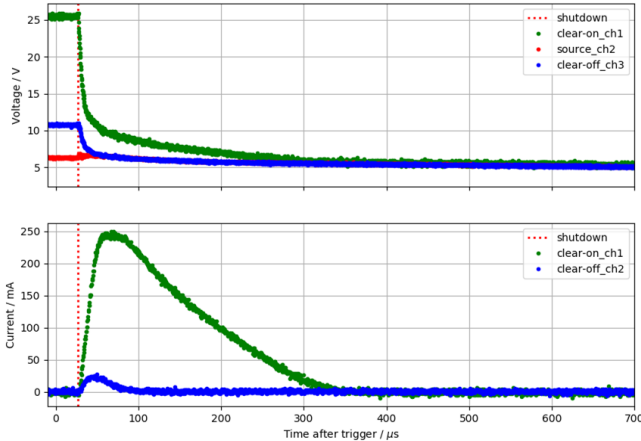
[7]



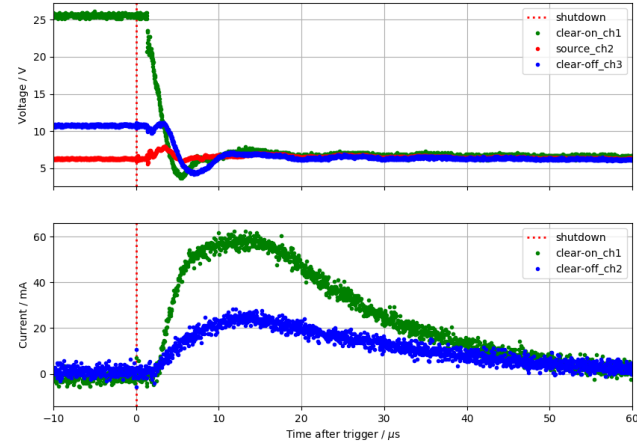
[8]

FAST SHUTDOWN MEASUREMENT

- Example: shutdown of voltage required for Switcher (Clear-on/ Clear-off), measured at Power Supply



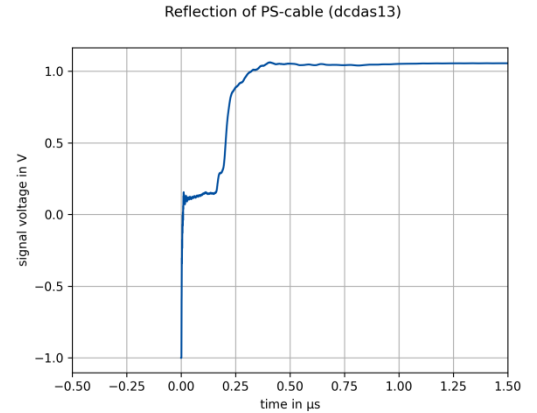
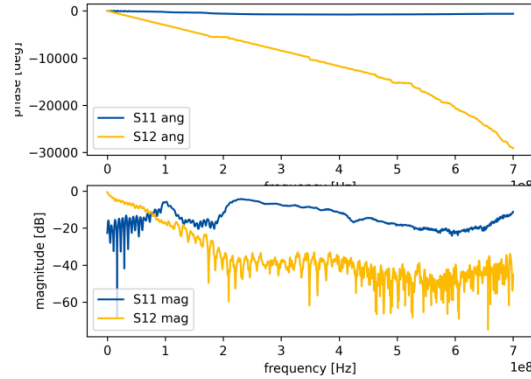
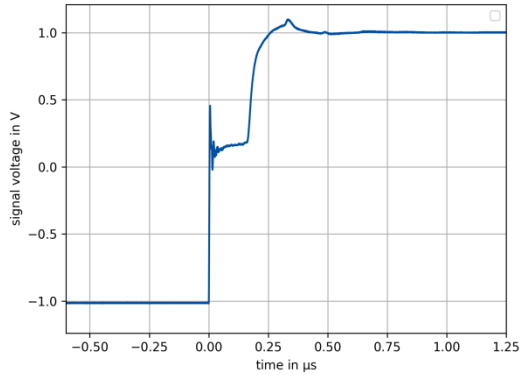
- $R_{\text{clear-on}} = 10 \Omega$, $R_{\text{clear-off}} = 10 \Omega$
- Decreased shutdown time
- Influence of FET visible



- $R_{\text{clear-on}} = 0 \Omega$, $R_{\text{clear-off}} = 0 \Omega$
- $V_{\text{clear-on}}$ drops below $V_{\text{clear-off}}$ \rightarrow violation of shutdown sequence

SIMULATION PROCESS

➔ Example: Reflection at open cable end (HyperLynx and s2spice-model)



Measure with **time domain** reflectometer



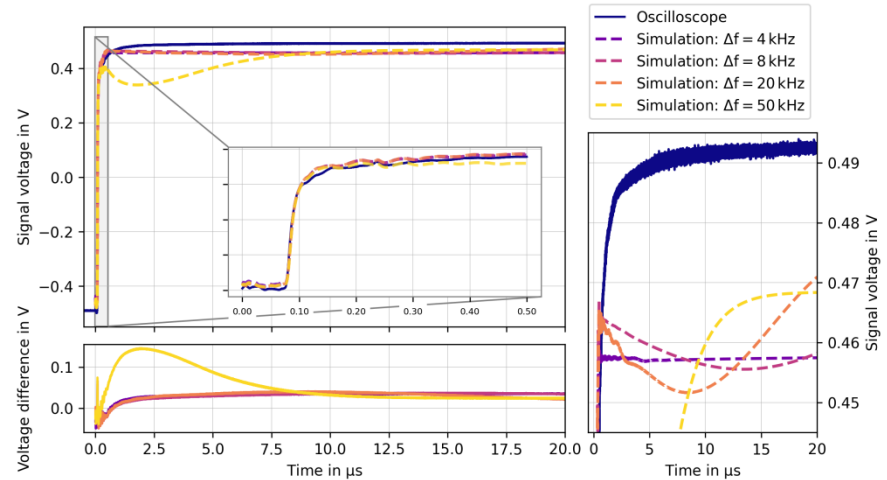
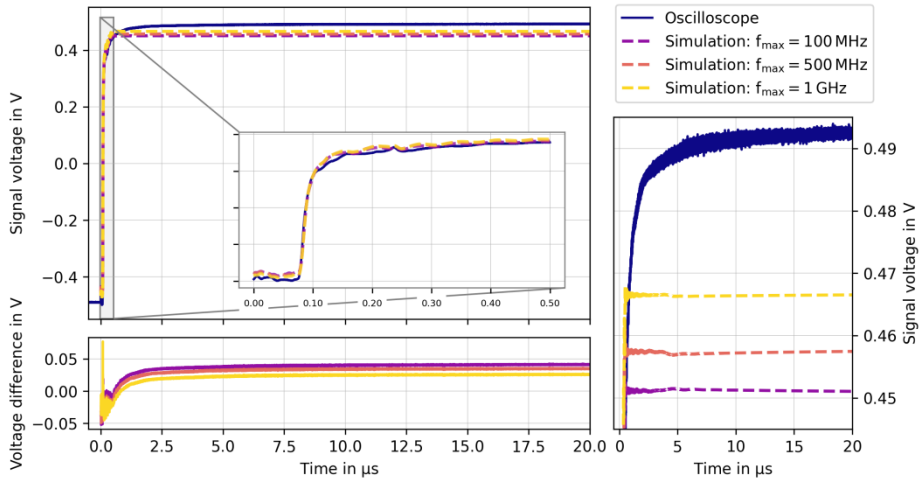
Fourier transformed into **frequency domain**

➔ Scattering Parameters



Use S-parameters in **time-domain** transient simulation

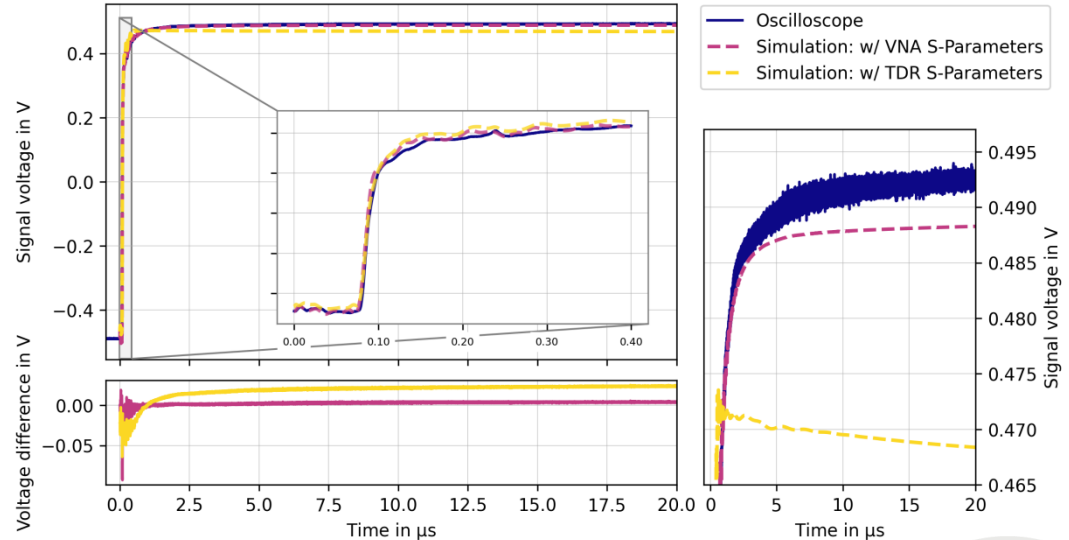
TDR S-PARAMETER SIMULATIONS



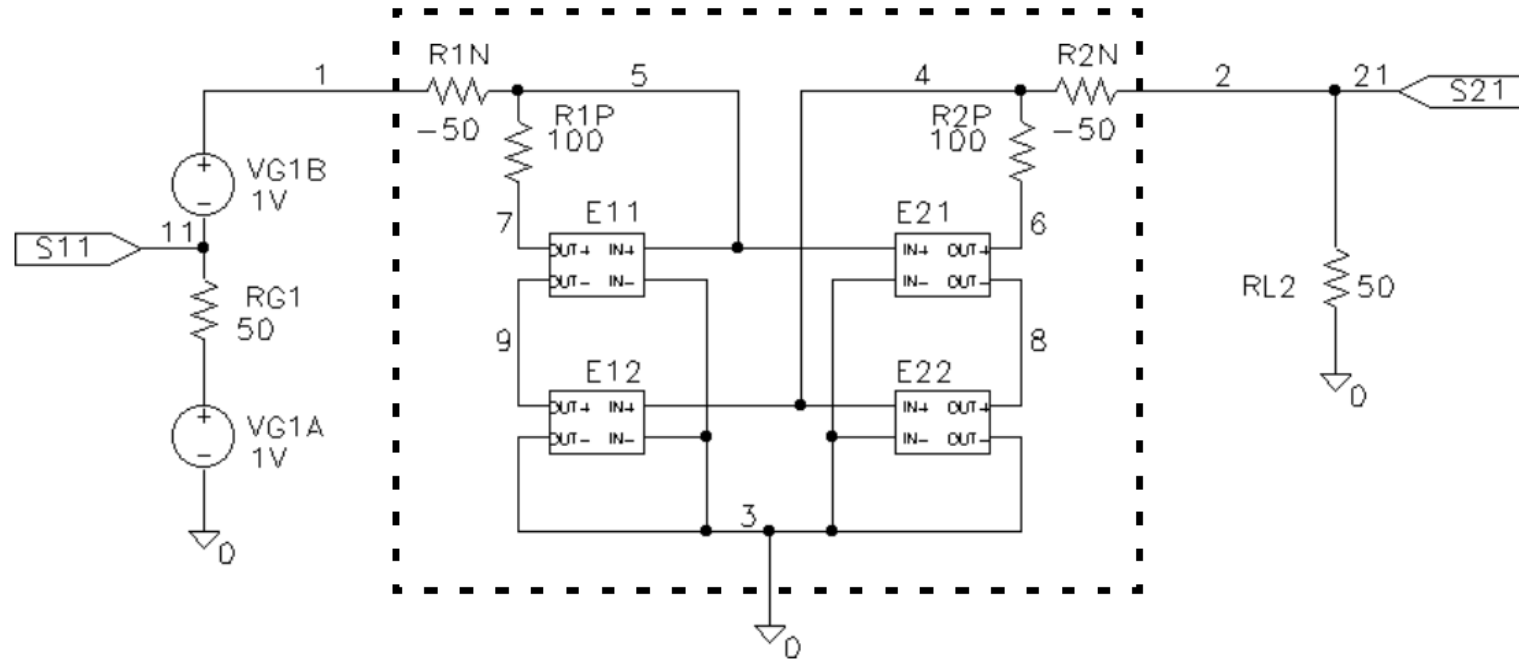
S-PARAMETER SIMULATION: TDR VS VNA

- Simulation of Bulk-line in PS-cable
- HyperLynx S-parameter model in simple transmission setup
- Voltage Deviation

Time window	VNA	TDR
0 – 40 μ s	3.8 mV	22.8 mV
0 – 1.5 μ s	4.28 mV	14.1 mV
1.5 μ s – 40 μ s	3.81mV	23.1mV

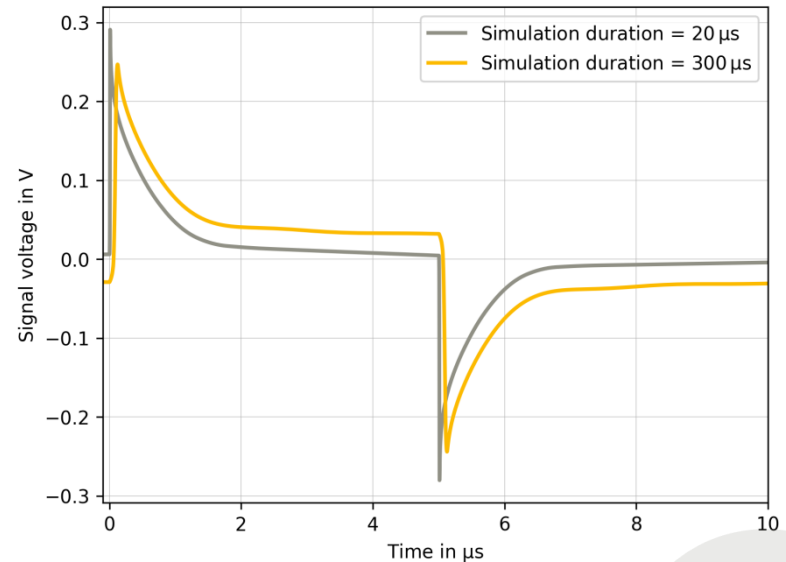


S-Parameter Subcircuit



S2SPICE PROBLEM

- Smallest segment of cable model: voltage dependent voltage source
 - Shows **same behaviour**
- Only suitable if simulation can be verified and simulation time can be adjusted flexibly

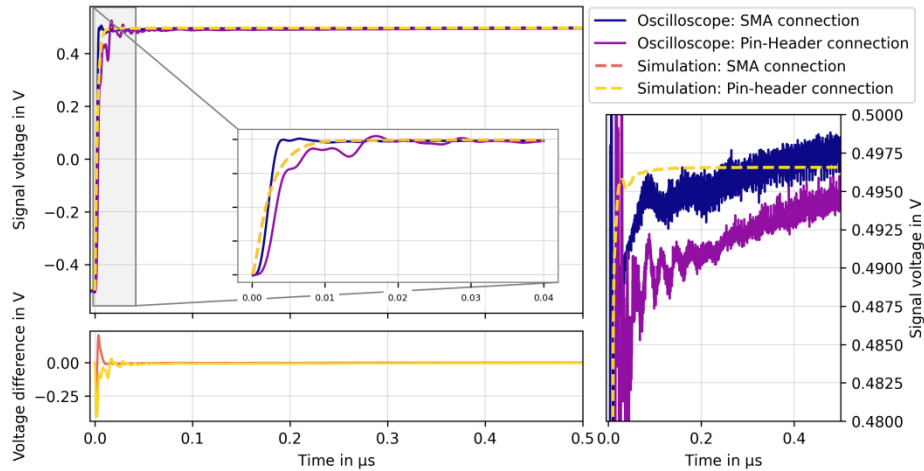


S2spice

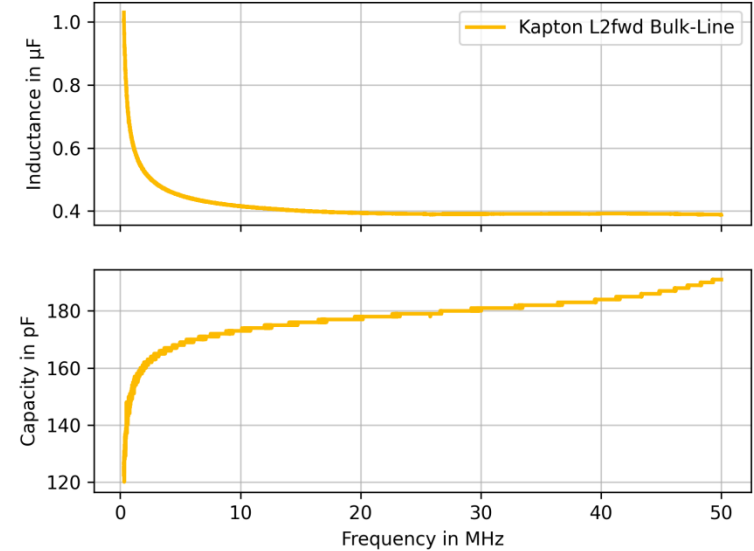
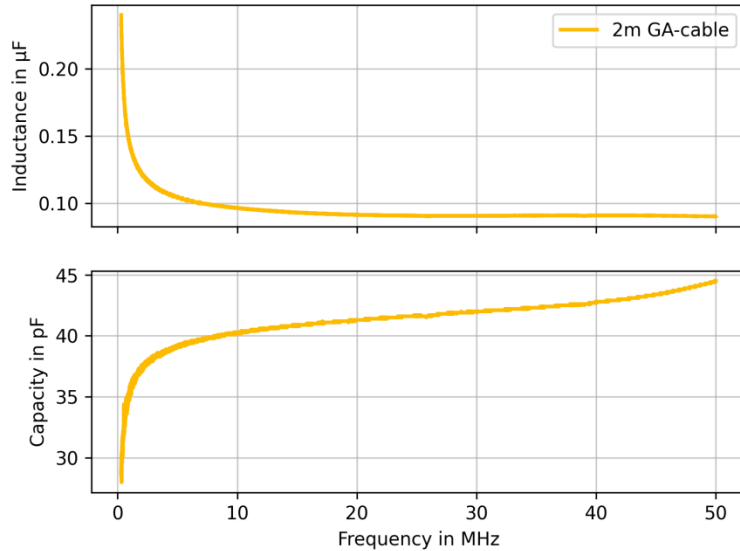
→ LTSpice

• S-Parameters

PIN HEADER VS SMA



INDUCTANCE AND CAPACITANCE OF GA AND KAPTON



$$L_{AWG\ 26} = (379.25 \pm 81.1) \text{ nH}$$

$$L_{AWG\ 20} = (288.6 \pm 67.68) \text{ nH}$$

$$L_{AWG\ 18} = (262.69 \pm 54.40) \text{ nH}$$

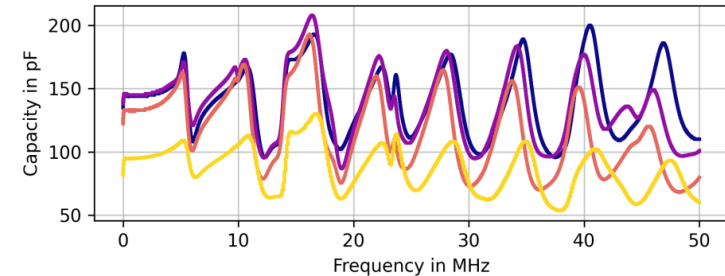
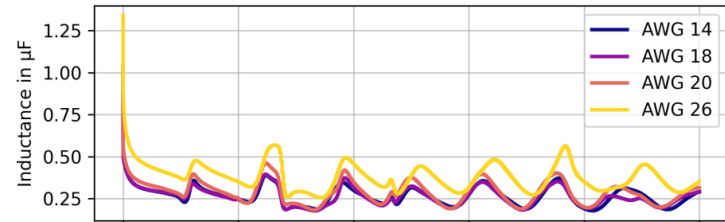
$$L_{AWG\ 14} = (265.34 \pm 54.43) \text{ nH}$$

$$C_{AWG\ 26} = (86.92 \pm 17.9) \text{ pF}$$

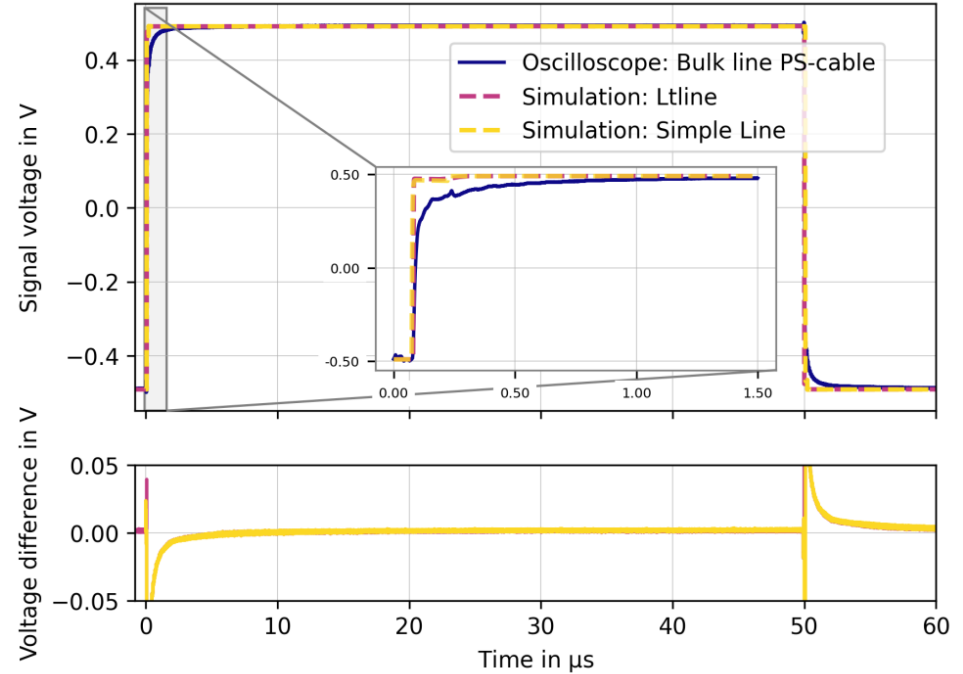
$$C_{AWG\ 20} = (115.63 \pm 31.09) \text{ pF}$$

$$C_{AWG\ 18} = (137.13 \pm 27.89) \text{ pF}$$

$$C_{AWG\ 14} = (139.72 \pm 26.71) \text{ pF}$$

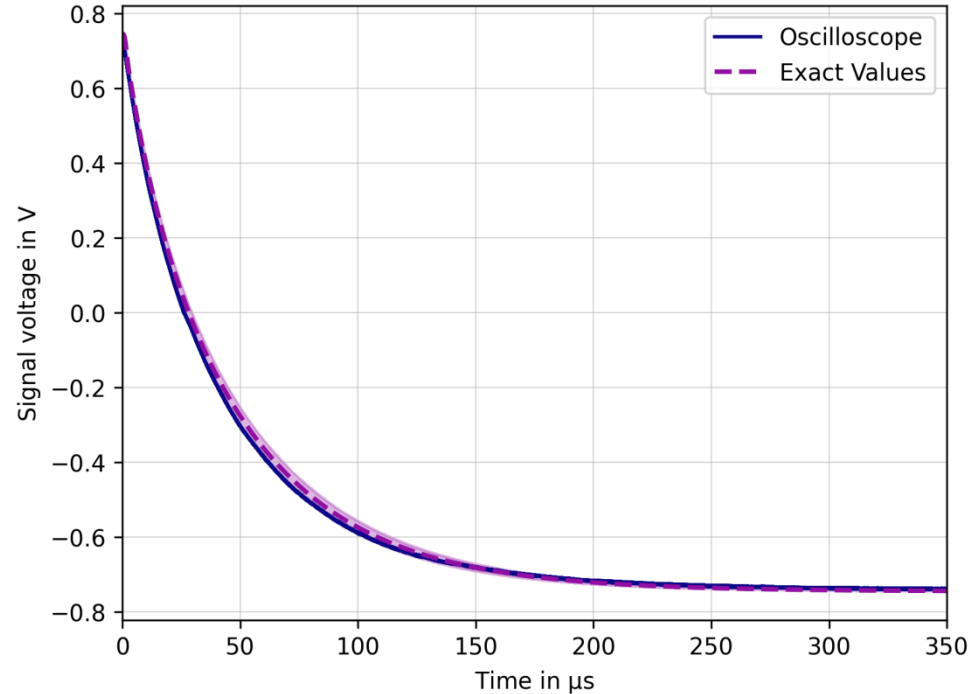


Time window	Ltline	Simple Line
0 – 40 μ s	3.11 mV	3.38 mV
0 – 1.5 μ s	4.3 mV	4.58 mV
1.5 μ s – 40 μ s	1.556 mV	1.729 mV

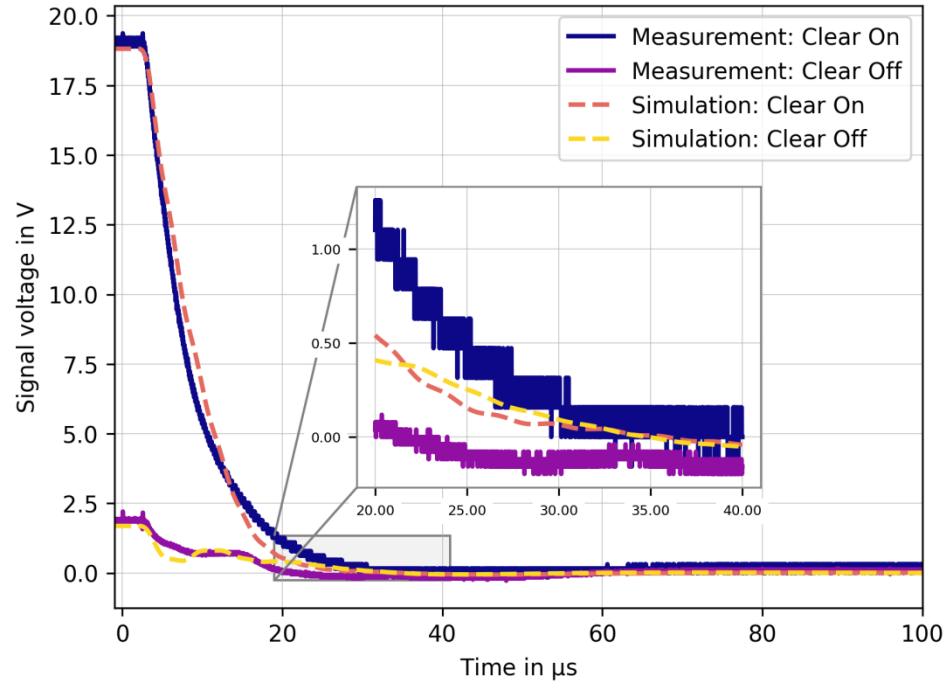


TOLERANCE OF CAPACITORS

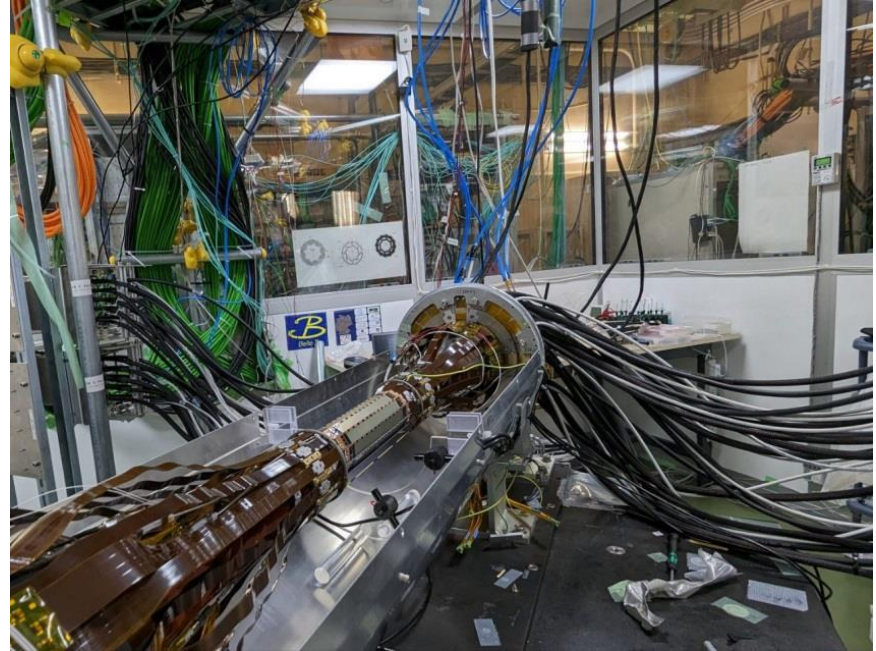
- +5 % and -5% on every capacitor in full simulation
- Oscilloscope measurement lies within tolerance band



ACTIVE SHUTDOWN: ZOOM IN

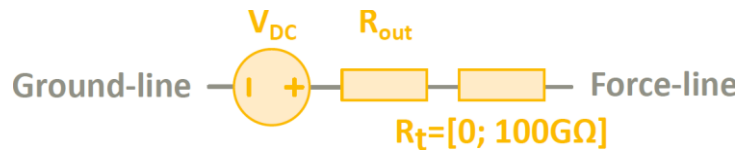


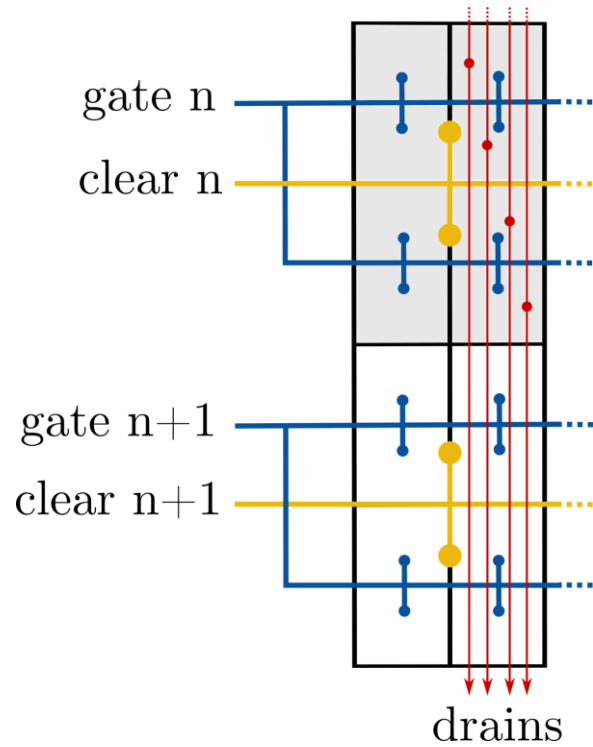
- Influence of cables on fast shutdown
unknown: in total **>15m**
- ➔ Simulate powering scheme of single
module
 - understand limitations
 - find hardware modifications
- Use cable characteristics in simulation



PASSIVE SHUTDOWN

- Passive shutdown → **separate** force line from power supply
- Simulate by **time dependent resistor** which switches from $0\ \Omega$ to $100\ \text{G}\Omega$





- Solving circuit equations (Maxwell equations)
- Netlist turned into matrix -> solve differential equations
- Tline model:
 - Transmission line theory
 - One dimensional wave equation $\frac{d^2V(x)}{dx^2} - \gamma^2(x) = 0$ and $\frac{d^2V(x)}{dx^2} - \gamma^2(x) = 0$
 - With $\gamma^2 = (i\omega L + R)(i\omega C + G)$
- Simple Line model:
 - Transmission Line theory
 - W-element algorithm
 - Initial sequence of elements which are compared and swapped for better results

- S-parameter model in HyperLynx:
 - ADMS simulator
 - Convert to complex pole model
 - Representation of impedance in frequency domain
 - Poles and Zeros of Impedance
 - Fast Fourier Transform