UNIVERSITÄT BONN

FTD

SI LAB
Silizium Labor Bonn

Development and Characterization of a Testing Stand for ITk Pixel Quad-Module Quality Control During Production

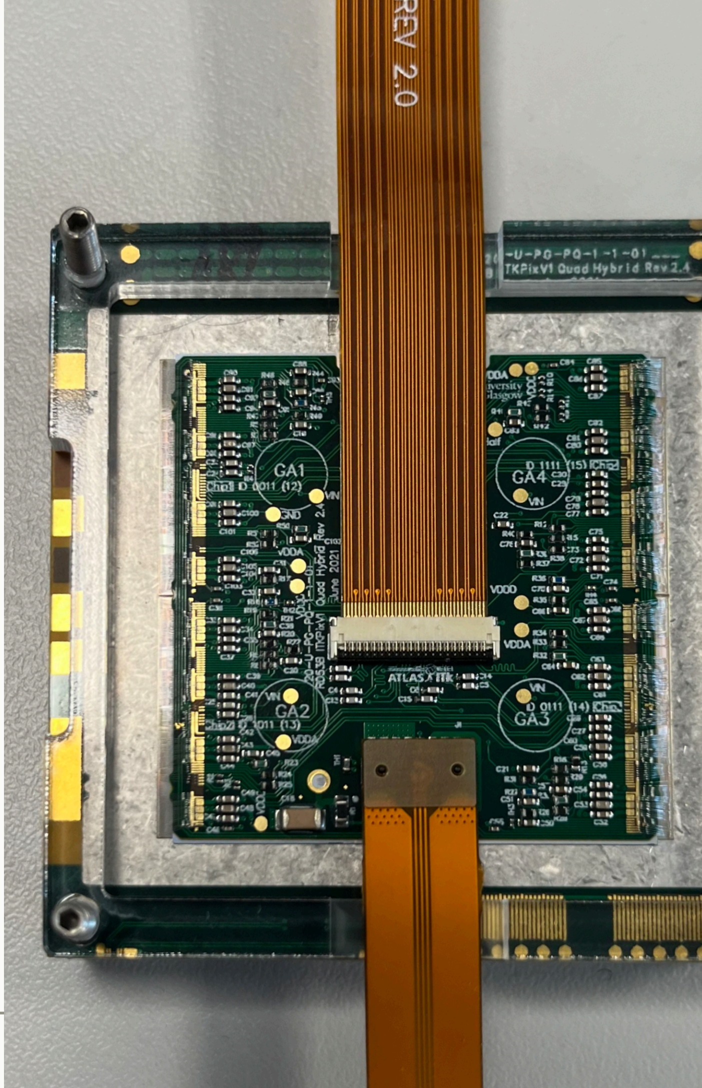
Master Thesis Colloquium

Matthias Schüssler - 16.10.2023

Supervisor: Prof. J. Dingfelder

OUTLINE

- Introduction: LHC and ATLAS
- The ATLAS ITk Pixel Detector
- A Setup for Quad-Module Testing
- Module Testing and Quality Control
- Summary

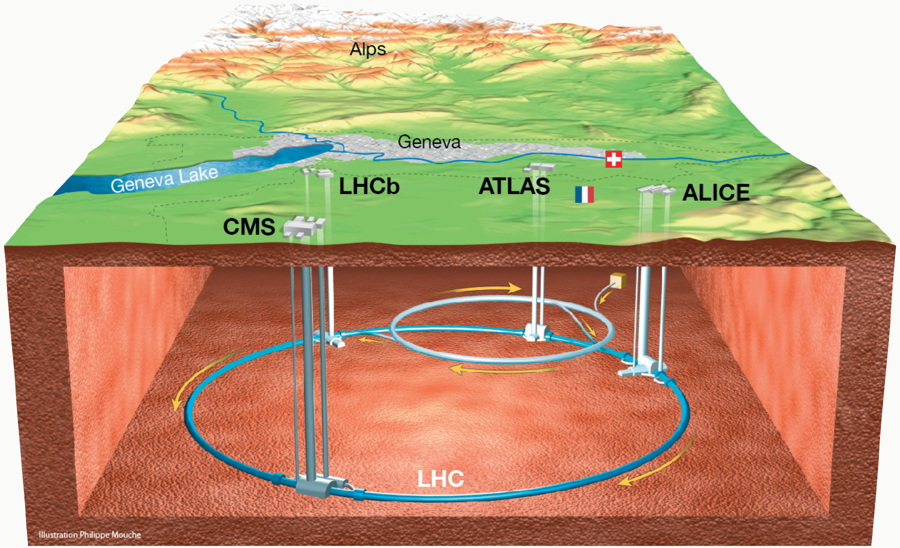


THE LARGE HADRON COLLIDER

Goal: Explore the Standard Model of particle physics and beyond

Symmetric circular collider located at CERN

- Accelerate protons and heavy ions
- Beam energy of up to 7 TeV for protons



P. Mouche / https://cds.cern.ch/record/1708847 / 2014

THE HIGH LUMINOSITY LHC

Goal: Study rare physics events with high precision

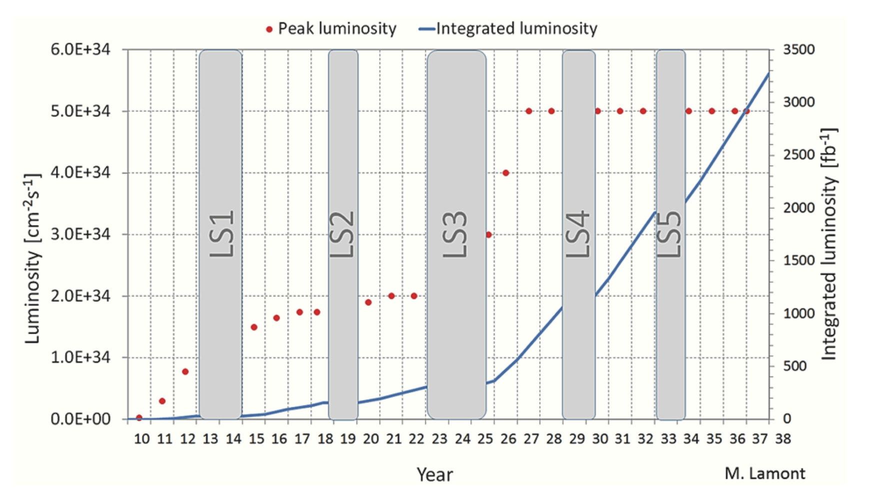
- Large number of events needed!

High Luminosity upgrade to LHC

- Increase luminosity by a factor of 5-7
- Design luminosity: 5×10^{34} cm^{-2} s^{-1}

Challenges for detectors at HL-LHC:

- Increased radiation levels -> radiation hard technology
- 10 times higher hit rate -> fast readout
- Up to 200 pile-up collisions -> high granularity



L. Rossi, O.Brüning / Introduction to the HL-LHC Project / 2015

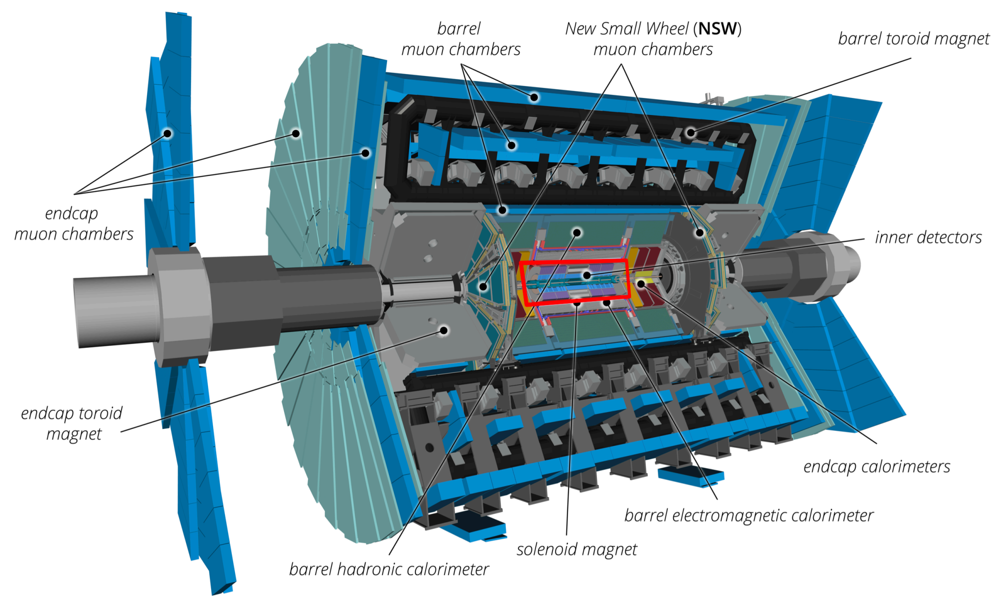
ATLAS EXPERIMENT

A Toroidal LHC Apparatus: ATLAS

- General purpose experiment at LHC

Detector subsystems:

- Barrel toroid magnet
- Muon chambers for muon identification
- Electromagnetic and hadronic calorimeters
- Solenoid magnet
- Inner Detector for tracking and vertexing



ATLAS / The ATLAS Experiment at the CERN Large Hadron Collider: A Description of the Detector Configuration for Run 3 / 2023

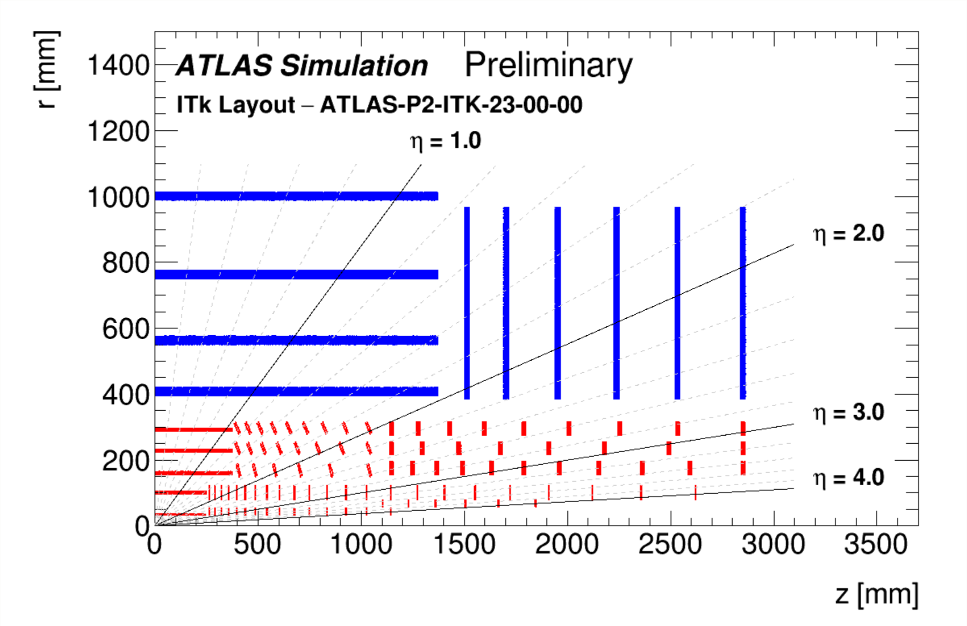
ATLAS INNER TRACKER

Upgrade for HL-LHC ➡ replace Inner Detector

- All-silicon ATLAS Inner Tracker (ITk)

- Outer strip detector
  - 4 barrel layers and 6 end-caps

- Inner pixel detector
  - 5 barrel layers and several end-caps
  - Consists of ~ 9000 pixel modules
    - ➡ 5x modules than in old ATLAS ID
      - ➡ Serial powering
      - ➡ **Streamlined production and testing!**



ATLAS / https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/ITK-2020-002/ / 2020

THE ATLAS ITk PIXEL DETECTOR

HYBRID PIXEL DETECTORS

Every detector has 2 functional blocks

- Signal generation and signal processing

Hybrid pixel detector ➡ components are separate

- Signal generation ➡ **Pixel sensor**
- Signal processing ➡ **Readout chip**

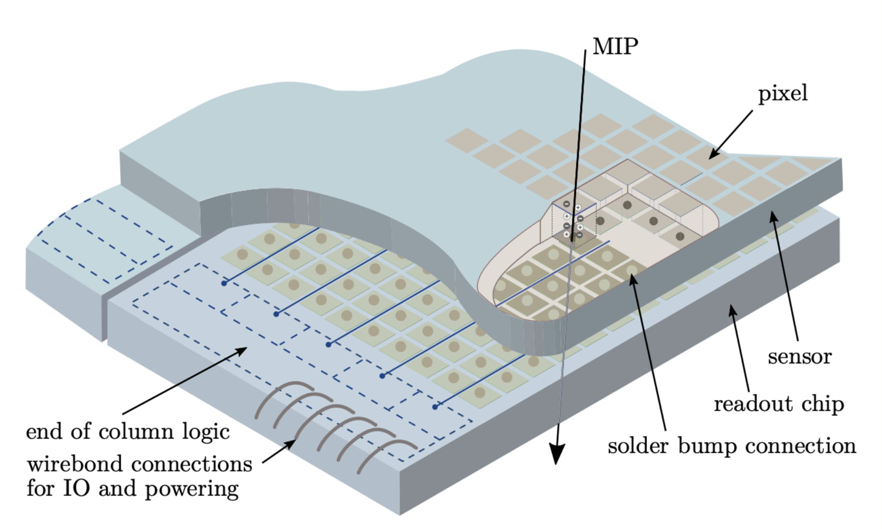
} Connected via bump-bonding

Advantage:

- Optimise production of each component

Disadvantages:

- Expensive and difficult interconnection process
  ➡ Needs testing!
- More inactive material

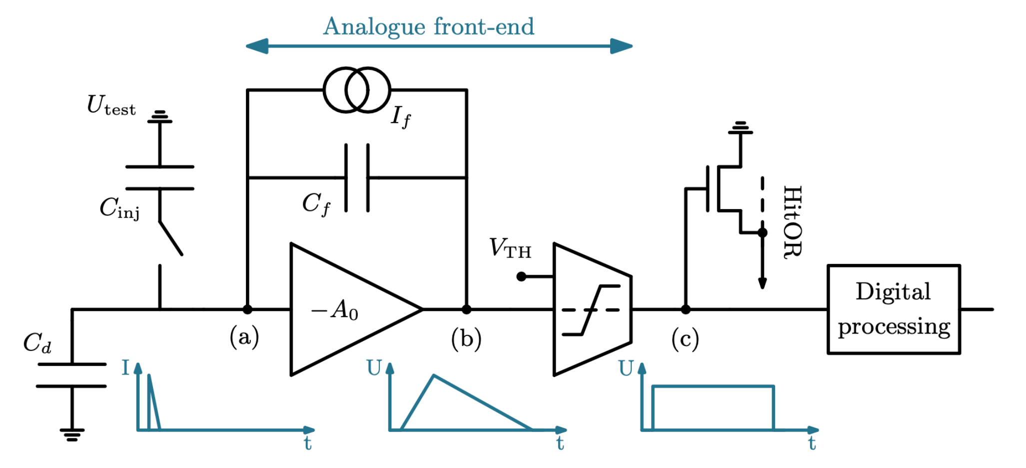


David-Leon Pohl / 3D-Silicon and Passive CMOS Sensors for Pixel Detectors in High Radiation Environments / 2020

ANALOG READOUT CHAIN

Goal: Fast signal digitisation

- Preamplifier
  - Integrate collected charge
  - Amplify signal
    - ➡ Voltage proportional to collected charge
- Discriminator
  - Compare signal to a voltage threshold
    - ➡ Output a signal high when threshold is crossed



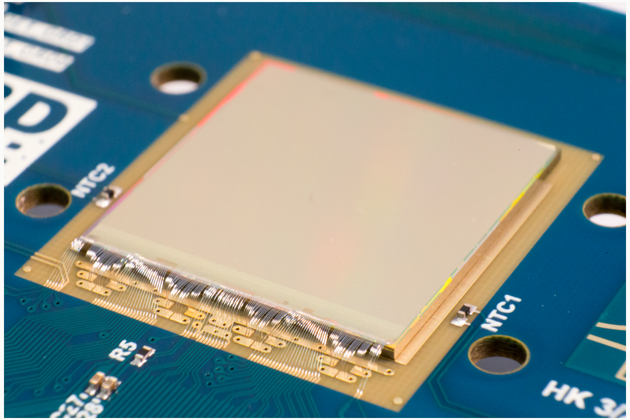
Y. Dieter / Development and Characterisation of Passive CMOS Sensors for Pixel Detectors in High Radiation Environments / 2022

THE ITkPix READOUT CHIP

- 65 nm CMOS technology
- 400 x 384 pixels grouped in 8 x 8 pixel cores
  - Pixel size: 50 µm x 50 µm

Important features:

- 2 SLDO regulators for serial powering
- Analog and digital injection circuit ➡ chip calibration and testing
- Configurable analog multiplexer (MUX) for readout of internal voltages
- NTC and diode based temperature sensors



RD53 Collaboration / RD53B users guide / 2021

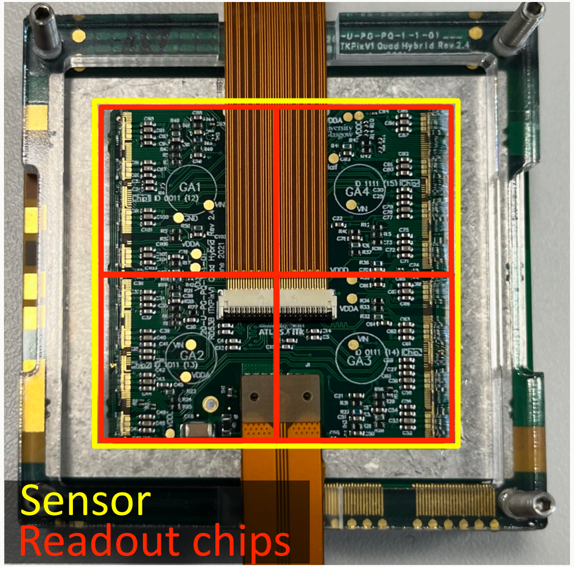
ITkPix QUAD-MODULE

Module: Unit consisting of a sensor tile and multiple readout chips

- Sensor
  - Pixelated 4 cm x 4 cm silicon sensor tile
  - Sensor thickness of 150 µm
- Readout chip
  - 4 readout chips per sensor ➡ quad-module
- Module flex
  - Common connection of all 4 readout chips to periphery
  - Connected to the chips by wire-bonds
  - Houses a module NTC for temperature measurements

1000 ITkPix quad-modules will be assembled and tested in Bonn

➡ Production rate: **10-12 modules/week**



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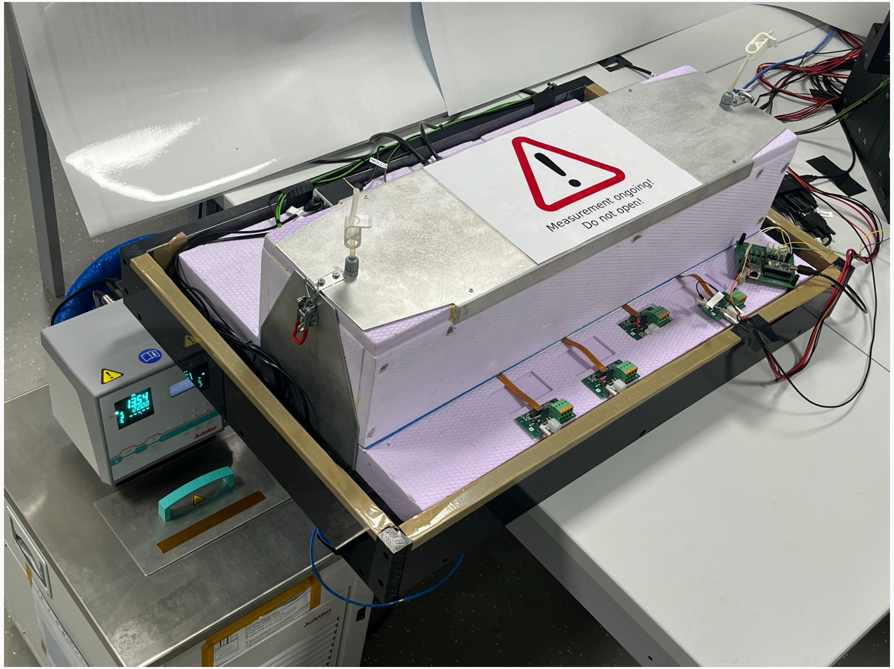
A SETUP FOR QUAD-MODULE TESTING

ASSEMBLED MODULE TESTING IN BONN

Goal: Testing of 12 modules per week during production

- Electrical test of the readout chip
- Testing at 20°C and - 15°C using the same setup

- **Automated testing**
  - Parallel testing of 4 modules
  - Automated control of environmental conditions



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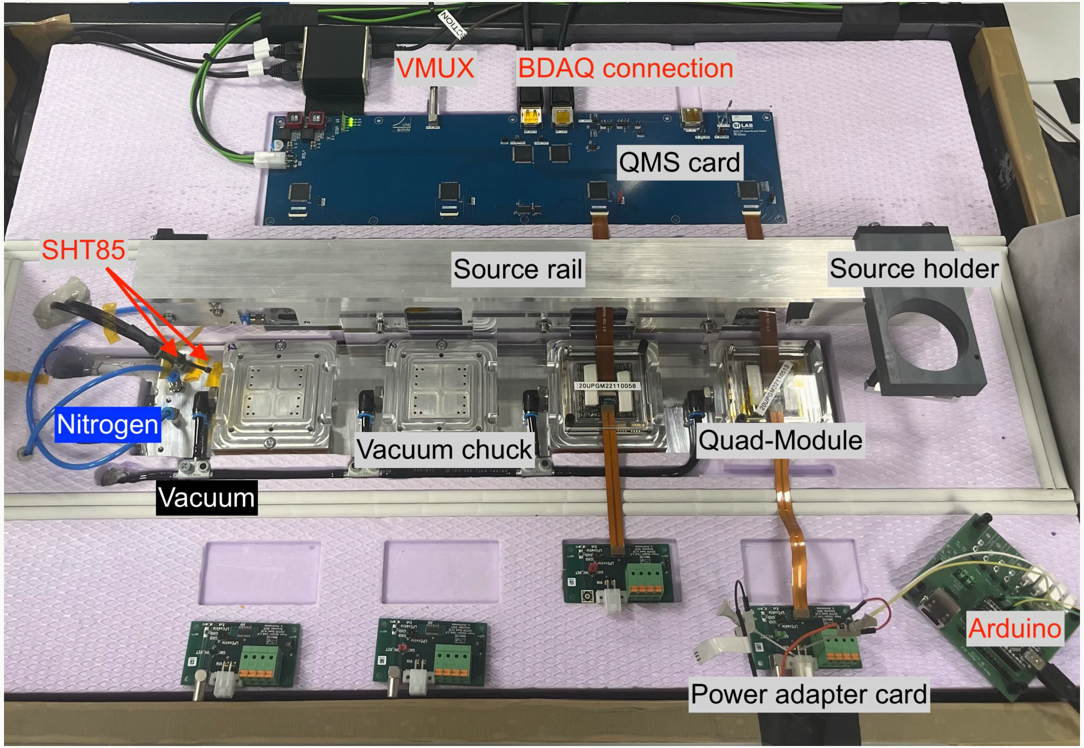
TESTING SETUP

Goal: Parallel testing of 4 modules

- Modules placed on aluminium cooling block
  - Held in place using vacuum
  - Cooled using a water-ethanol mixture
- Nitrogen used to control humidity
  - Temperature and humidity are tracked with two SHT85 sensors
- Rail for measurements with sources
- QMS card for readout of all 4 modules



COMMISSIONING OF THE COLD BOX

Goal: Verify that measurements at 20°C and - 15°C are possible with 4 modules installed

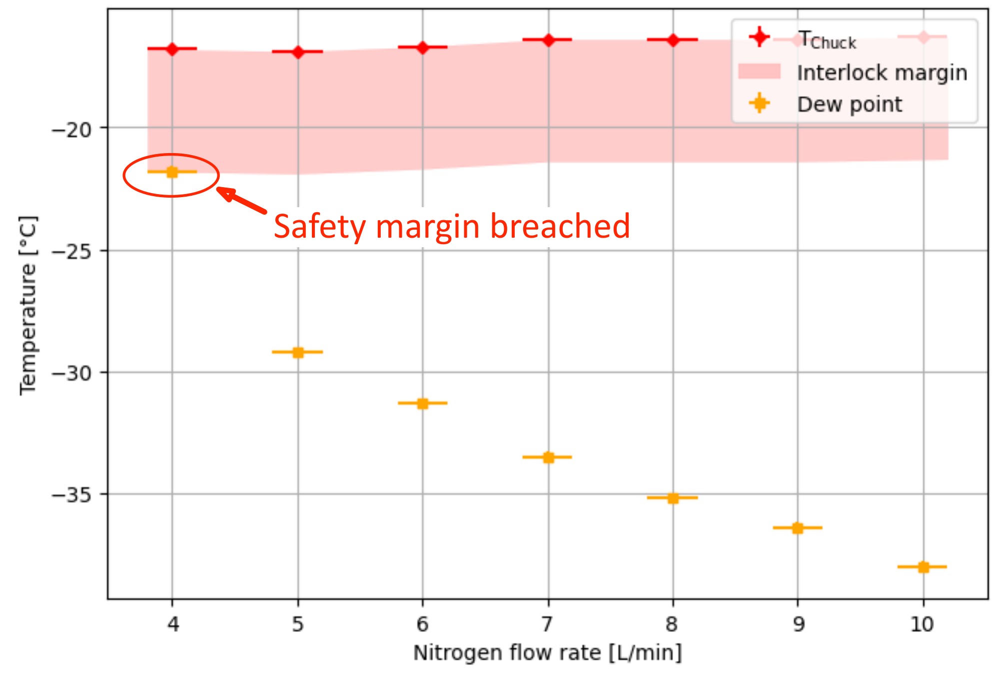
Dew point: Temperature at which humidity in the air condensates

➡ damage to modules possible

➡ **maintain 5°C safety margin**

Measure temperature and humidity to establish minimum nitrogen flow

➡ At -15°C: > 4 L/min required



DETECTOR CONTROL SYSTEM (DCS)

Goal: Monitor environmental conditions during measurements

➡ Detector Control System (DCS) developed

Monitored Parameters:

- **Environmental:**
  - Ambient temperature (SHT 85)
  - Cooling block temperature (SHT 85)
  - Ambient humidity (SHT 85)
  - Humidity at cooling block (SHT 85)
  - Ambient dew point (calculated)
  - Dew point at chuck (calculated)
  - Vacuum pressure (Arduino)

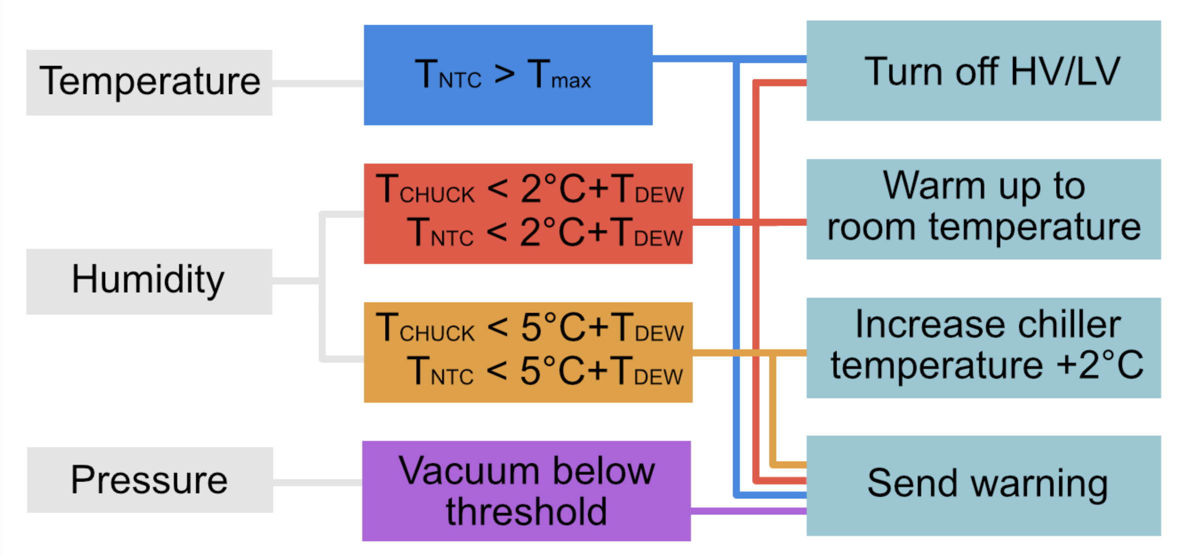
- **Module under test:**
  - Module temperature (NTC)
  - Input voltage (Powersupply)
  - Input current (Powersupply)
  - Input bias voltage (HV Powersupply)
  - Leakage current (HV Powersupply)

DETECTOR CONTROL SYSTEM (DCS)

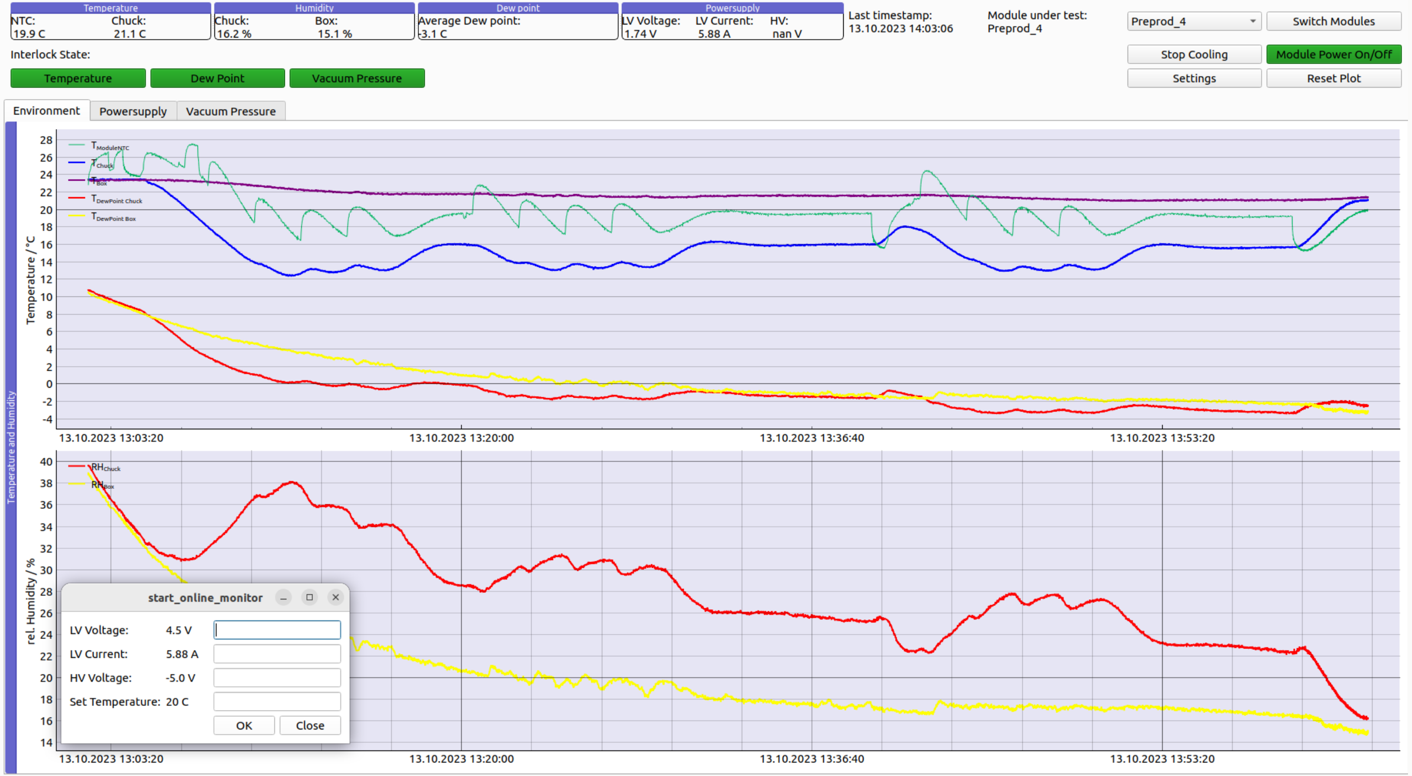
Goal: Safeguard against hazardous environmental conditions

➡ Continuously monitor data from DCS

➡ Take action if critical situation arises



DETECTOR CONTROL SYSTEM (DCS)



MODULE TESTING AND QUALITY CONTROL

ELECTRICAL QC ROUTINE

Goal: Test electrical functionality of components

- **Non DAQ tests:**
  - Efuse
  - ADC calibration
  - VDDA/VDDD trim
  - Temperature sensor readout
  - Analog read back
  - SLDO test
  - Measure Injection Capacitance
  - VCal Calibration

- **Pixel failure analysis**
  - Minimum Health Test
  - Tuning to 1500e threshold
  - Pixel Failure Test

Routine is implemented ➡ results for 2 modules cross-verified by tests performed in Siegen

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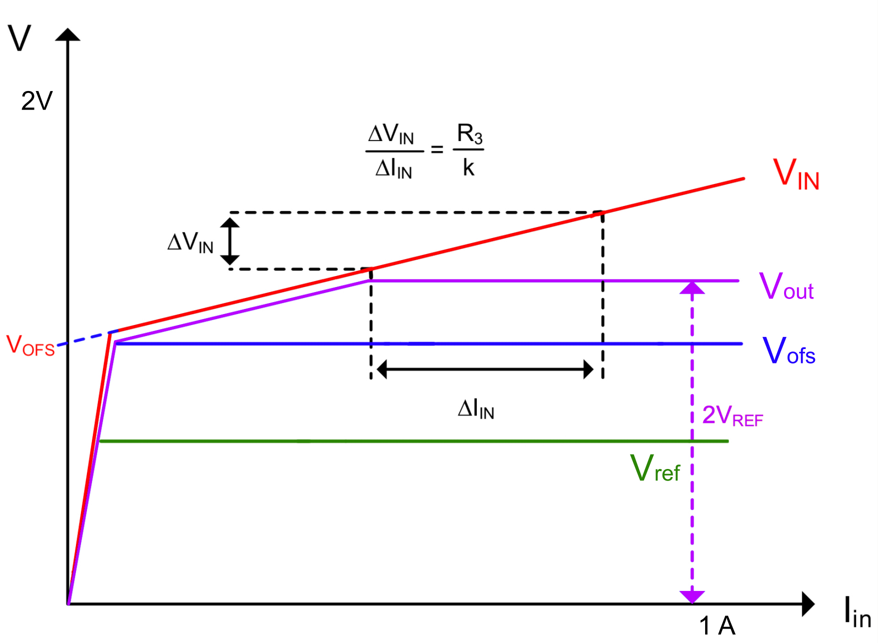
NON DAQ TESTS - SLDO

SLDO

- Convert supply current to constant voltage
  - Shunt excess current
- Linear behaviour of input voltage
  - ➡ Allows for parallel operation of all chips on each module



M. Karagounis / Shunt-LDO Regulator - Internal Review / 2019

QC criteria: Input voltage is linear and follows prediction

NON DAQ TESTS - SLDO

SLDO

- Set input current to 9.48 A
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  - Readout voltages
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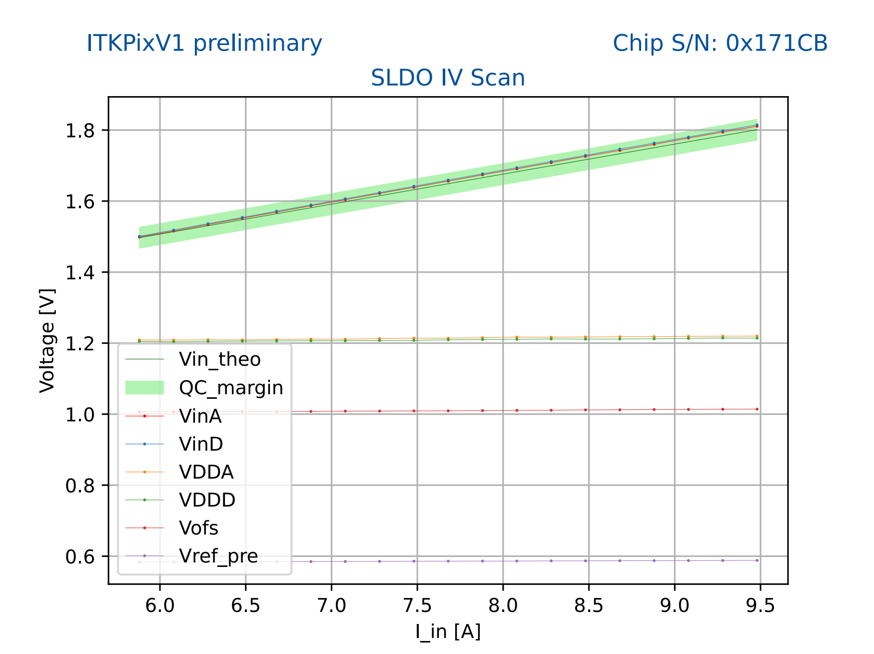

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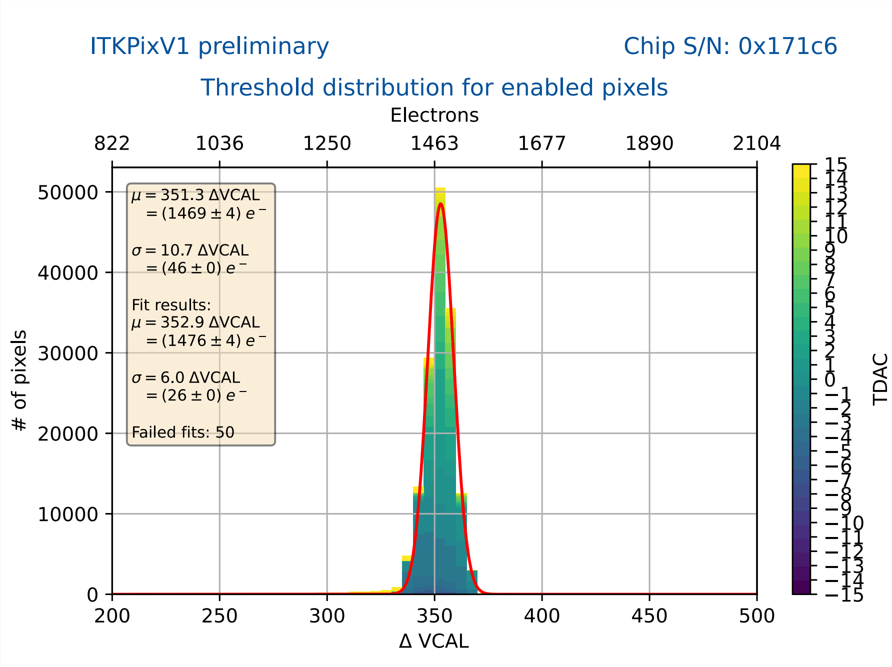
PIXEL FAILURE ANALYSIS

Goal: Test functionality of the readout chain

- Minimum Health Test:
  - Quickly identify defective chips
  - Digital injection scan, analog injection scan, threshold scan
- Tuning:
  - Set the discriminator to a 1500e charge threshold
- Pixel Failure Test
  - Identify and deactivate defective pixels
  - Digital injection scan, analog injection scan, threshold scan, noise occupancy scan

QC criteria: Rate of pixel failures < 0.1 %



TUNING PERFORMANCE

Goal: Establish optimal tuning threshold for ITkPix modules with a 150 µm planar sensor

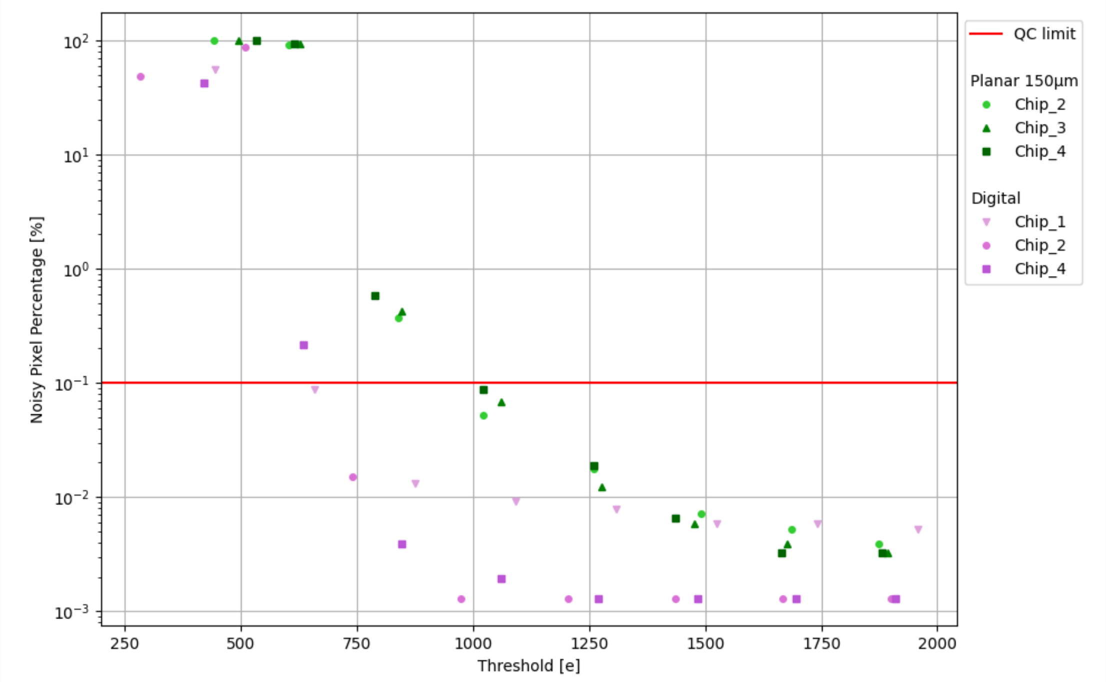
Procedure:

- Tune chip to a threshold
- Perform Pixel Failure Test

Minimum tuning threshold:

➡ 700 e for digital module

➡ 1 000 e with 150 µm planar sensor



SOURCE MEASUREMENTS

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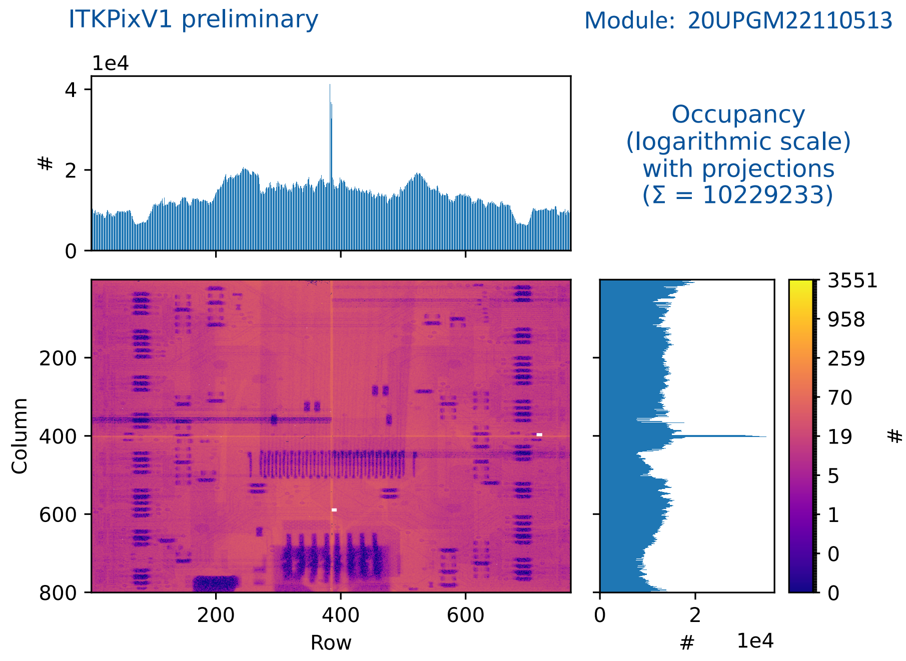
Goal: Identify defective bonds between sensor pixels and readout chip

- A radioactive source (Cd109) is used to generate signals
  ➡ **Need enough hits in each pixel to assure clear identification**

- Optimisation:
  - Distance of source from module
  - Scan time



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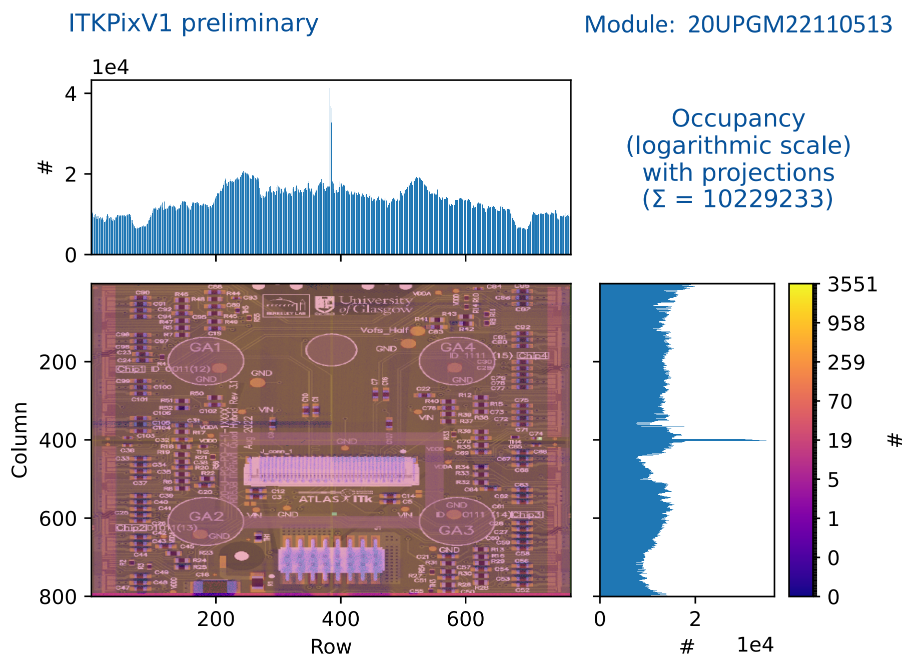
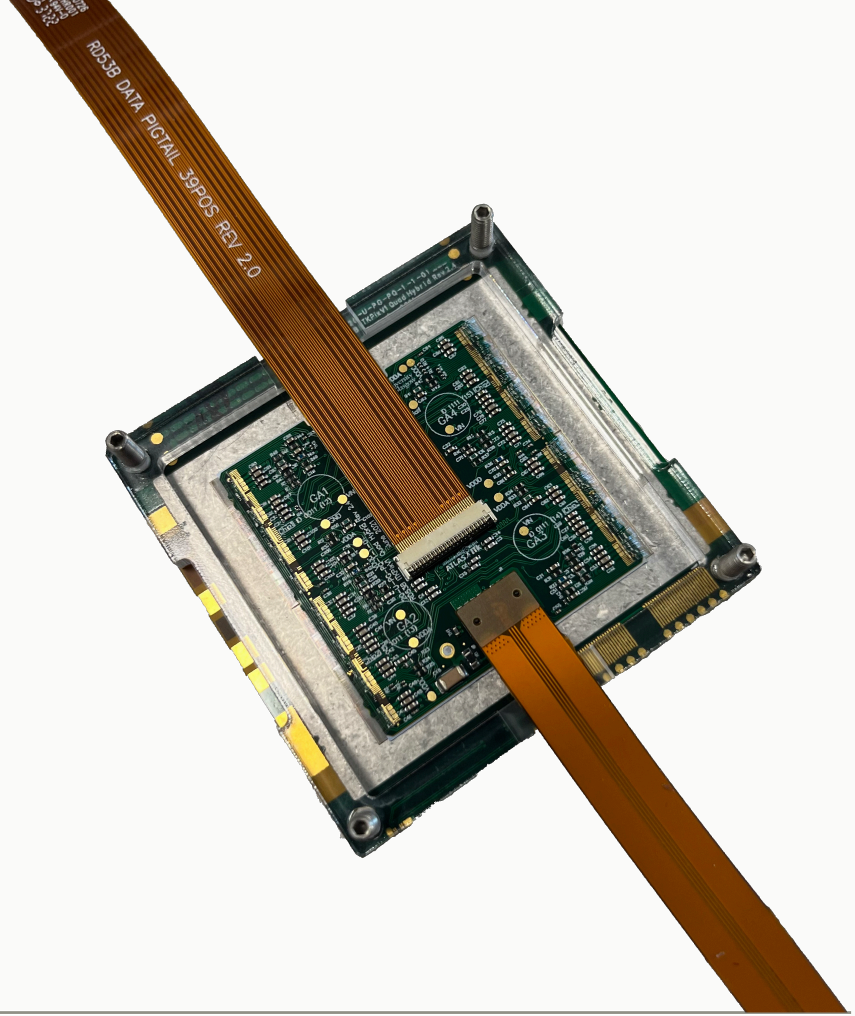


SUMMARY

- **Setup of module testing site:**
  - Test setup is commissioned
  - ready for full testing with 4 modules
  - DCS is operational and meets ATLAS testing requirements
  - DCS reacts to prevent hazardous conditions

- **Electrical module QC**
  - Necessary tests are implemented in readout software
  - Complete routine was performed on several modules
  - Source measurements are possible



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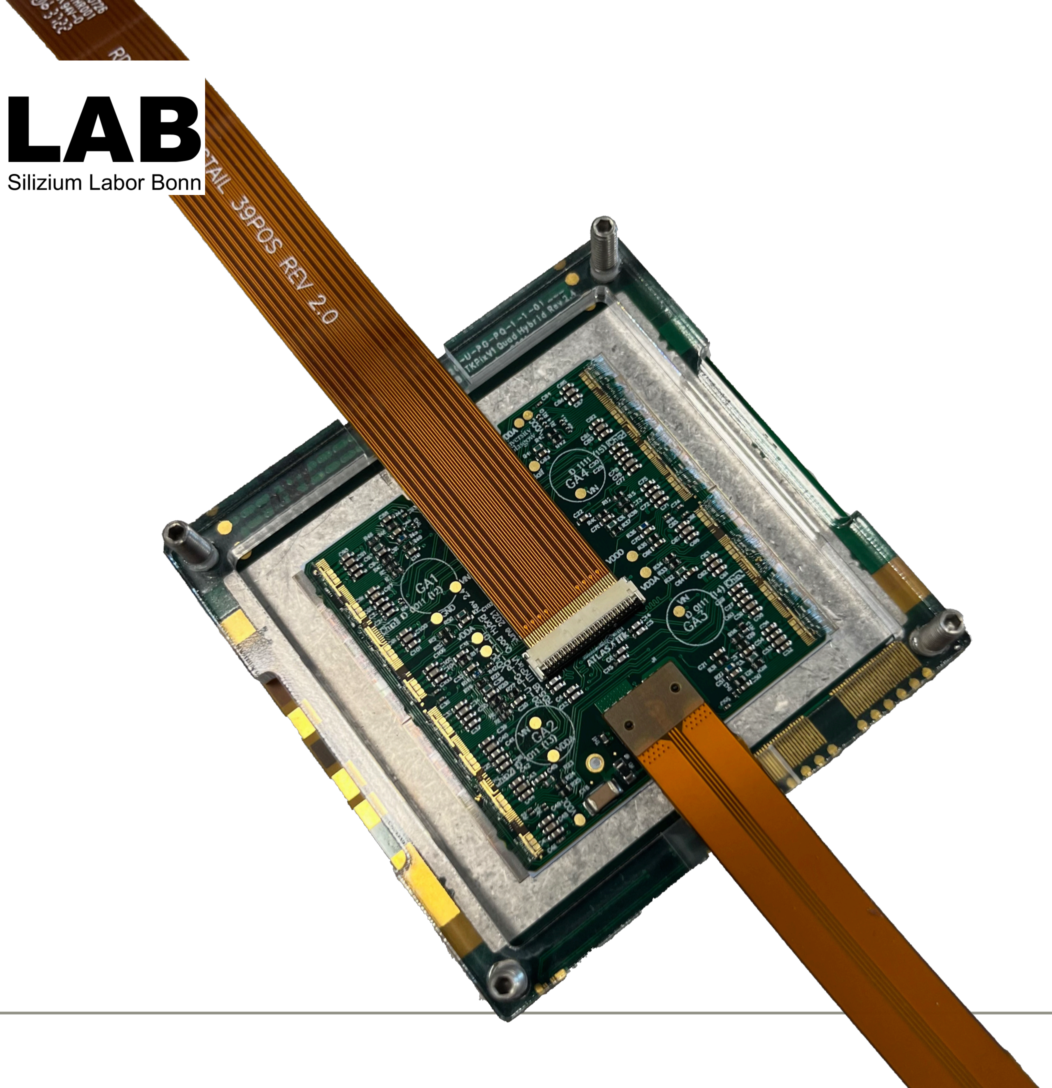
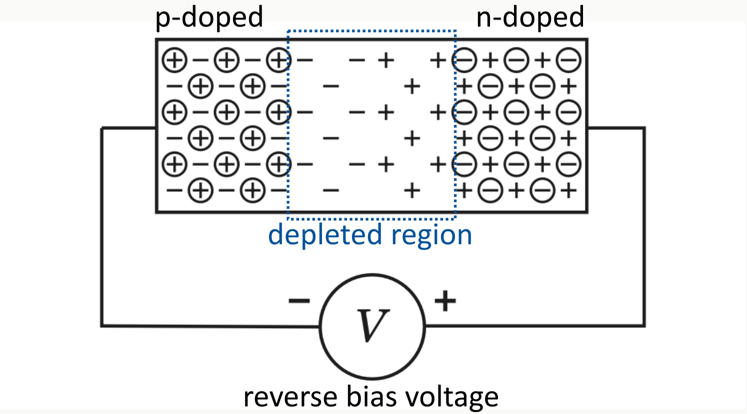
BACKUP

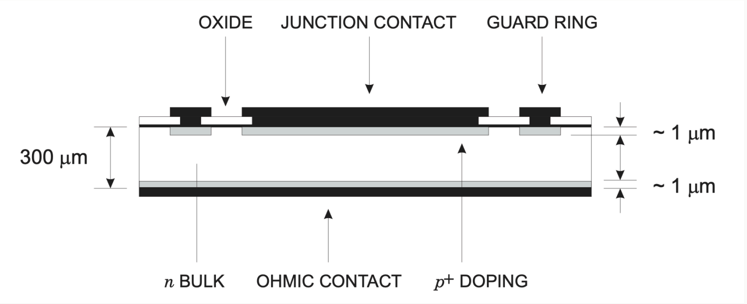


P-IN-N SILICON SENSOR

- pn-junction of a semiconductor as detection region
  - Operate in reverse bias -> depleted region forms
- Heavy particles loose energy by ionisation
  - ➡ electron-hole pairs are formed
  - ➡ charge measured at electrode

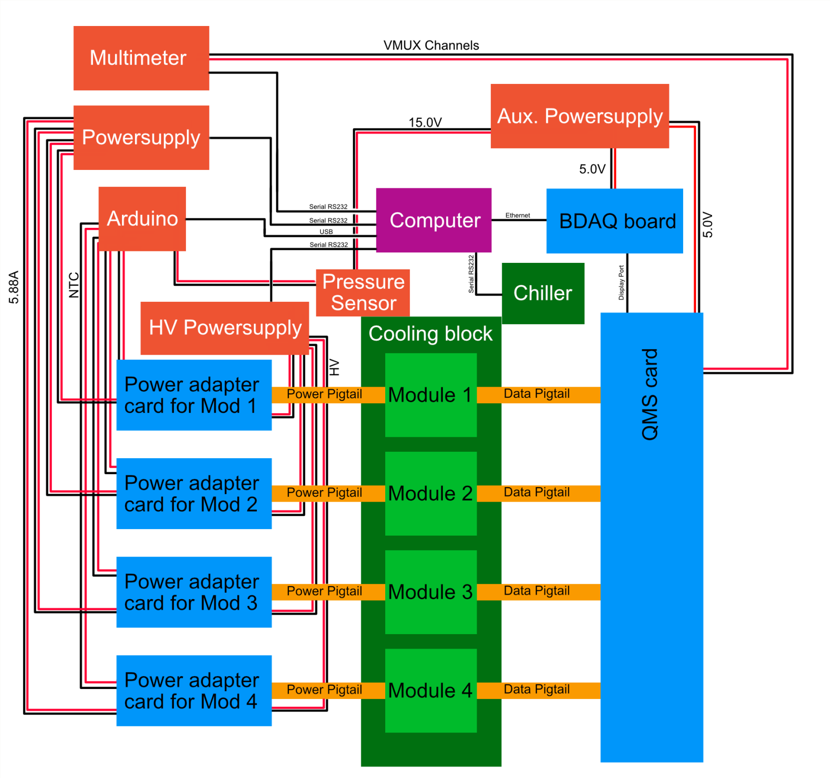
- p-in-n sensor: n-doped bulk with p-doped electrode
  - Advantage: Simple production
    - ➡ single sided process

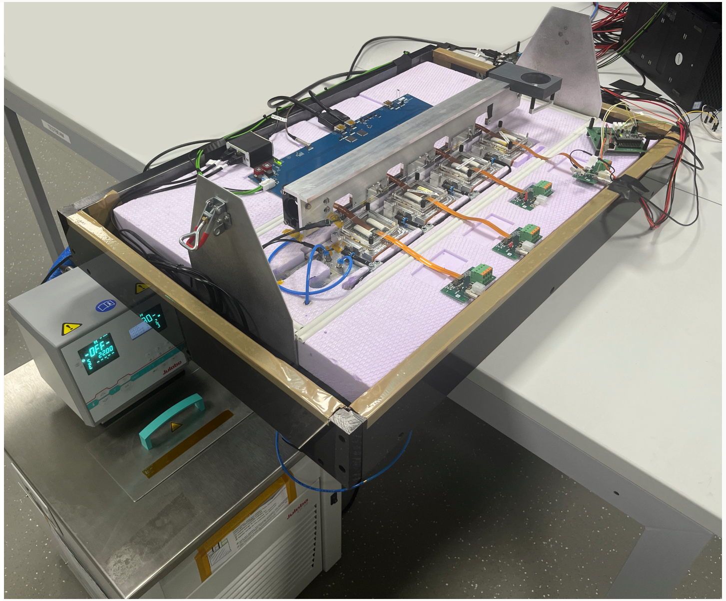




H. Spieler / Semiconductor Detector Systems / 2005

TESTING SETUP



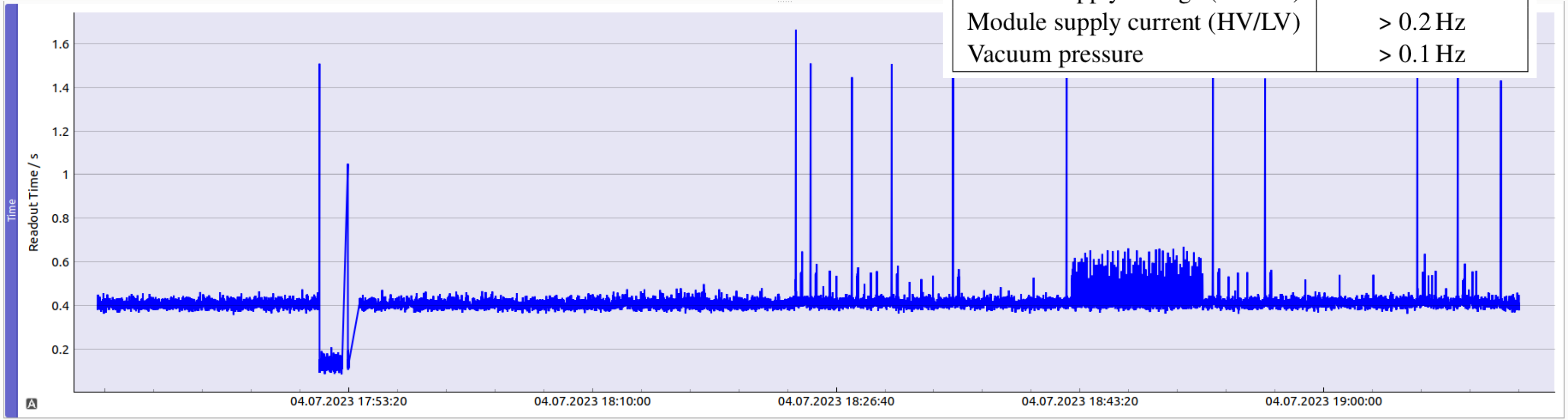


DCS READOUT RATE

- All parameters are updated synchronously in a measurement cycle
- Time for each cycle is tracked
- Readout rate: ~ 2.5 Hz

Required readout rates

Parameter	Update frequency
Module temperature	> 1 Hz
Chuck temperature	> 1 Hz
Relative humidity	> 1 Hz
Dewpoint	> 1 Hz
Module supply voltage (HV/LV)	> 0.2 Hz
Module supply current (HV/LV)	> 0.2 Hz
Vacuum pressure	> 0.1 Hz

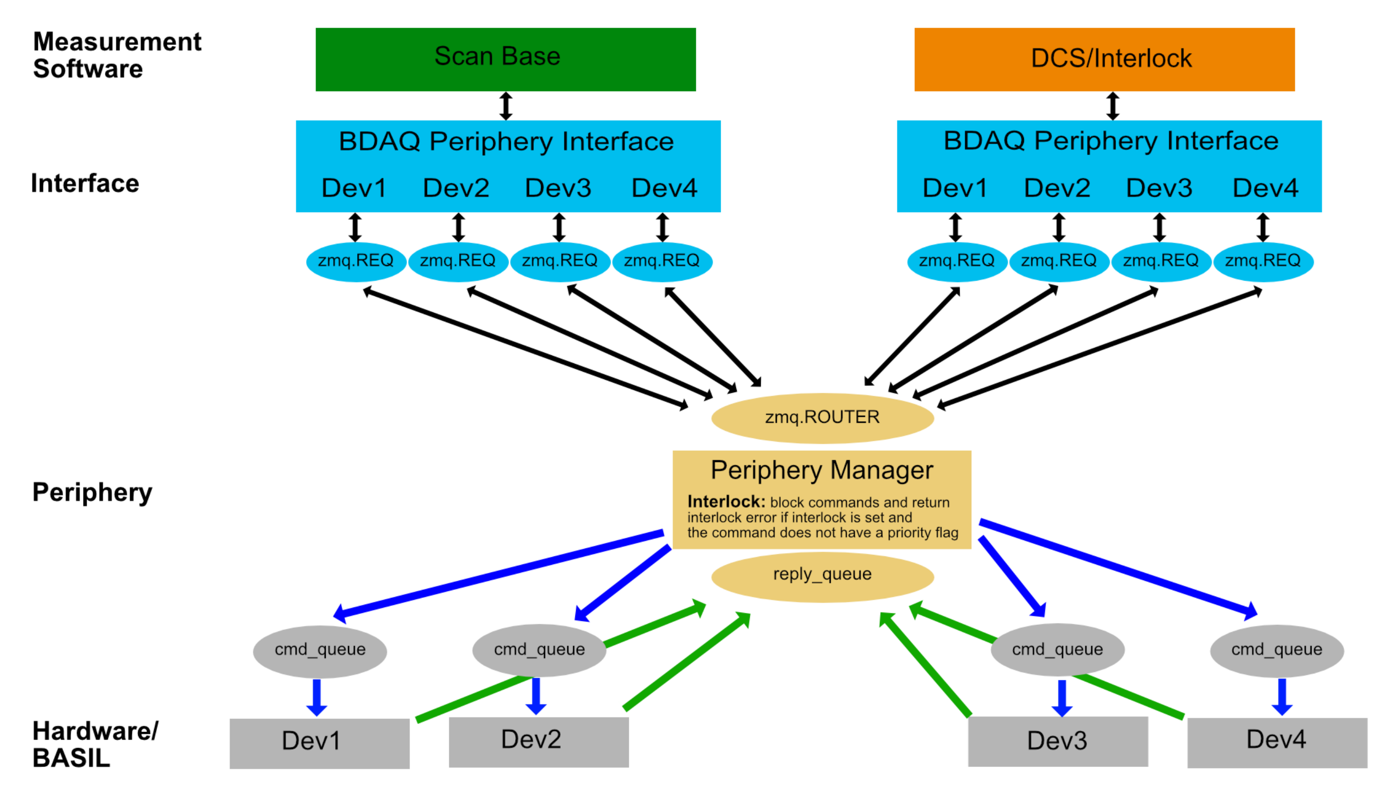


PERIPHERY ACCESS

Goal: Unify hardware access to avoid conflicts

- Provide virtualised hardware access to measurement processes
- Prioritise critical commands, e.g. interlock actions
- Keep device access parallel for different devices -> readout rate

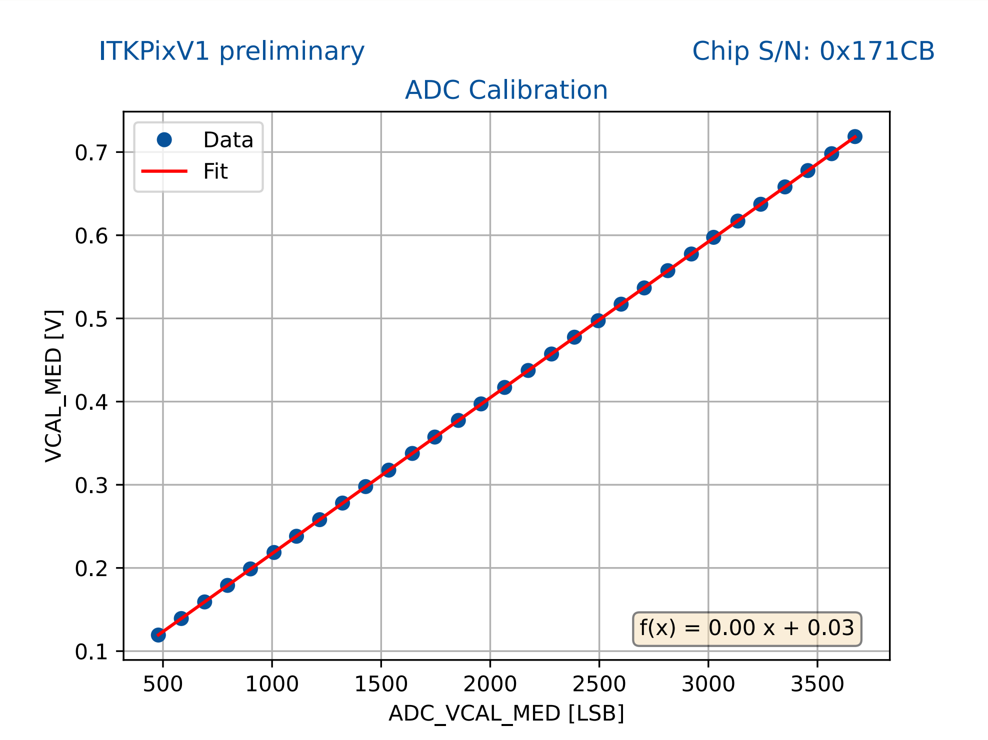
PERIPHERY ACCESS



NON DAQ TESTS - ADC CALIBRATION

Procedure

- Use the DAC for V_{CAL_MED} to generate a voltage
- Measure using the internal ADC
- Measure with an external multimeter
- Repeat for voltage steps over the entire operational range

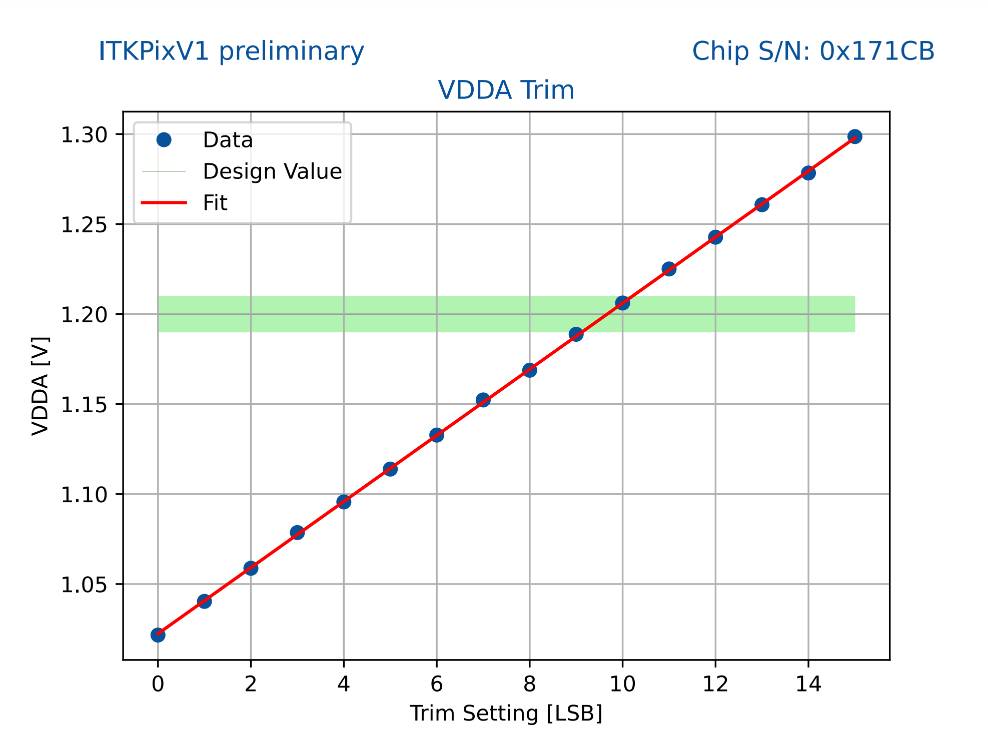


NON DAQ TESTS - VDDA/D

Trim VDDA/VDDD to 1.2 V

- Set all possible trim register settings
  - 4 bit registers -> 16 values
- Measure voltage with external multimeter

QC criteria: Voltage after trim is (1.20±0.02) V



NON DAQ TESTS - SLDO

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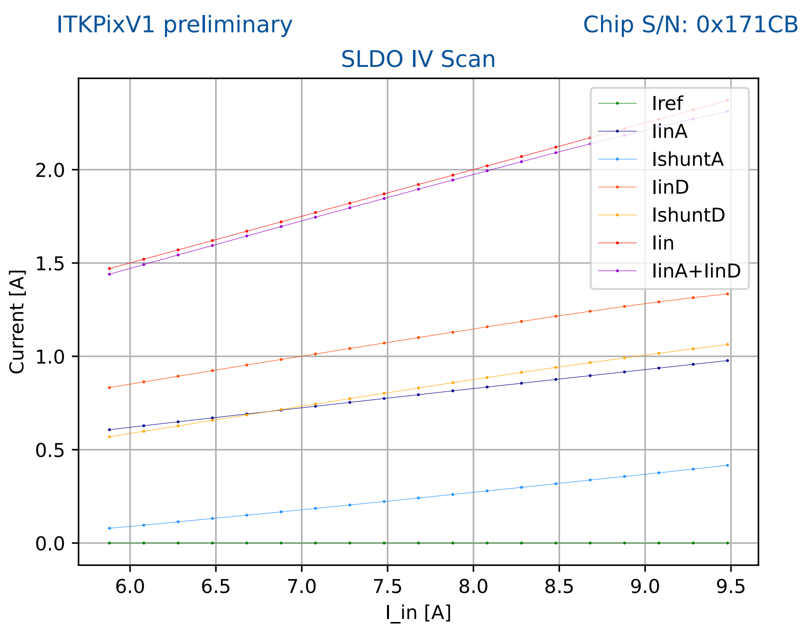
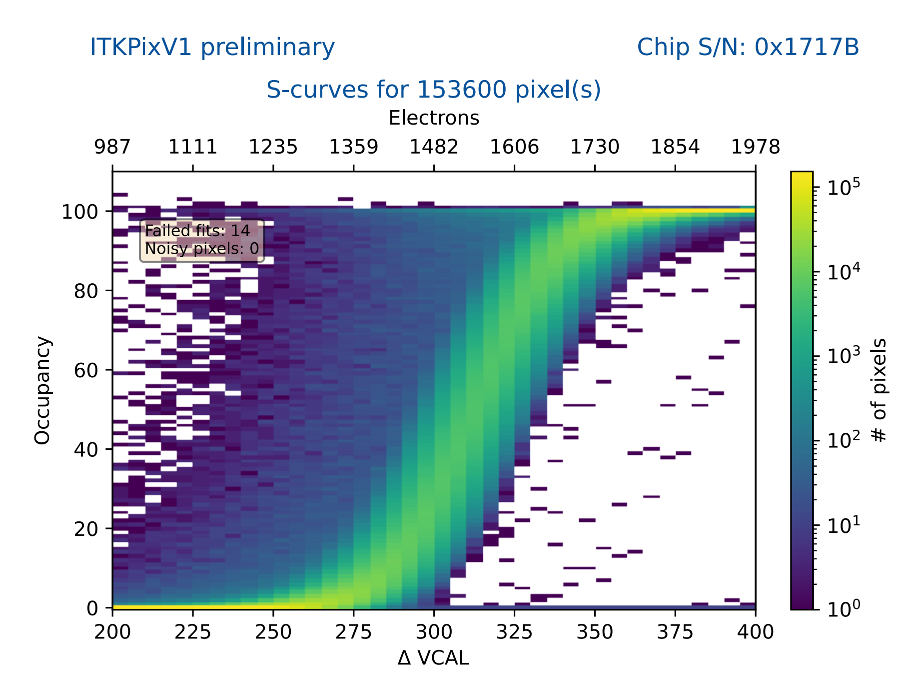
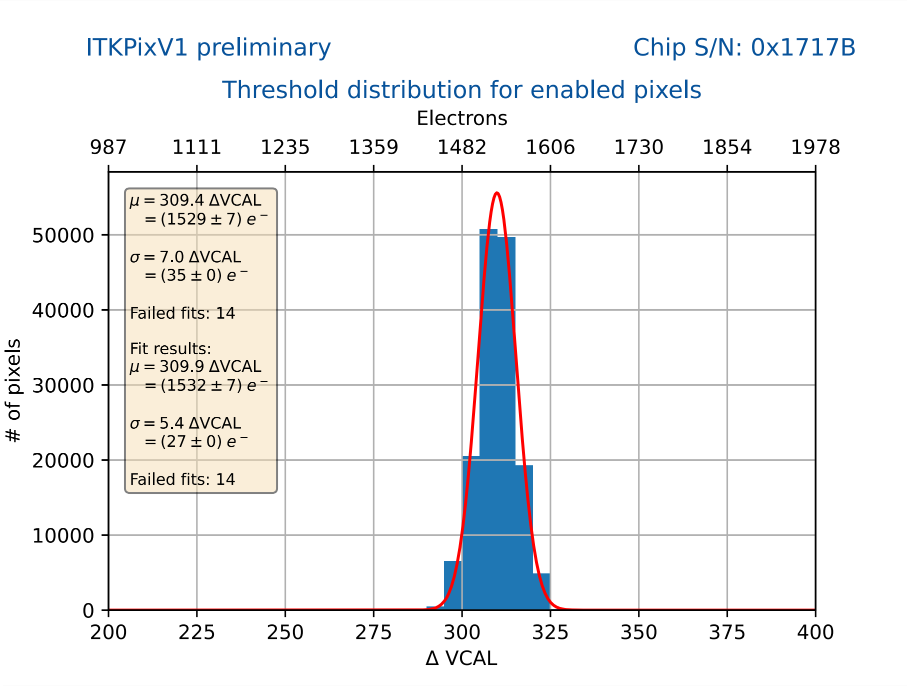


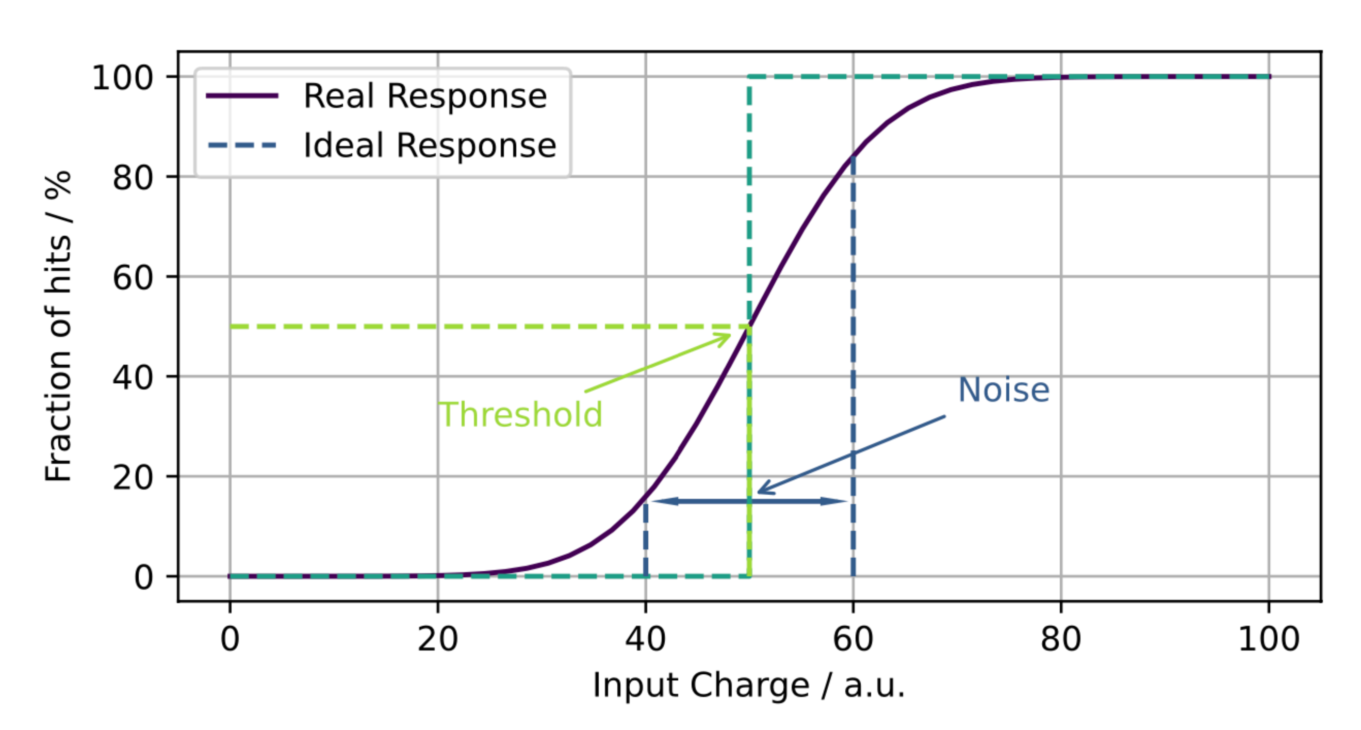
QC criteria: Input voltage is linear and follows prediction

THRESHOLD SCAN





THRESHOLD INVESTIGATION - NOISE



F. Hinterkeuser / Evaluation of a Serial Powering Scheme and its Building Blocks for the ATLAS ITk Pixel Detector / 2022

THRESHOLD INVESTIGATION - NOISE