

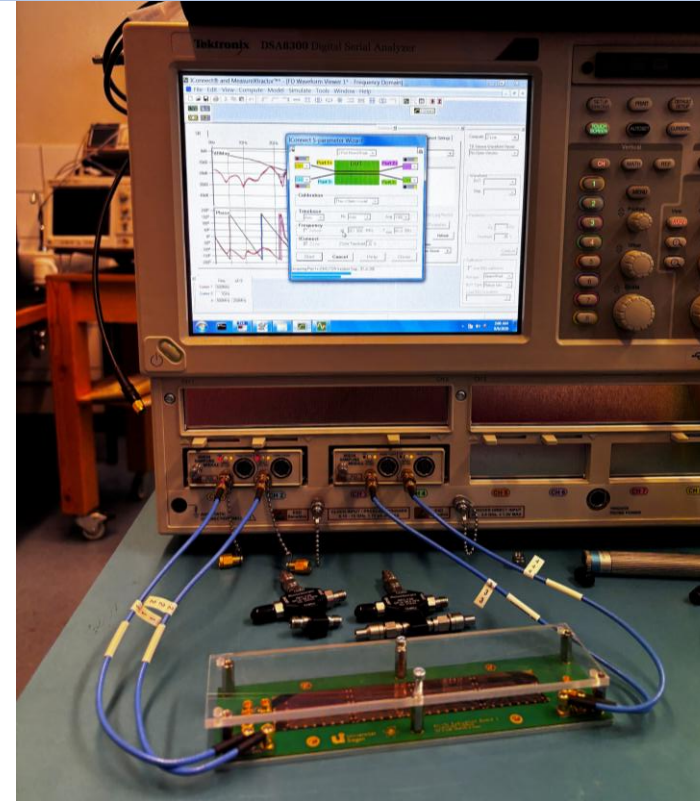
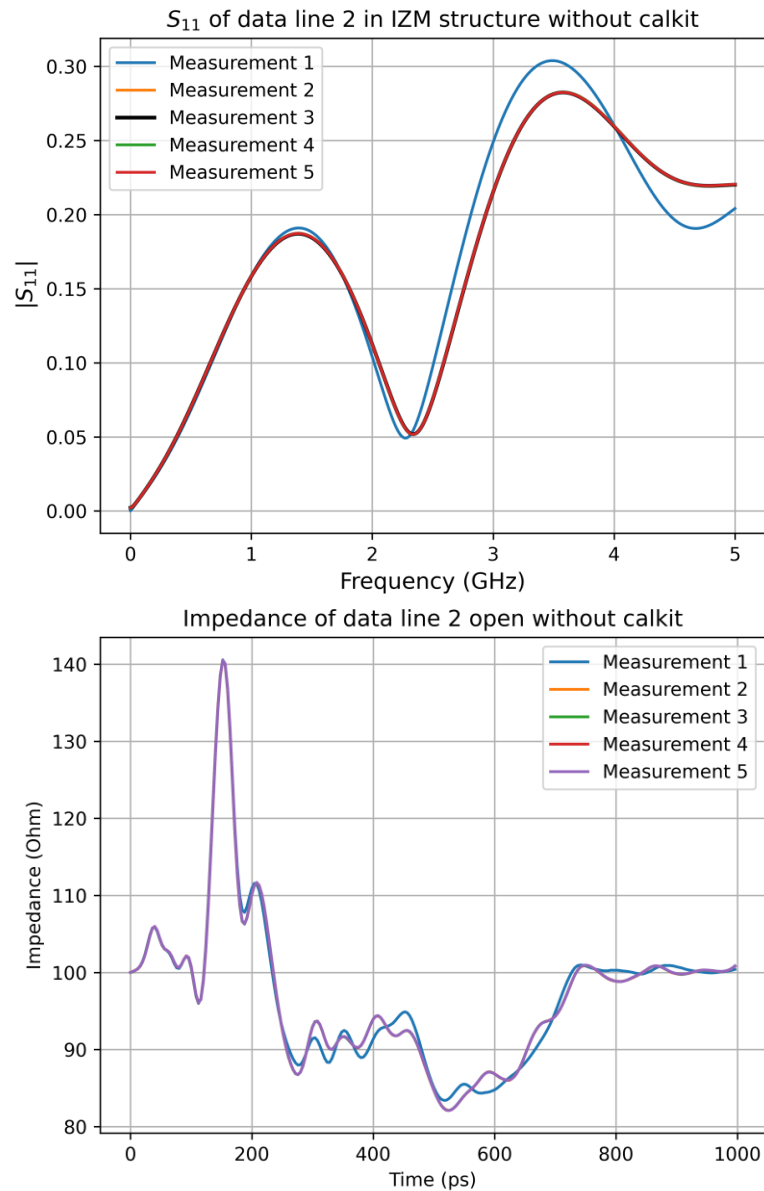
All-silicon meeting

Markus Cristinziani, Qader Dorosti, Stefan Heidbrink, Denise Müller, Noah Siegemund, Waldemar Stroh, **Darshil Vagadiya**, Wolfgang Walkowiak, Jens Winter, and Michael Ziolkowski

04.09.2026

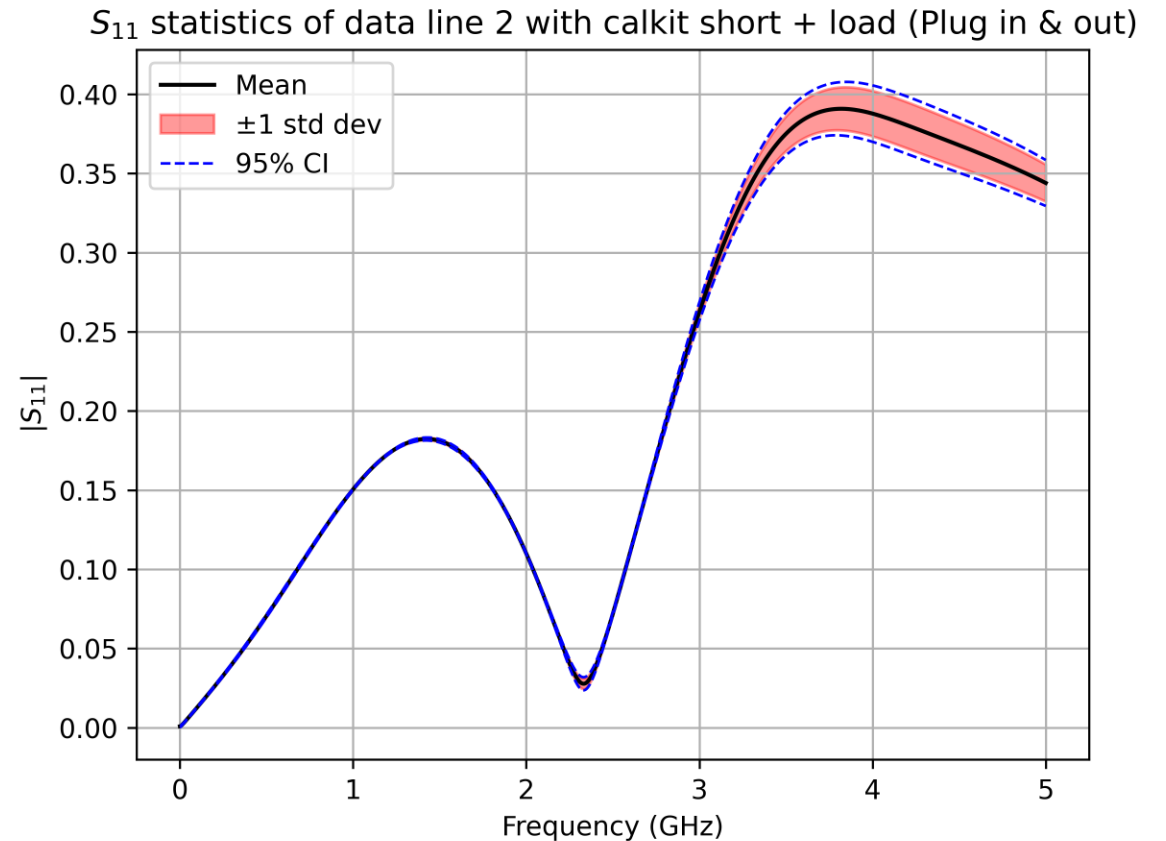
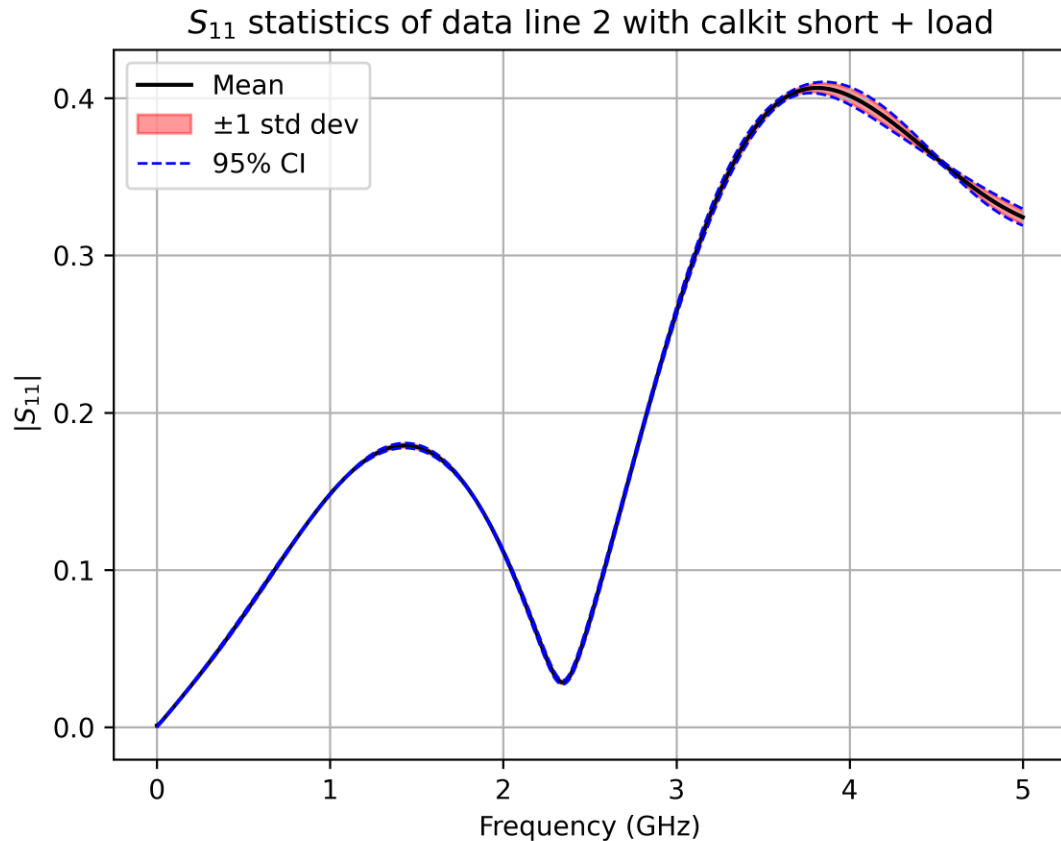
In collaboration with

TDR measurements



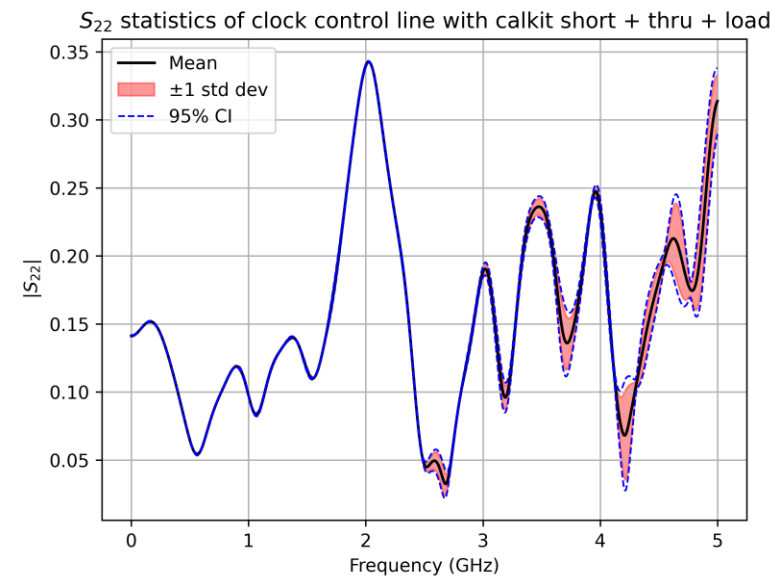
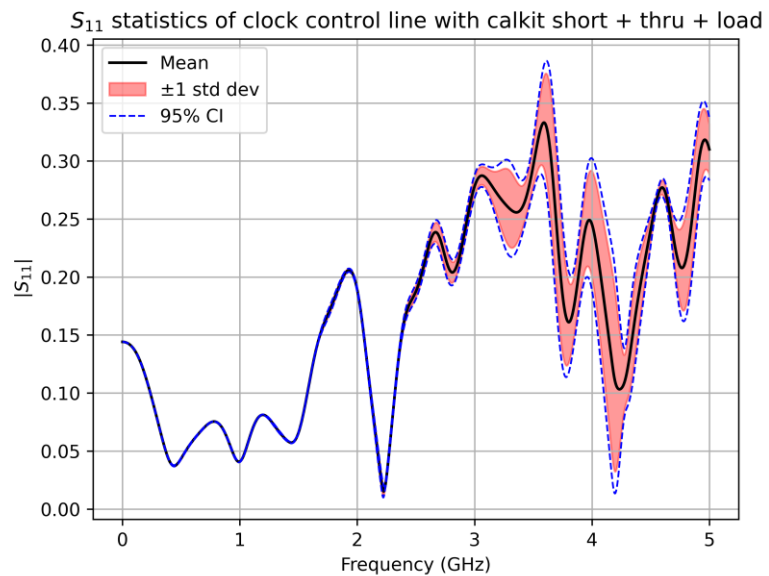
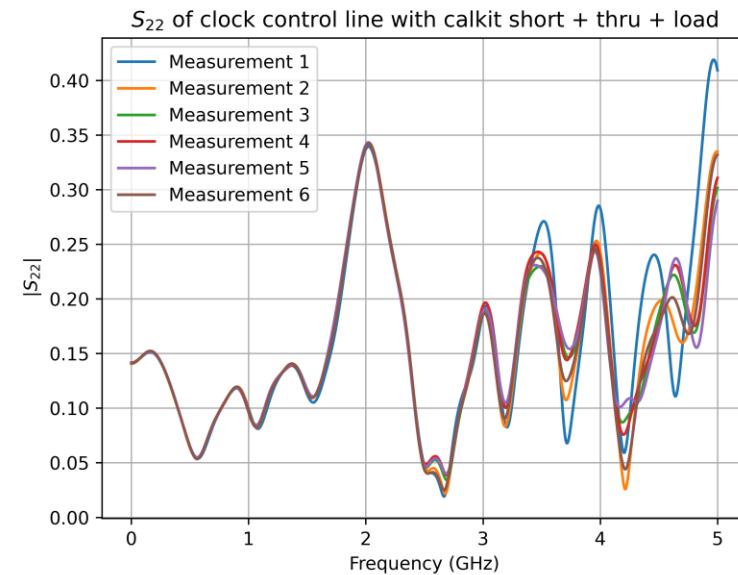
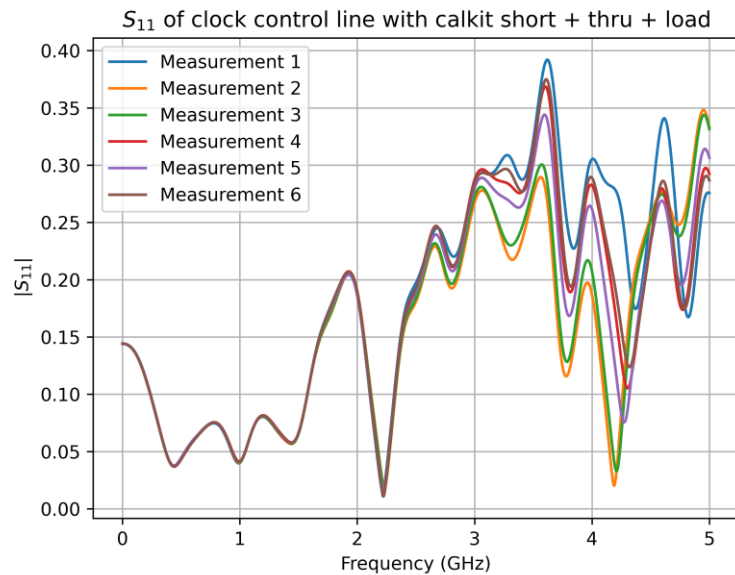
- After measurement 1, cables from the readout PCB were unplugged and plugged in again, and then other measurements were taken
- If we repeat measurements without unplugging and plugging in cables, the results remain the same
- Does this suggest that systematic uncertainty comes from cable orientation??

TDR measurements

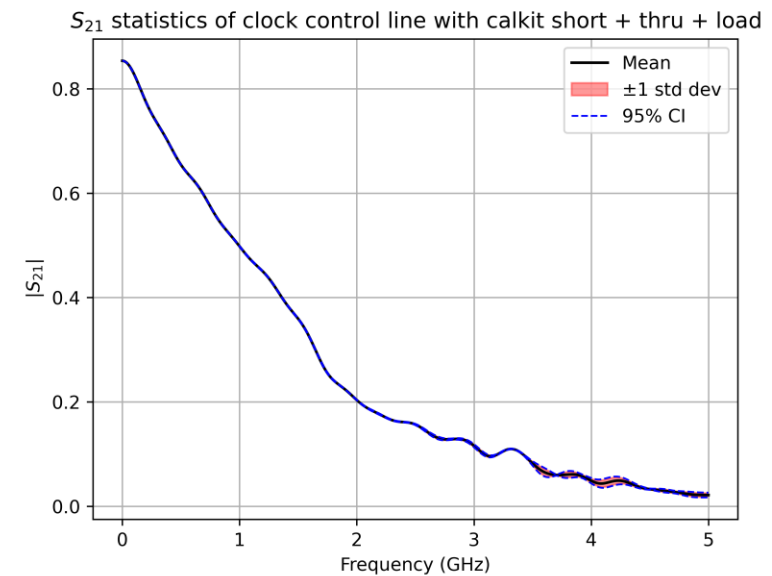
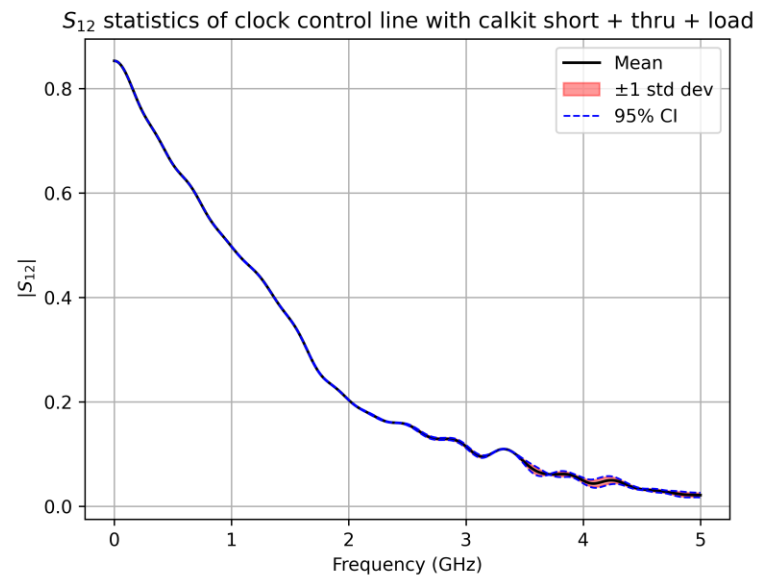
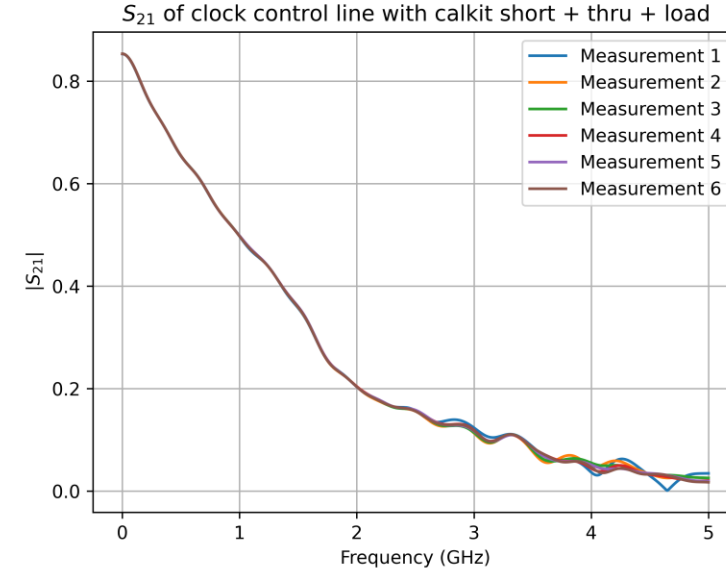
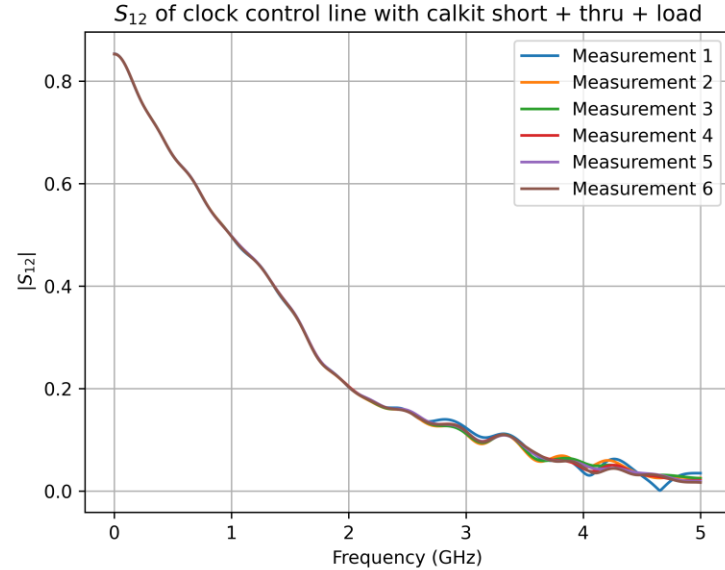


- After each measurement, cables from the readout PCB were unplugged and plugged in again, and then the next measurements were taken for the right side of the plot
- For the left side of the plot, cables were connected all the time, but cables were moving during the measurement
- This suggests that systematic uncertainty comes from cable orientation!!

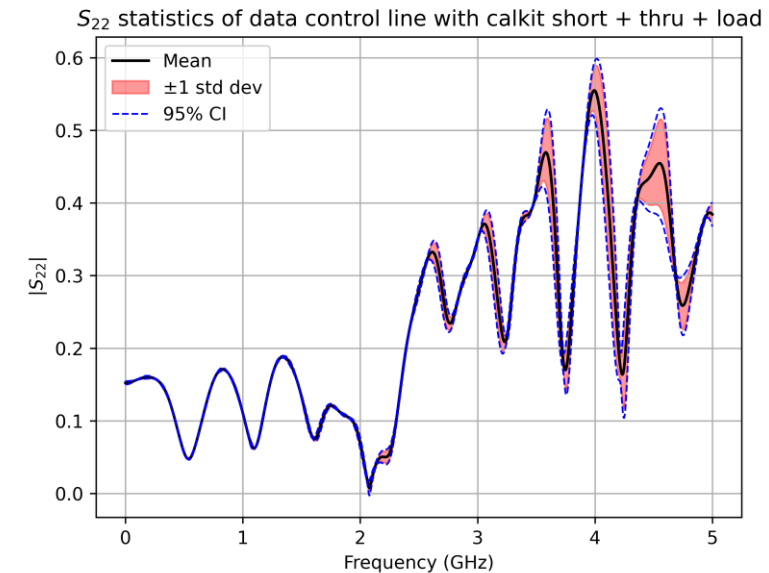
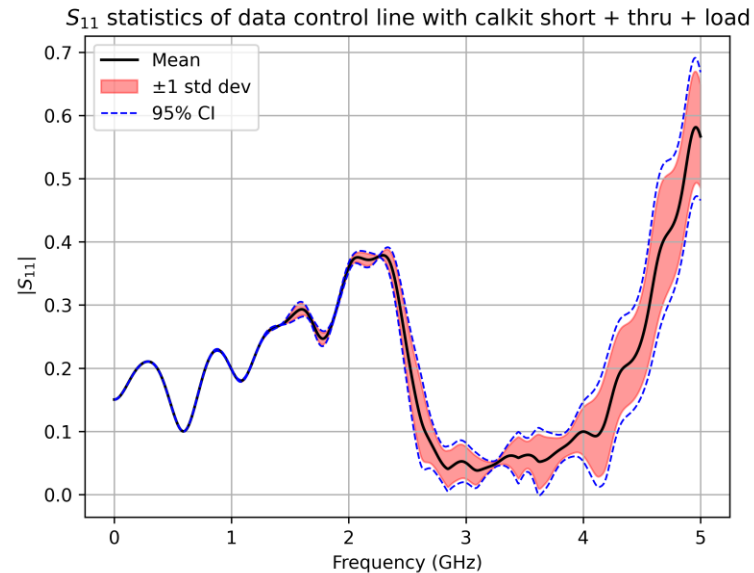
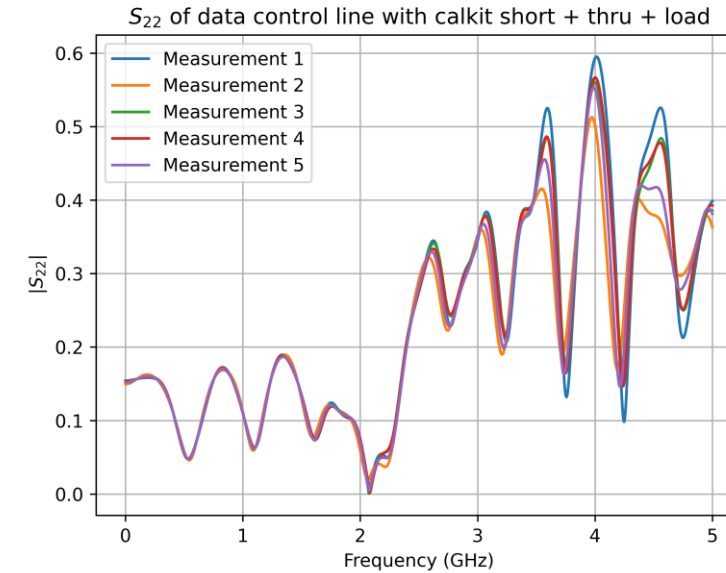
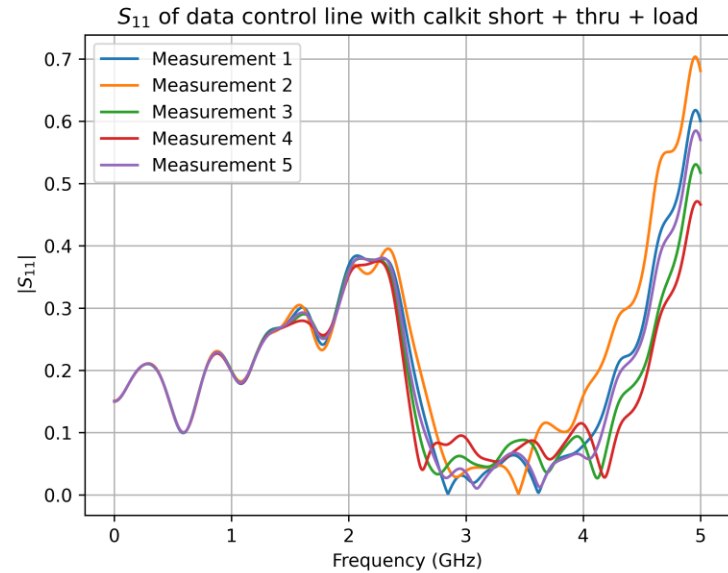
TDR measurements of the clock control line



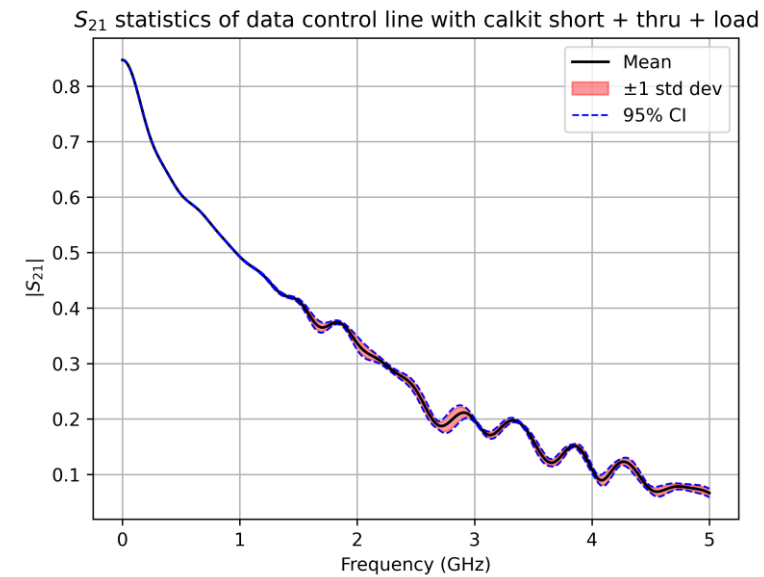
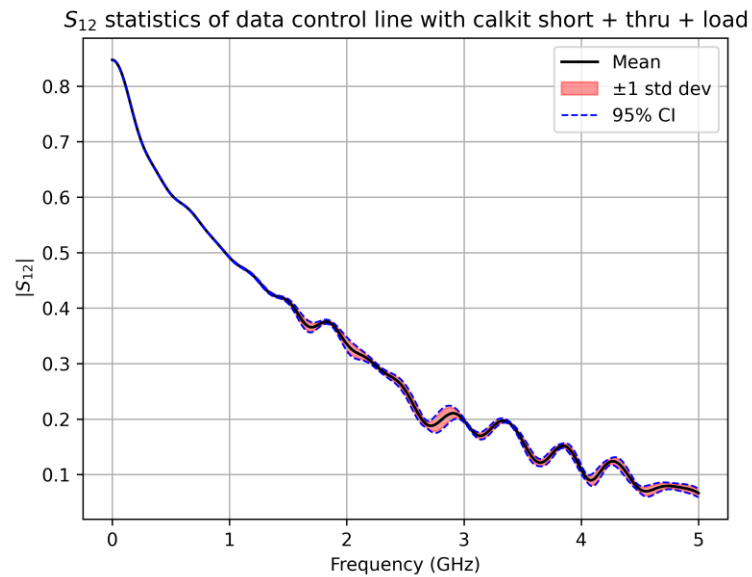
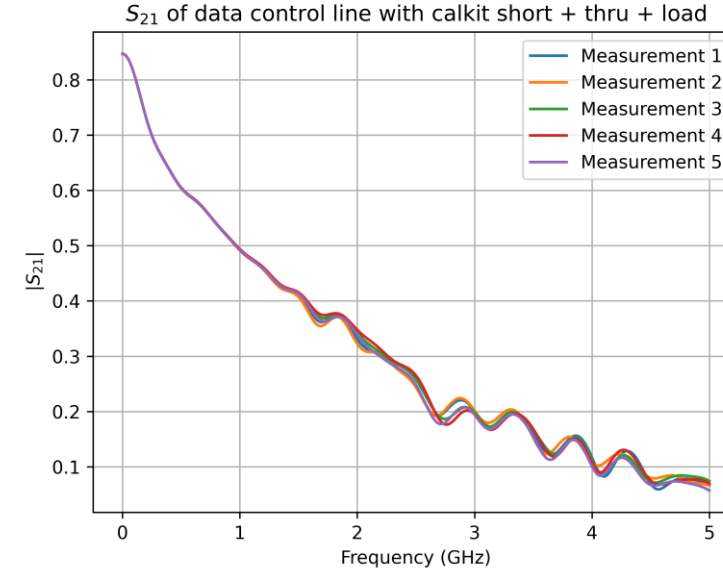
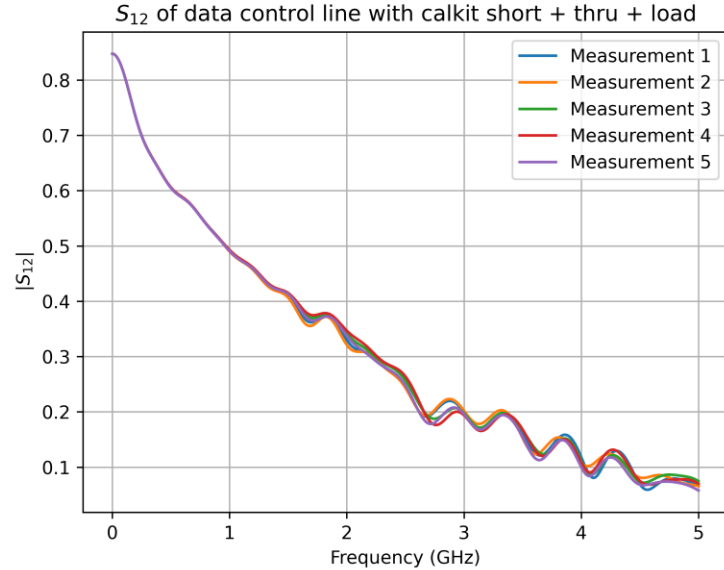
TDR measurements of the clock control line



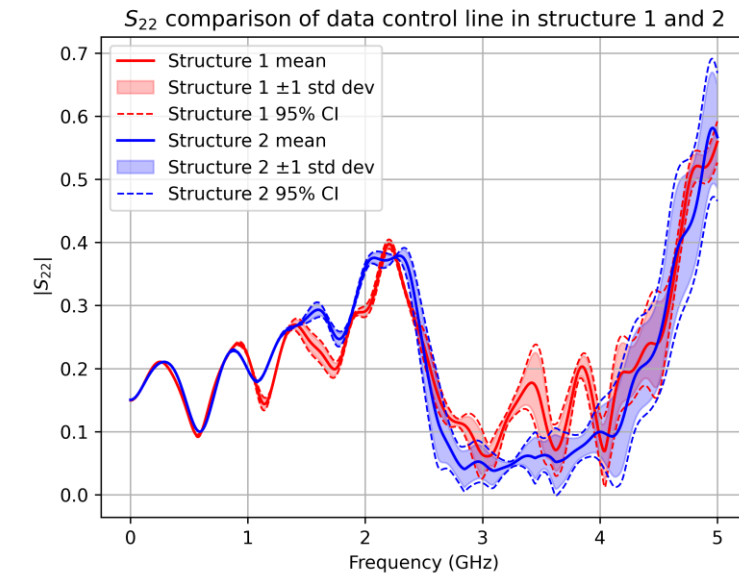
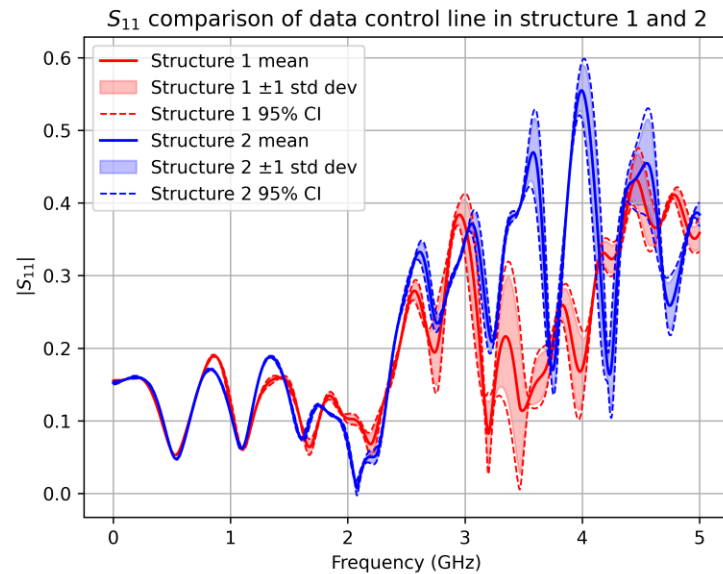
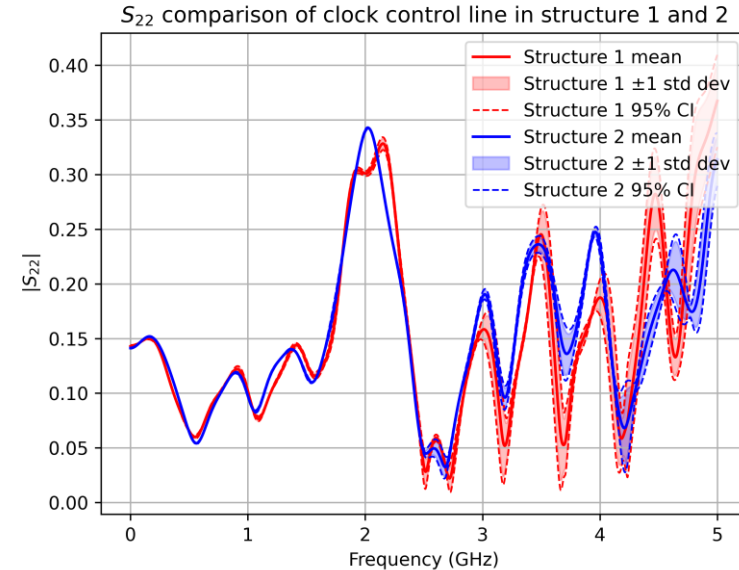
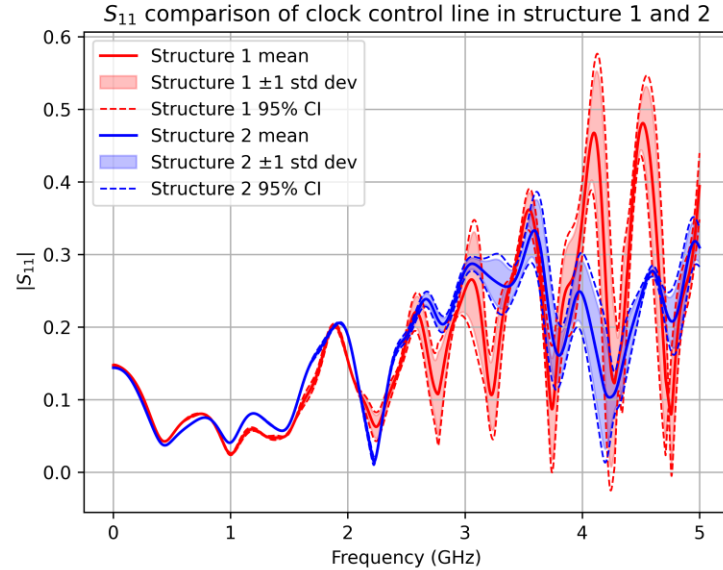
TDR measurements of the data control line



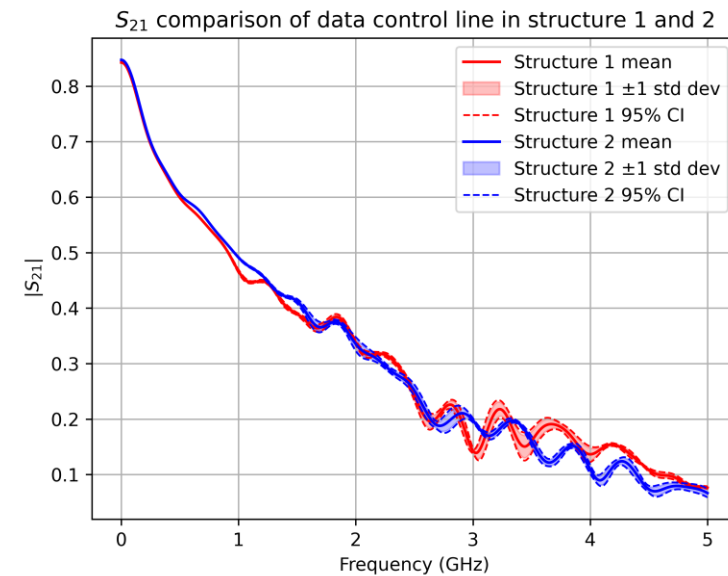
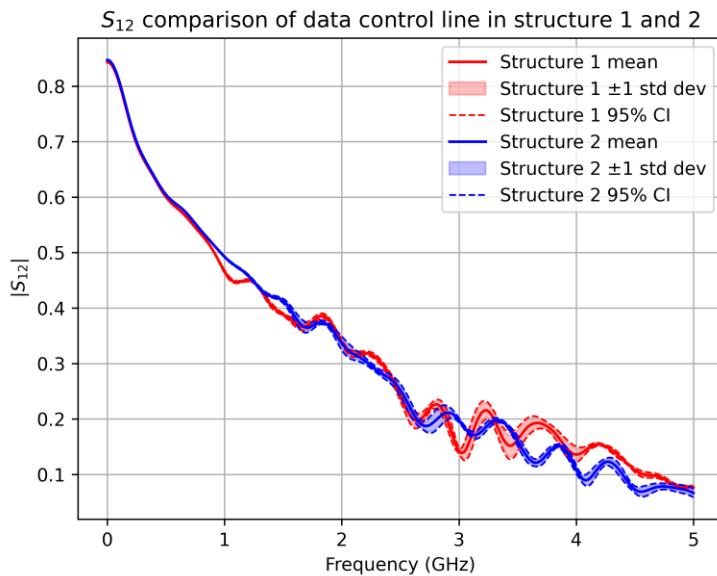
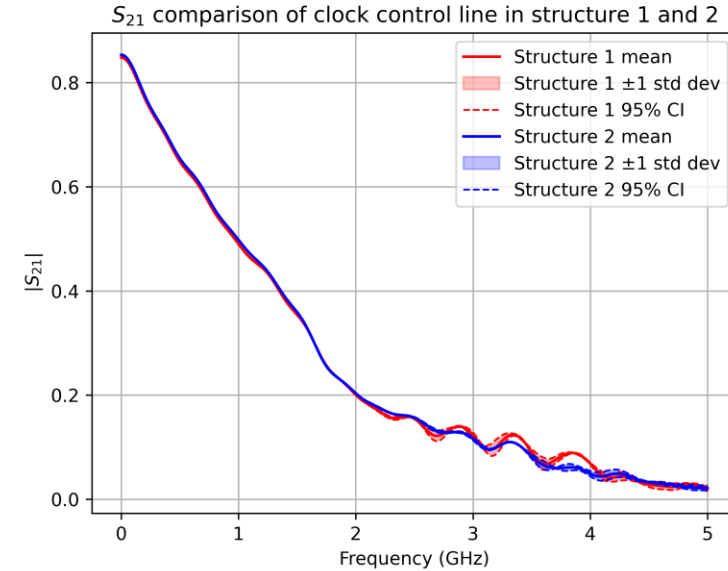
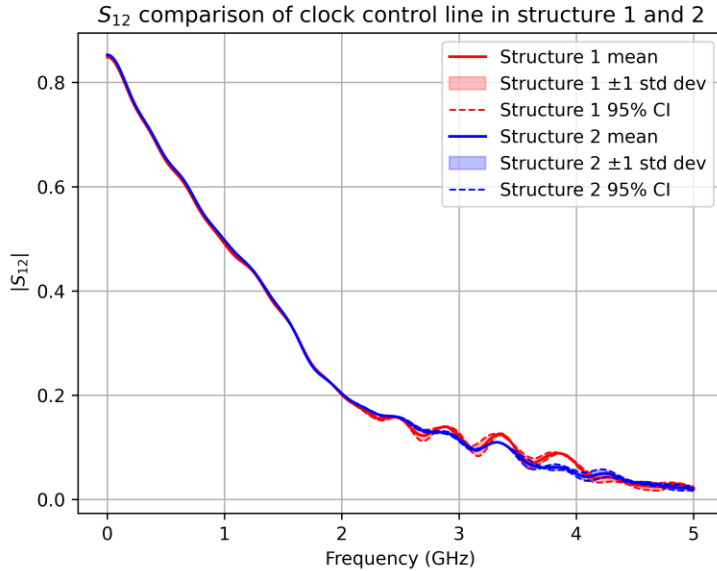
TDR measurements of the data control line



Comparison of structures 1 and 2

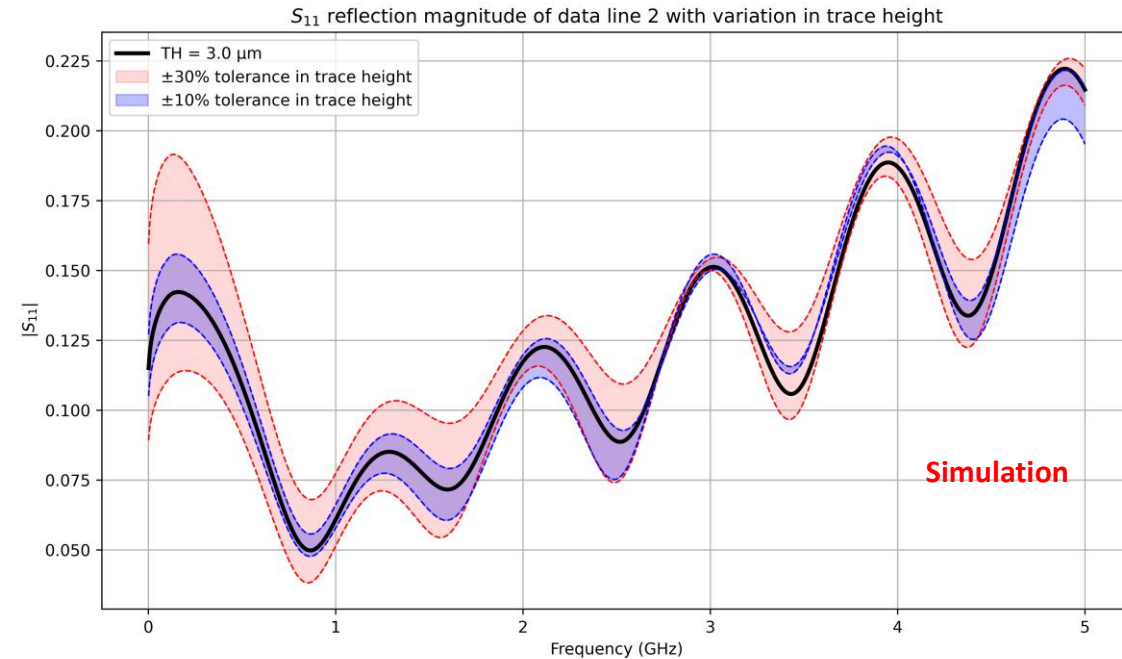
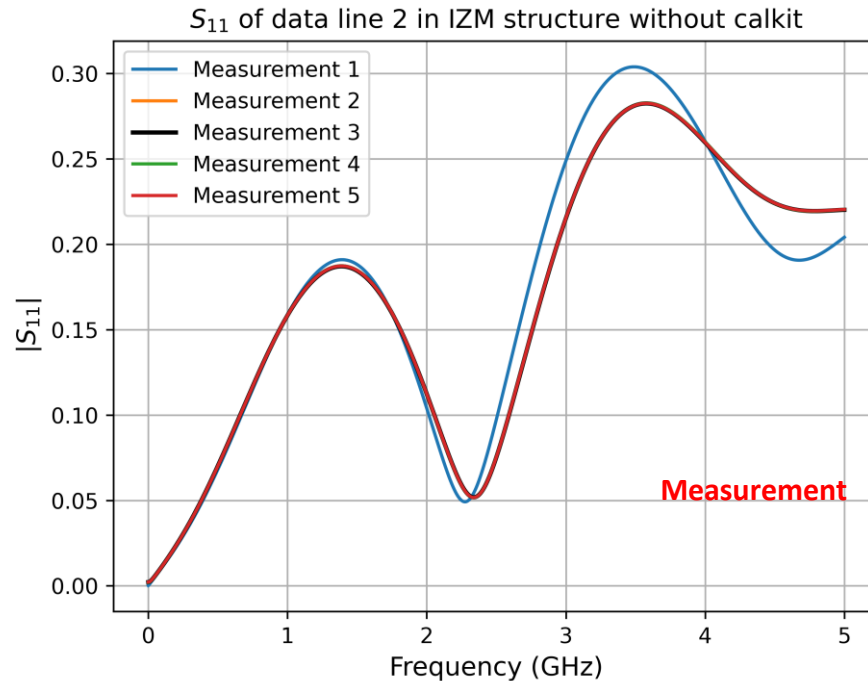


Comparison of structures 1 and 2



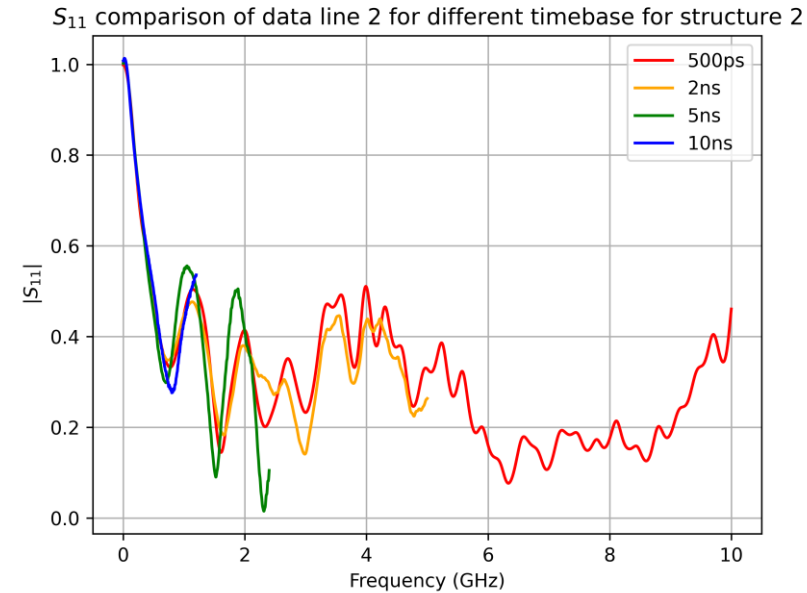
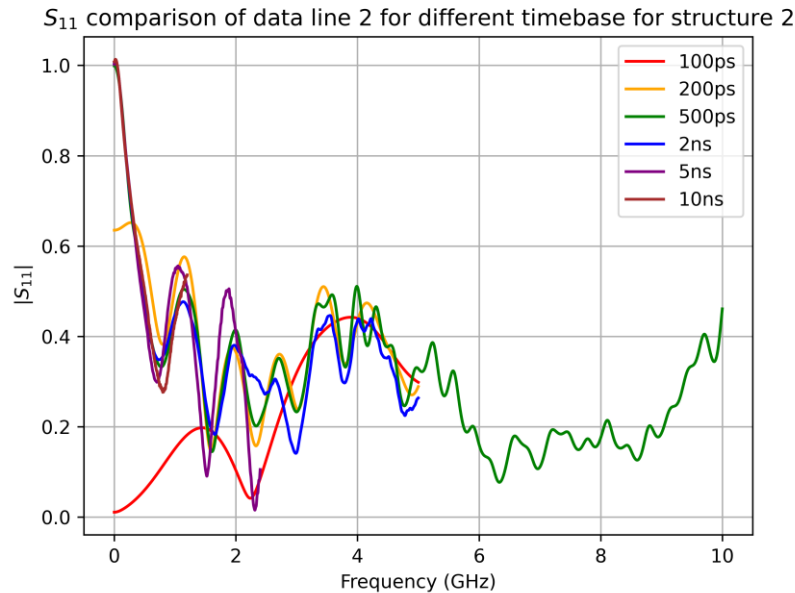
Comparison of simulations and measurements

Improved simulations (with frequency-dependent dielectric and rough trace surface)



- Reflection pattern in simulation suggests that reflections are occurring at a length of ~ 95 mm (from the via at the end of the line), but in measurement, it is at a length of ~ 43 mm (Impedance mismatch in line).
- This is tricky to realize in simulations because of mesh-creating issues
- Currently working on this issue

TDR measurements of data line 2



- Timebase is the time over which the waveform for TDR measurement is acquired. For example 100ps timebase, TDR device will record S-parameters only for the first 100ps. After 100ps, it will not record any reflection coming from the structure.
- Data line 2 is approximately 600ps long, therefore 100ps timebase is not sufficient.
- At least need $2 \cdot 600\text{ps} = 1.2\text{ns}$. Ideally $> 5 \cdot 600\text{ps} = 3\text{ns}$ to cover all the reflections.
- Increase the timebase while keeping the same record length; the oscilloscope has to spread the same number of sample points over a longer time interval; therefore, it decreases the maximum frequency to maintain resolution.

Next steps :

- Redo the measurement of data line 2 in structure 1 with a different timebase
- Improved simulations of the IZM structure with tolerance in trace height and via height are in progress for all transmission lines

