Cologne Chip: Industrial Partnership and Future Collaboration

Dr.-Ing. Michael Gude
Cologne Chip AG

Company Overview

Cologne Chip

1994 Founding year of **Cologne Chip Designs GmbH**.

1996 Presentation of world's first single-chip-solution for ISDN.

2000 Rebranding to **Cologne Chip AG** and sales in millions of units after annual growth rates by 100%

2007 Establishment of the **XHFC-Series** with open access to drivers and software; part of Linux Kernel since v. 2.6.27.

2020 Introduction of a new product line: **GateMate FPGA**.

> 30 Years

Experience in Semiconductor Business

Certified Quality

100 %

On-time Deliveries

designed and manufactured in Germany

Reliable Supply Chain

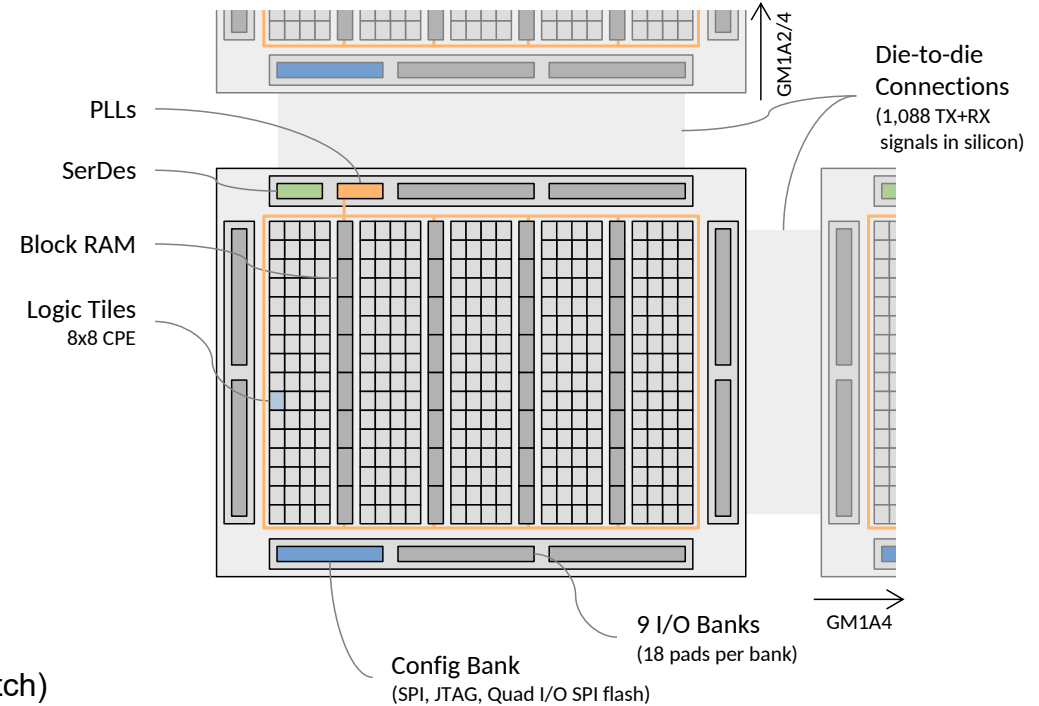
GateMate FPGA

Features at a glance

FPGAs MADE IN GERMANY

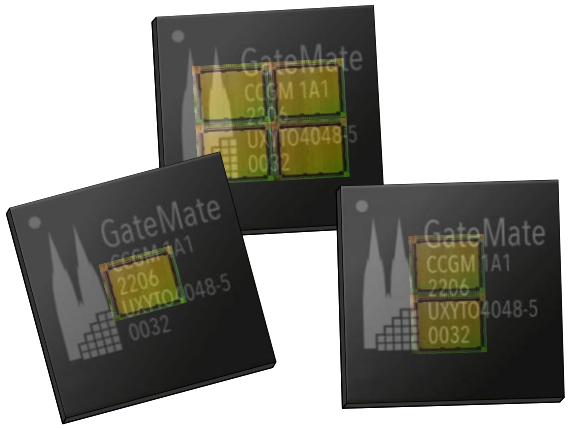
Cologne Chip

- Globalfoundries™ 28 nm SLP process (Fab 1 Dresden, Germany)
- 20,480 programmable elements per FPGA-die
  - 8 inputs or 2x 4 independent inputs + 2 flip-flops
  - 1- or 2-bit full adder or 2x2-bit multiplier
- All 162 GPIO configurable as single-ended or LVDS differential pairs with DDR support
- 32x 40 Kbit RAM cells (Total 1,280 Kbit)
- 4 Clock Generators (PLLs)
- 5 Gbit/s SerDes Controller
- Core voltage from 0.9V to 1.1V
  I/O voltage from 1.2V to 2.5V
- **Open Source Toolchain** using yosys and nextpnr
- A1, A2, A4: 324-ball FBGA package (15x15 mm, 0.8 mm pitch)



GateMate FPGA Series

Feature Summary by Device



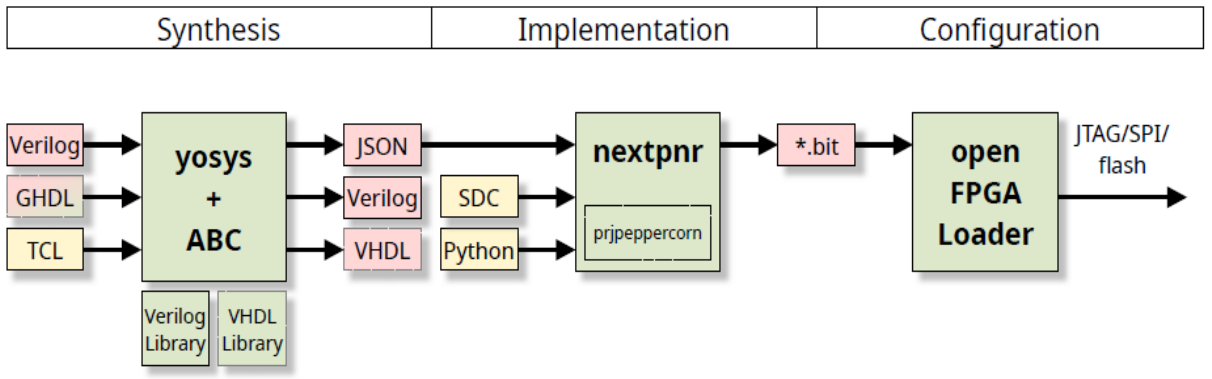
* Patented Technology

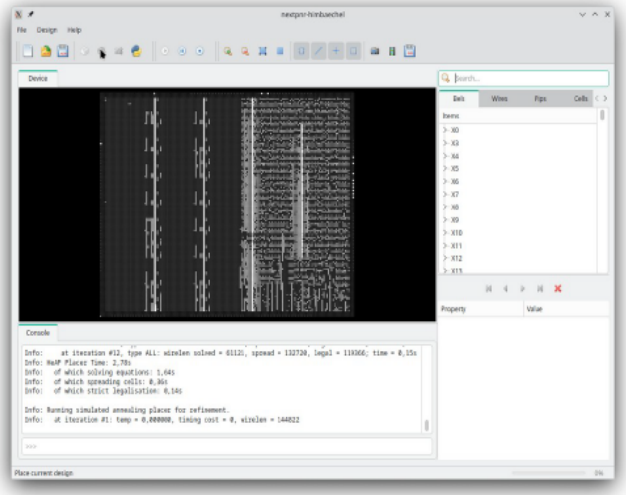
Device	CPEs	FFs	Block RAM		PLL	SerDes	GPIO		Package
			20K	40K			Single-ended	Diff. Pairs (LVDS)	
A1 ★	20,480	40,960	64	32	4	1	162	81	324 FBGA 15x15 mm
A2 ★	40,960	81,920	128	64	8	2	162	81	324 FBGA 15x15 mm
A4	81,920	163,840	256	128	16	4	154	77	324 FBGA 15x15 mm
...									
A25	512,000	1,240,000	1600	800	100	25	tba	tba	tba

★ Mass Production ★ Engineering Samples

GateMate Toolchain

Open-Source at Every Step





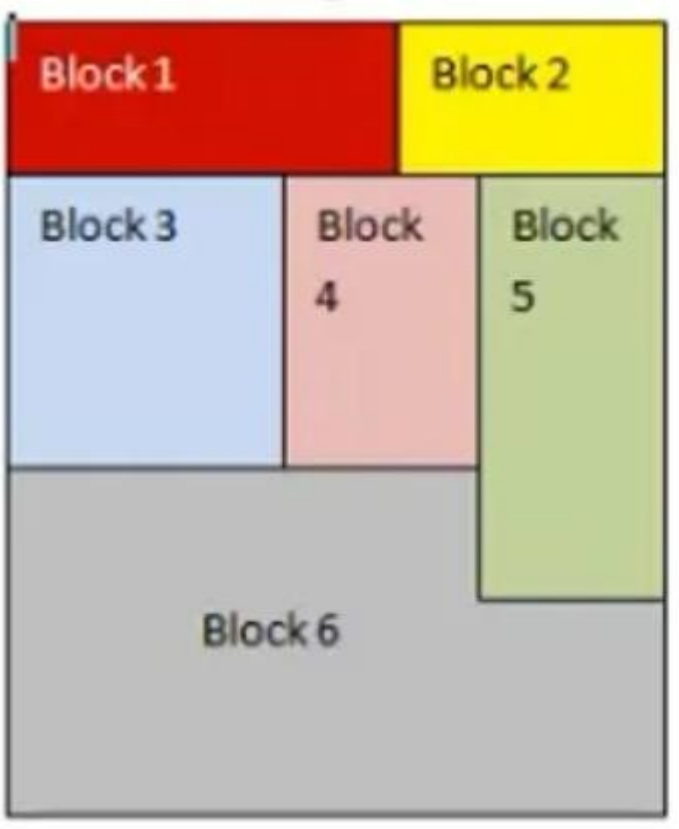
»nextpnr« user interface

GateMate Toolchain new features

Floorplanning:

Chip area can be defined for every HDL Source Module

So, customer can define for the A2…A25 on which Die the circuit is located.



GateMate
Integrated Development Environment (IDE)

Cologne Chip

ONE WARE Studio

- HDL – Editor
- Test Bench Editor
- Simulation Environment
- IO-Editor (Pin Planner) with direct feedback from EVAL-board
- Programming Environment
- ONE AI Application Suit (additional, but low cost)

Radiation Effects on Electronics

Cologne Chip

Total Ionizing Dose (TID)

- Cumulative radiation exposure over time
- Causes threshold voltage shifts, leakage current increase, and eventual parametric degradation or failure of transistors

Single-Event Effects (SEE)

- Single-Event Upset (SEU): Bit flip in memory or configuration
- Single-Event Transient (SET): Temporary gitch in logic

Go to document

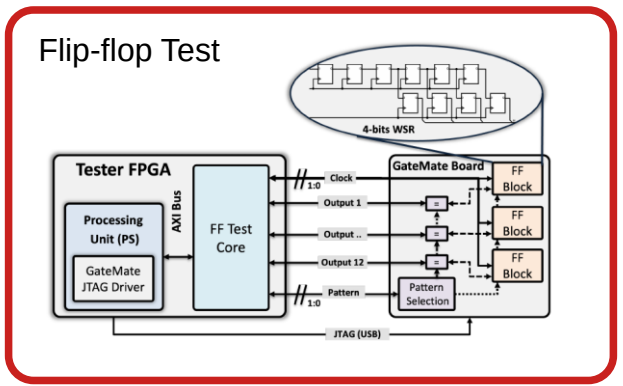
Damaging Effects: Latch-up & Beyond

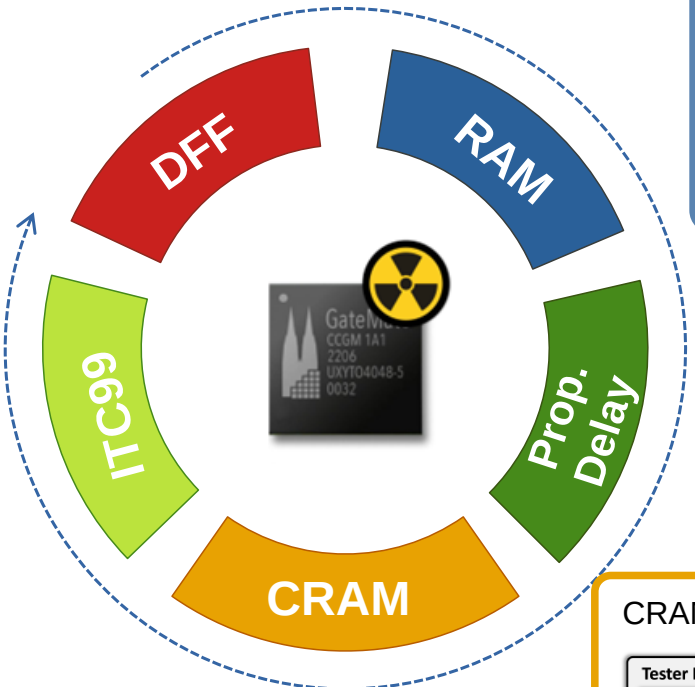
- Most severe radiation-induced failure: You don’t want that

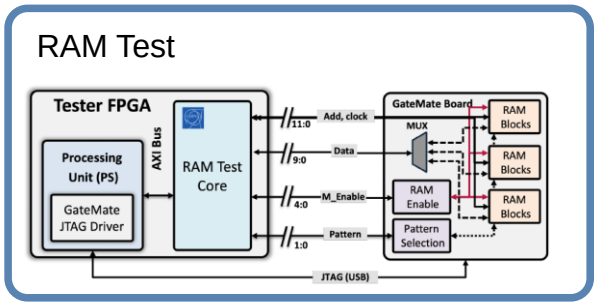
Radiation Tests

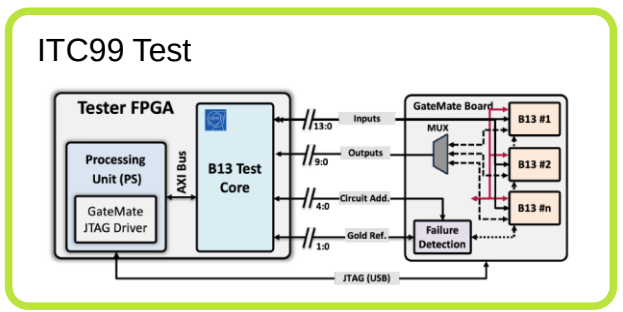
SEE & TID Test Structures

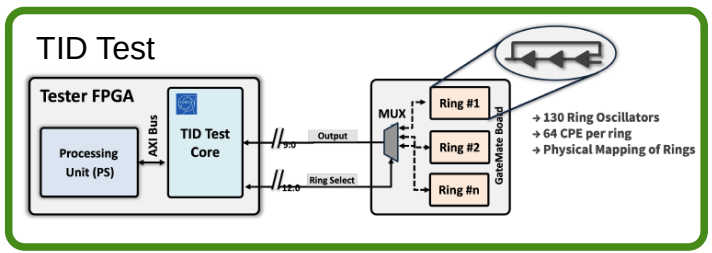
Single event effects / Total ionization dosis

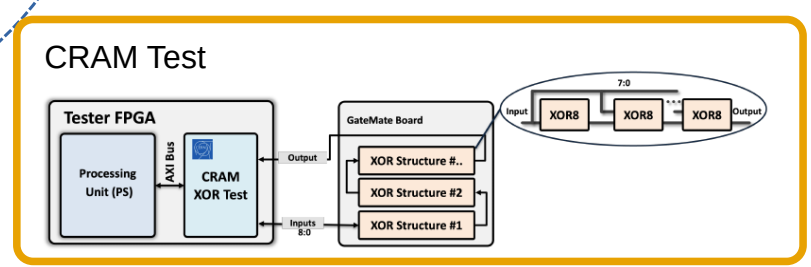








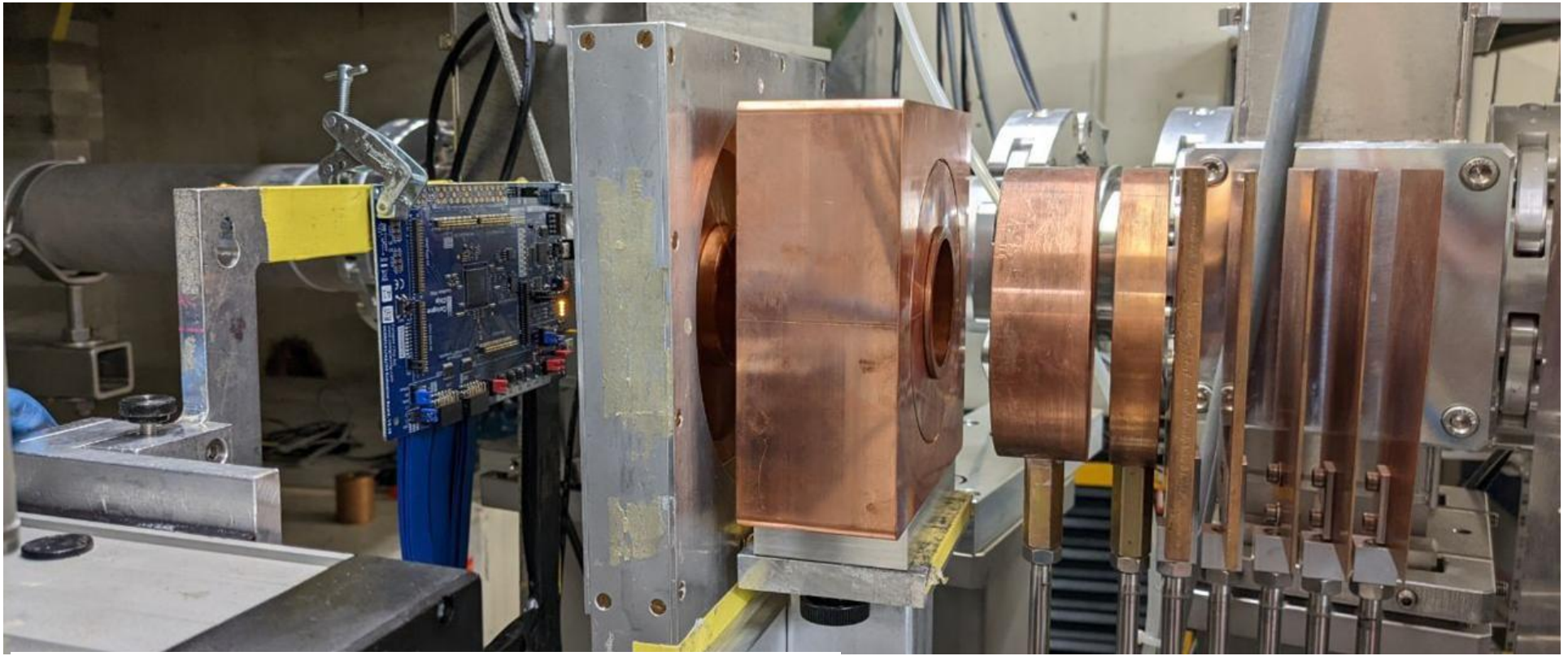




Radiation Tolerant Version of GateMate is available soon

Radiation Test Setup

at Paul Scherrer Institut (PSI) measurements made at CERN Geneva

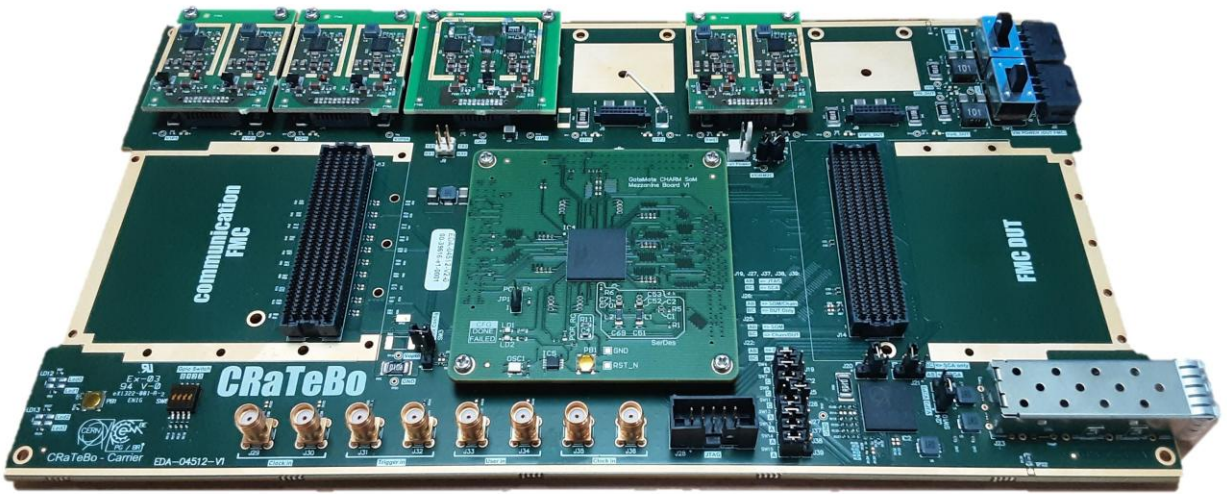


Proton Beam Setup @ PSI

CraTeBo System on Module

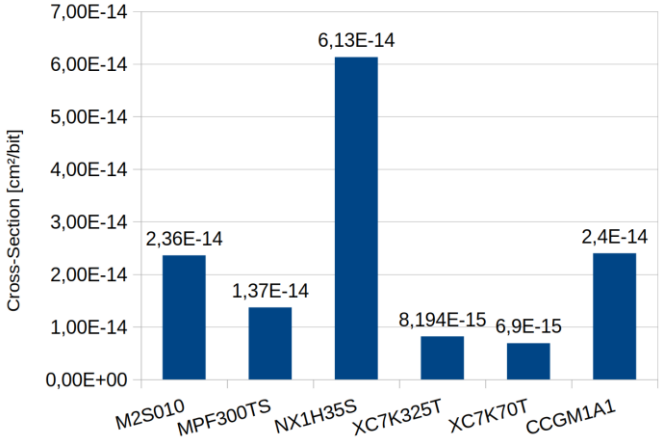
For TID Tests at CHARM

Entire Evaluation Board
exposed during TID test

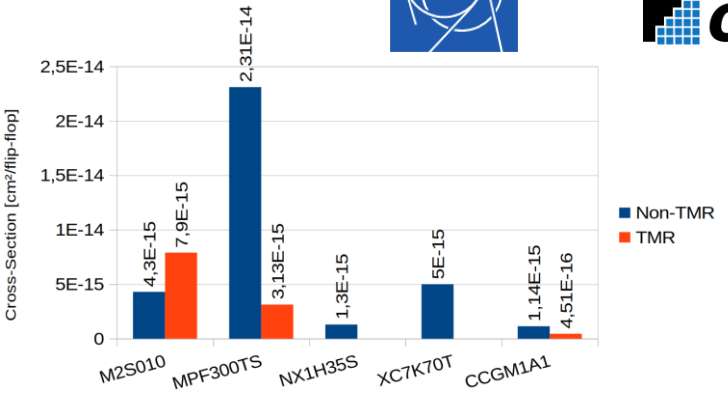


CERN's Radiation-hardened CraTeBo Platform

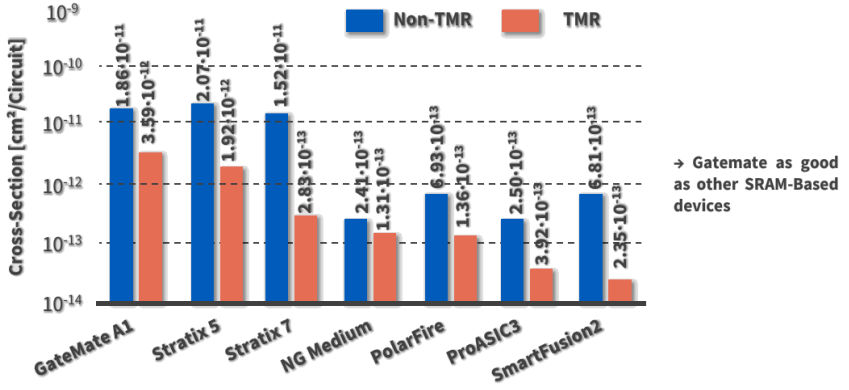
SEE Test Results
at Paul Scherrer Insitut (PSI)



Comparison of BRAM test results



Comparison of flip-flop test results

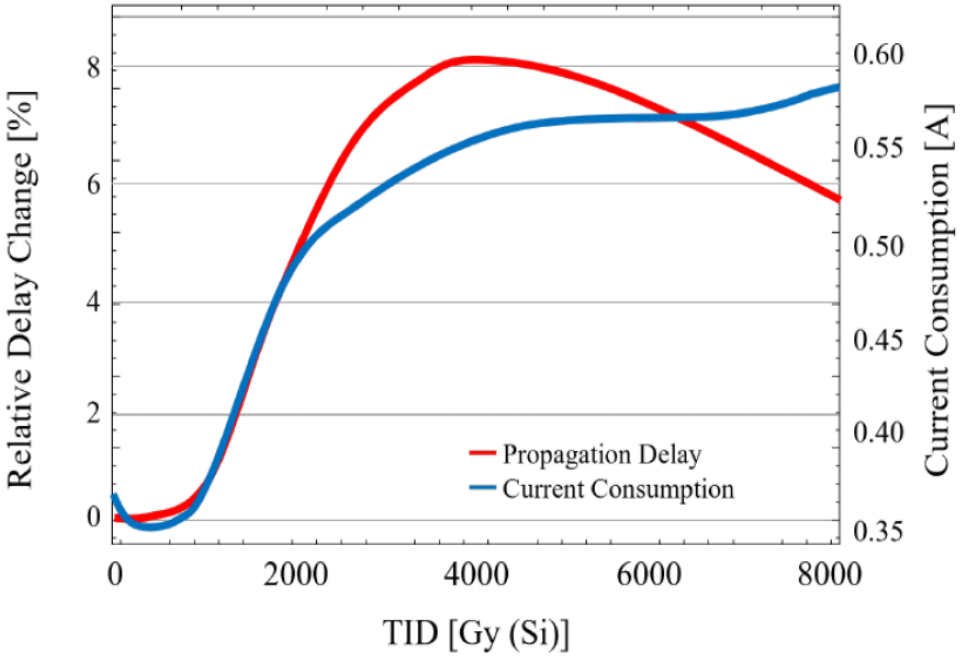


Comparison of ITC99 test results

[1] Radiation Qualification of the Cologne Chip GateMate A1 FPGA

TID Test Results

at CHARM Irradiation Infrastructure (CERN)



- No degradation up to **1kGy**
- Good correlation b/w propagation delay increase and current consumption increase up to **4kGy**
- Good robustness to TID

Cooperation Projects with Akademia and Industry

Cologne Chip

Fentwums:	**Open-Source-Entwurfs- und Visualisierungsumgebung für dynamisch konfigurierbare Mikrochips**
Gate-V:	**Hochoptimierte Open-Source-RISC-V-Prozessoren für universelle Anwendungen**
GoodTimes:	**Open-Source Timing für moderne Mikroelektronik**
ChipsEDU:	**Chipdesign in Ausbildung und Lehre**
SEE-AI:	**Sicherer und energieeffizienter Mixed-Signal-Prozessor für Edge-KI in sicherheitskritischen Systemen**

Thanks for your Attention
Questions?

Dr. Michael Gude
Cologne Chip AG

Eintrachtstr. 113
50668 Köln

https://colognechip.com
info@colognechip.com