Gefördert durch:

Bundesministerium
für Forschung, Technologie
und Raumfahrt

eFPGA Technologies: Vision and Opportunities for the IHL

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- FPGA CAD Tools
- Partial Reconfiguration
- Reliability
- Applications
- eFPGAs
- Hardware Security

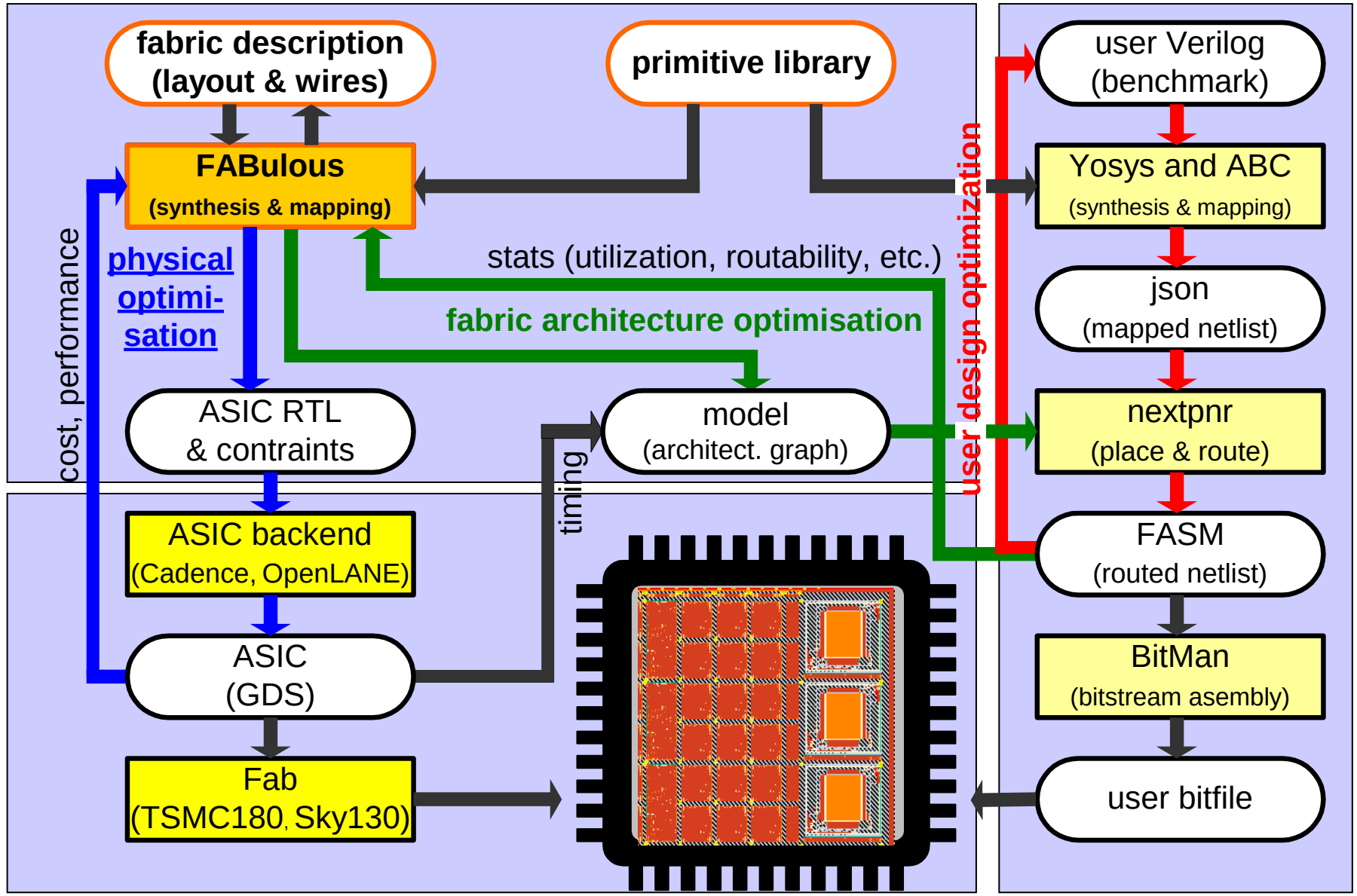
- 16K RISC-V Threads on U55c; 1GHz RISC-V; RISC-V in 90 LUTs

The FABulous Framework for Custom eFPGAs

- Fully integrated framework for eFPGAs

Uses many projects:

- Yosys & nextpnr
- OpenLane/ LibreLane
- OpenRAM
- Verilator
- or industry tools…



What is FABulous offering?

- Fully integrated open-source FPGA framework with good quality of results

  (area & performance) → we can achieve >95% core density

- Entirely open and free, including commercial use

- Supports custom cells (if provided), like passgate multiplexers, configuration cells

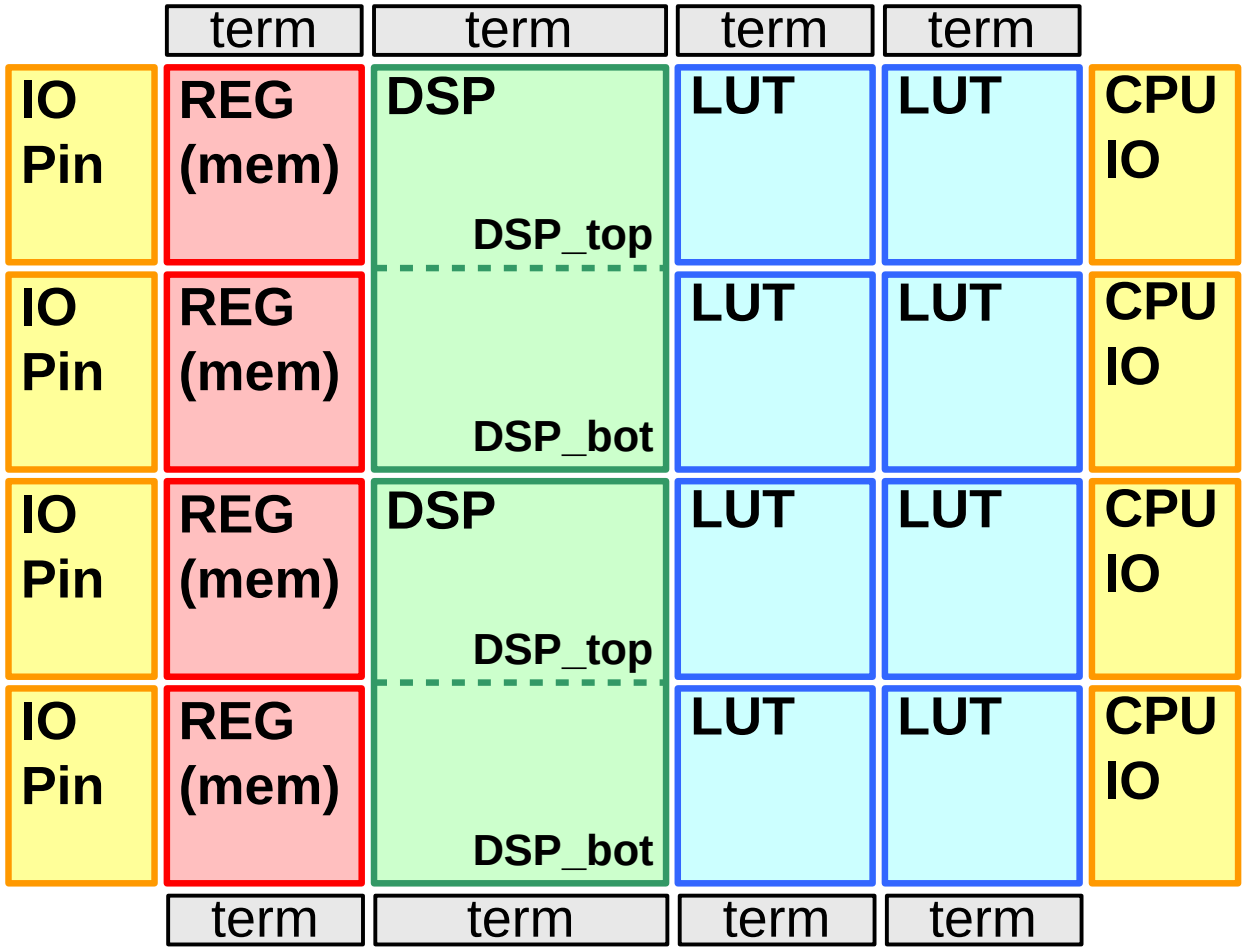
- Supports partial reconfiguration

- Versatile
  - Different flows (LibreLane ←→ Cadance)
  - Easy to customize and integration of own IP (inside the fabric or attached)

- Silicon proven on TSMC 180, 130, 28; **GF 180***; **SKY 130***; **IHP 130*** **(*open)**

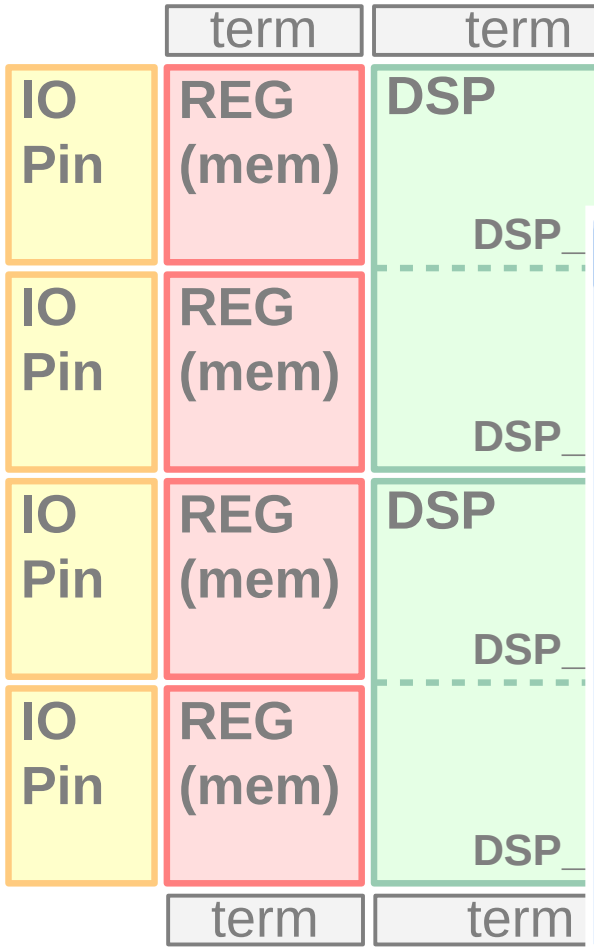
  in development: TSMC N16, GF 22, XFAB 180

Let‘s build a small eFPGA: Fabric Definition



- 4 x register file, 2 x DSPs, 8 x LUT-tiles (CLB), I/Os left and right,

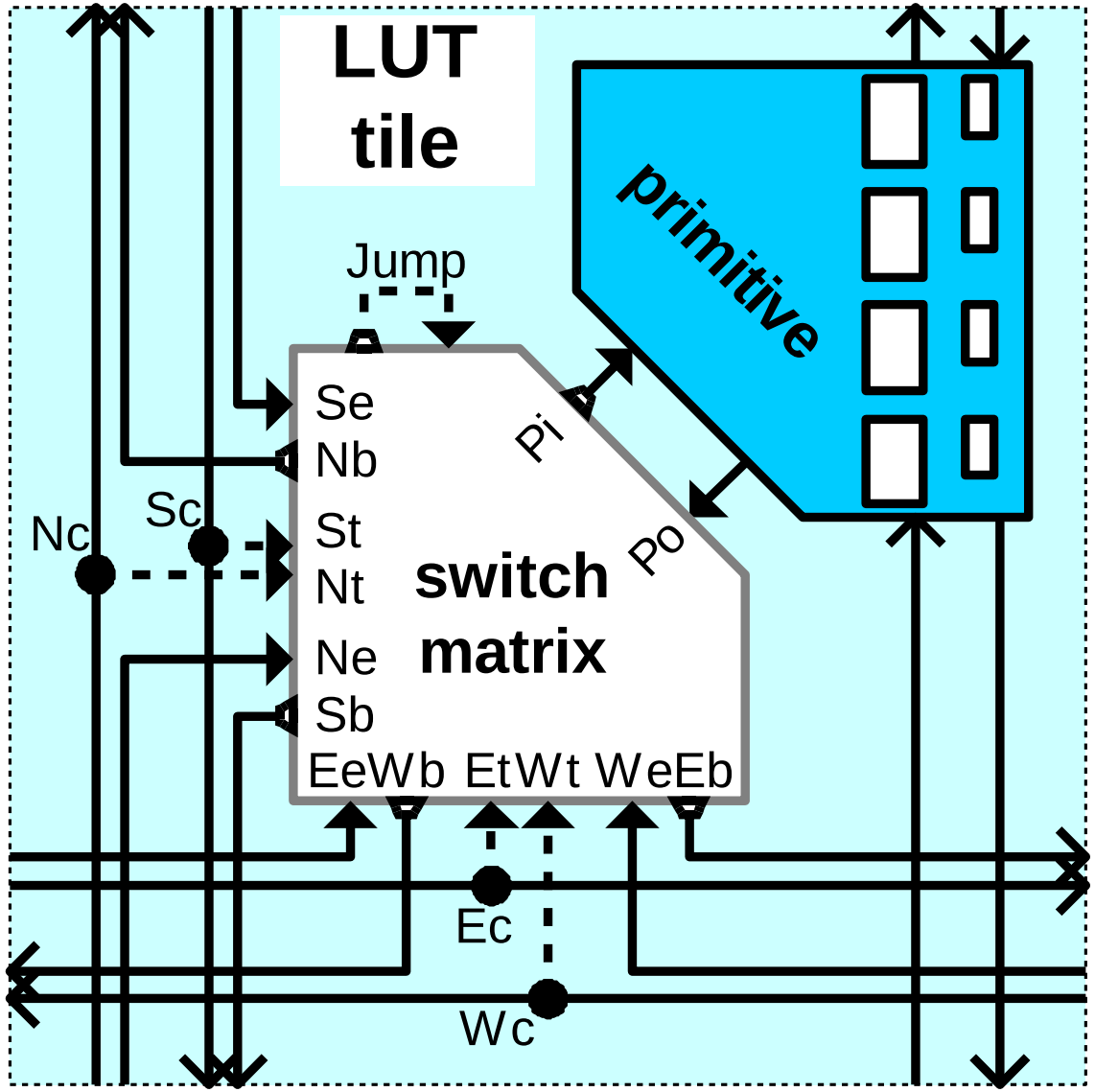
Let‘s build a small eFPGA: Fabric Definition



	A	B	C	D	E	F
1	*FabricBegin*					
2	NULL	N_term	N_term	N_term	N_term	NULL
3	W_IO	RegFile	DSP_top	LUT4AB	LUT4AB	CPU_IO
4	W_IO	RegFile	DSP_bot	LUT4AB	LUT4AB	CPU_IO
5	W_IO	RegFile	DSP_top	LUT4AB	LUT4AB	CPU_IO
6	W_IO	RegFile	DSP_bot	LUT4AB	LUT4AB	CPU_IO
7	NULL	S_term	S_term	S_term	S_term	NULL
8	*FabricEnd*					

- 4 x register file, 2 x DSPs, 8 x LUT-tiles (CLB), I/Os left and right,
- A fabric is modelled as a spreadsheet (tiles are references to tile descriptors)

Let‘s build a small eFPGA: Tile Definition



- Wires
- Switch matrix
- Configuration storage
- Primitives (basic elements) (can be just Verilog/VHDL files)

The FABulous Ecosystem

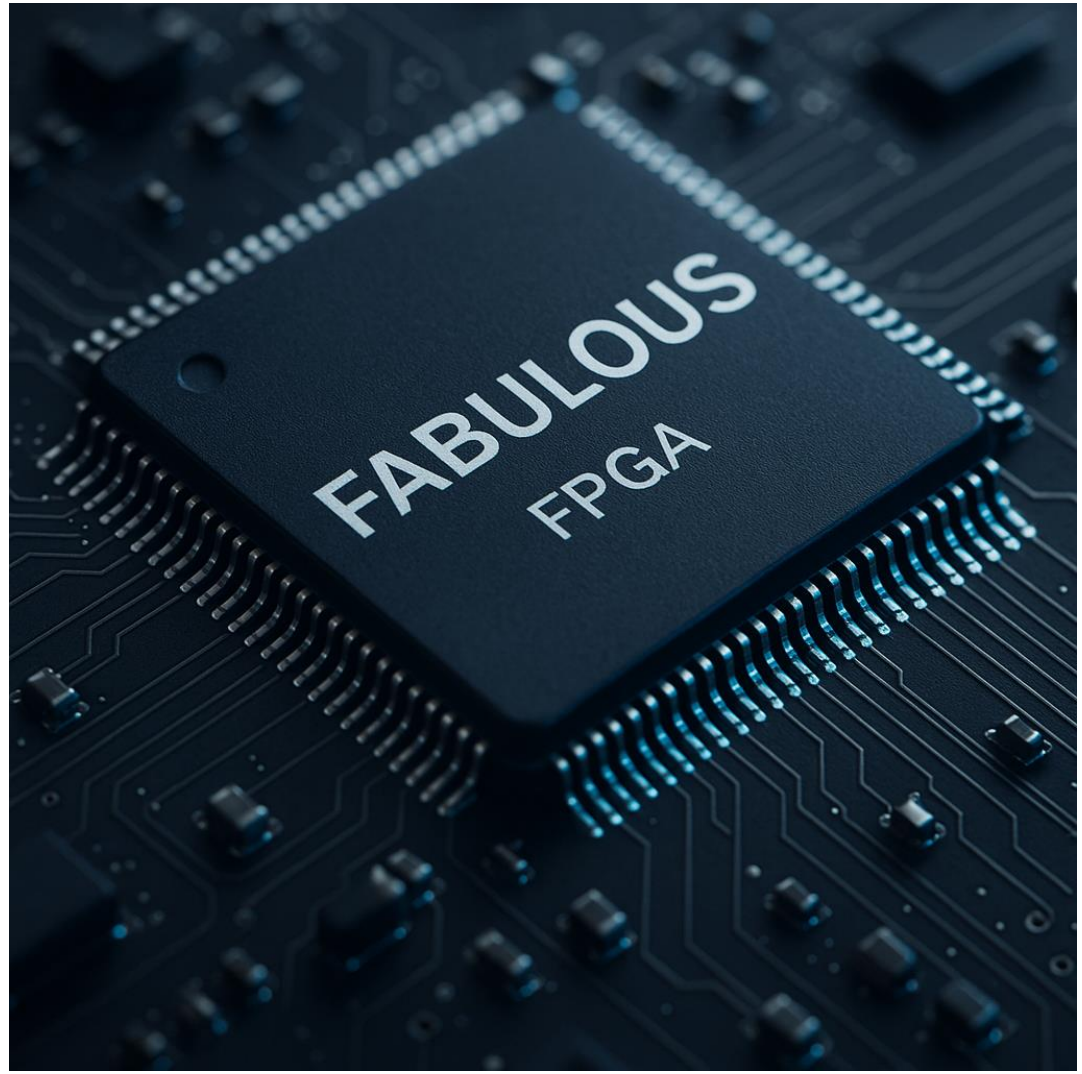
- ASIC generation (GDS)

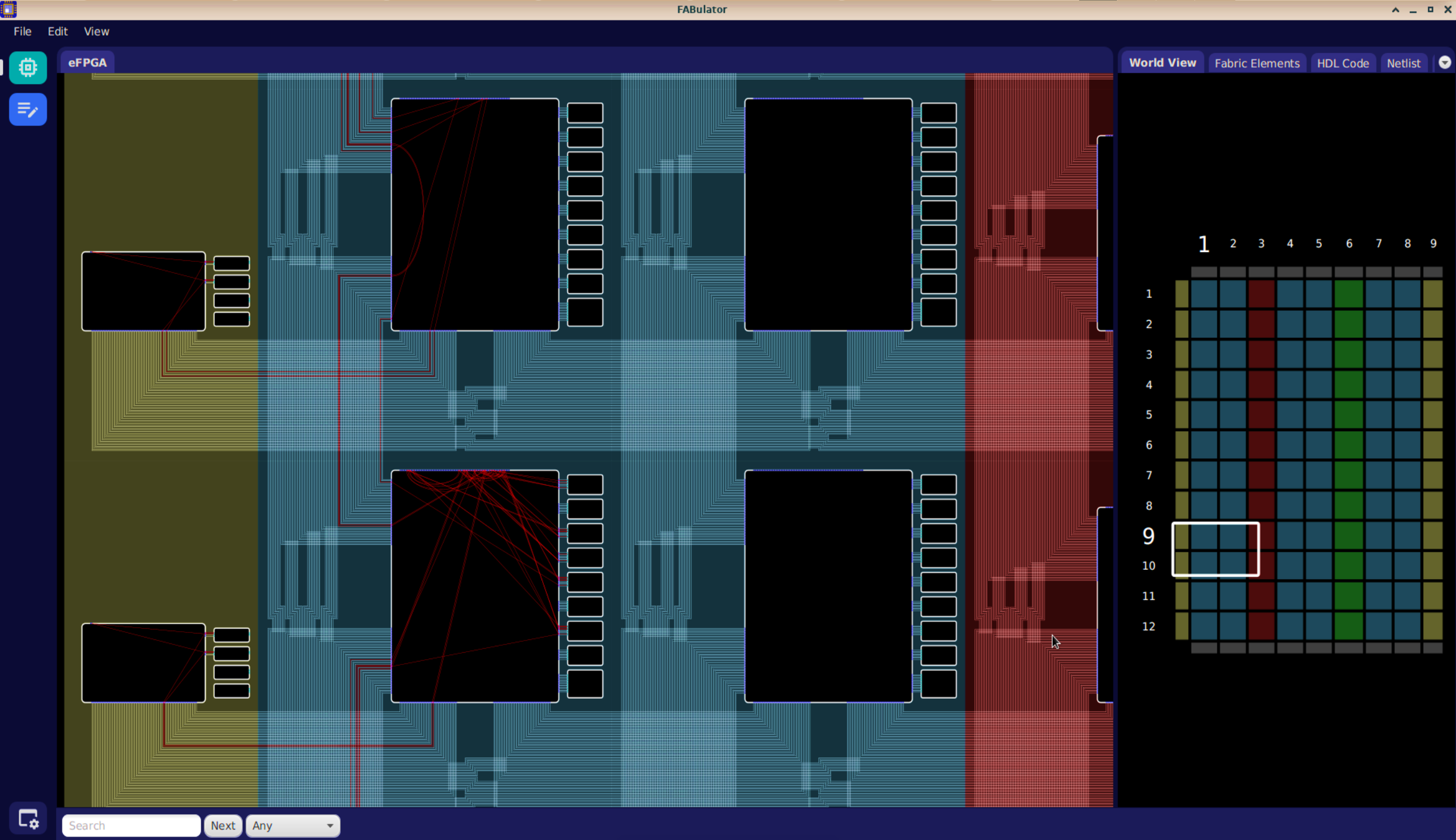
  RTL, constraints, physical optimizations
- FPGA CAD tool adaptation

  (for compiling user bitstreams)
- Simulation and emulation models
- Timing model generation

  (for timing driven place & route)
- Factory test bitstreams (in progress)

- Fully reproducable and deterministic flow




FABulator
File
Edit
View
eFPGA
World View
Fabric Elements
HDL Code
Netlist
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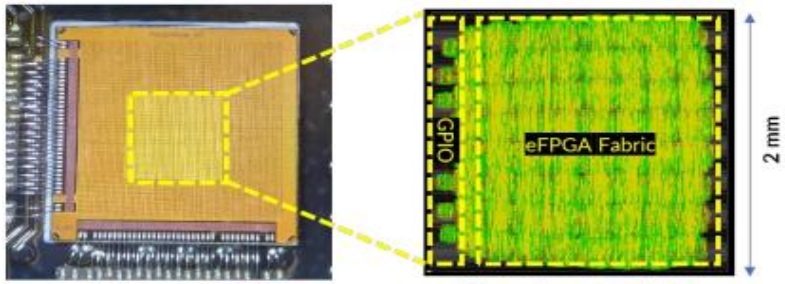
Next
Any

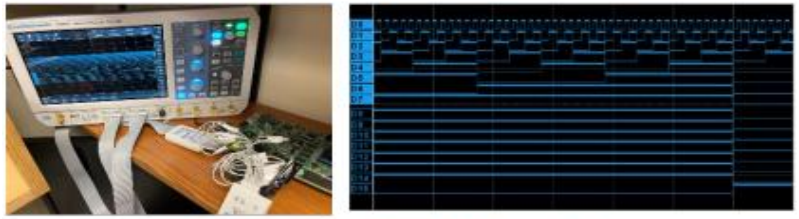
FABulous Users

- **Stanford University**
  TSMC 130 & TSMC 28
- **New York University**
  TSMC 180 & 2x TSMC 28
- **Fudan University (TSMC 28)**
- **University of Bristol (Sky130)**
- **Berkeley (TSMC 130)**



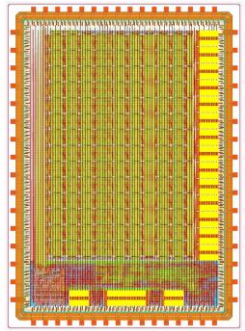
Fabulous v1 ASIC

Floorplan of eFPGA fabric after Place&Route



Outputs from eFPGA (16b counter) probed with oscilloscope

- **Indian Institute of Science, Bangalore**
  → Analog FPGAs
- **Indian Space Research Organisation**
  → GF 180 Testchip
- **Université de Sherbrooke (Canada)**
  → Cyrogenic FPGAs (Quantum Computer)
- **Multiple FPGAs by Leo Moser**
- **Plans with CERN on a rad-hard FPGA**



Radiation-tolerant FPGAs

- **Config bits are exported**

  → can swap SRAM cells for DICE, TMR…

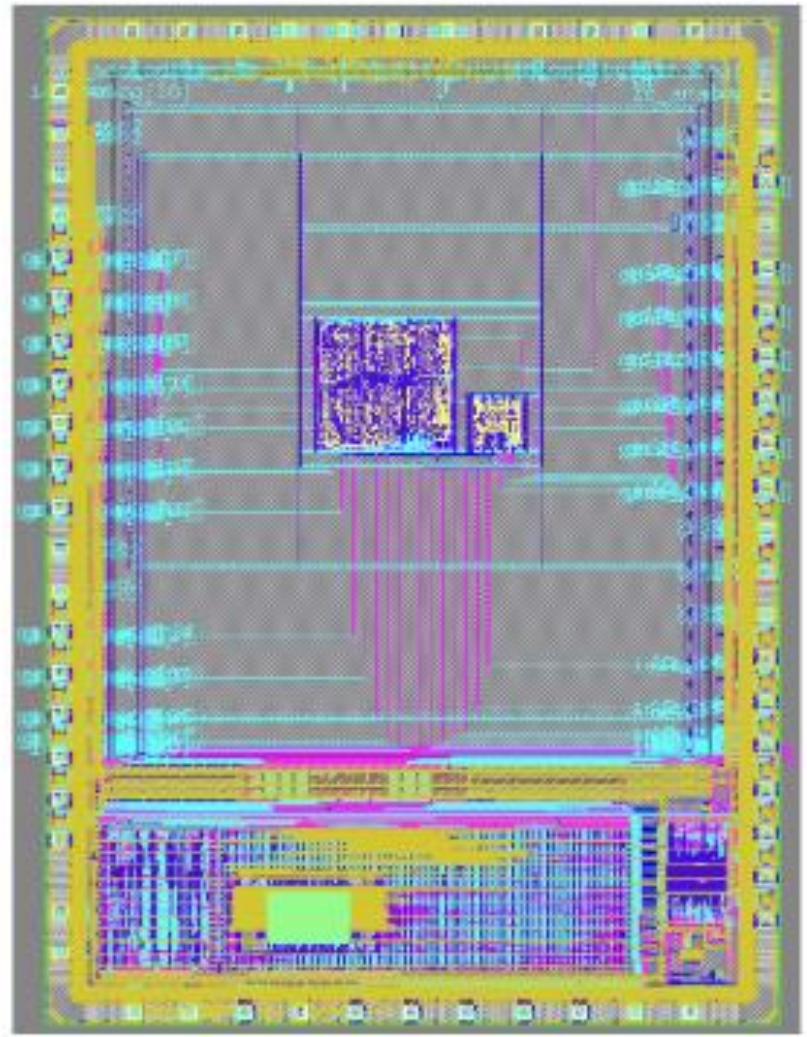
  → we did a ReRAM FPGA

- **Easy to customize logic cells**

  → TMR latches, voters

- **New SAT-based mapper is ideal for mixed criticality**

  → put in redundancy as required



Open_ReRAM_eFPGA

eFPGA Technologies: Vision and Opportunities for the IHL

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Gefördert durch:

Bundesministerium für Forschung, Technologie und Raumfahrt

See our projects under:

https://github.com/FPGA-Research

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