



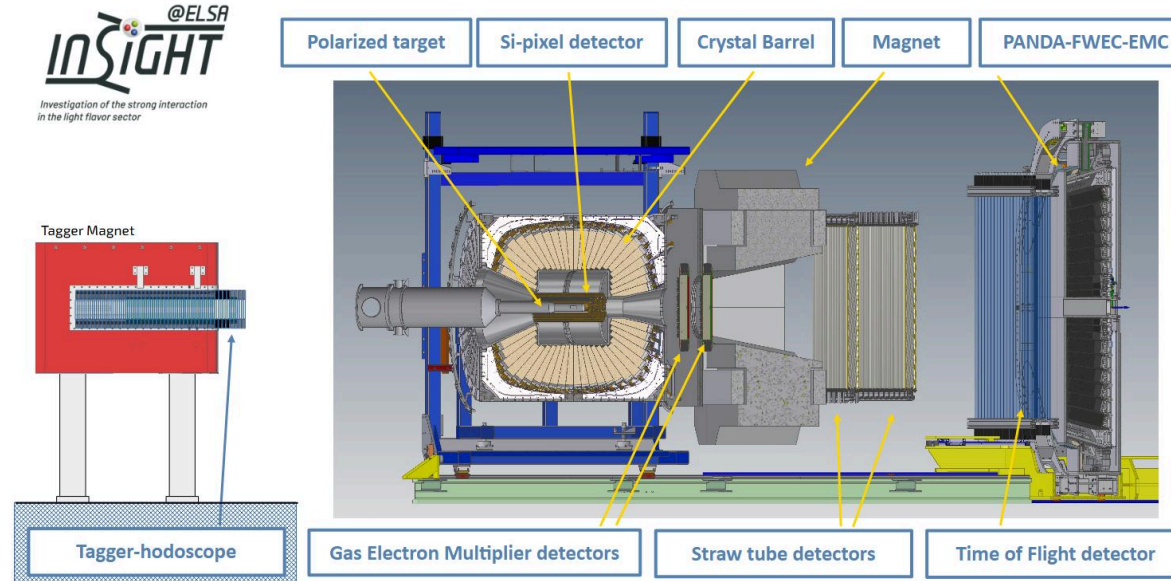
INSIGHT Detector Electronics

Challenges and Opportunities for the IHL

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IHL Kick-Off Meeting · July 17th, 2026

INSIGHT Experiment @ ELSA



- ▶ new experiment at ELSA
- ▶ polarized photons on a polarized target
- ▶ high-resolution photon measurements
- ▶ precise charged-particle detection

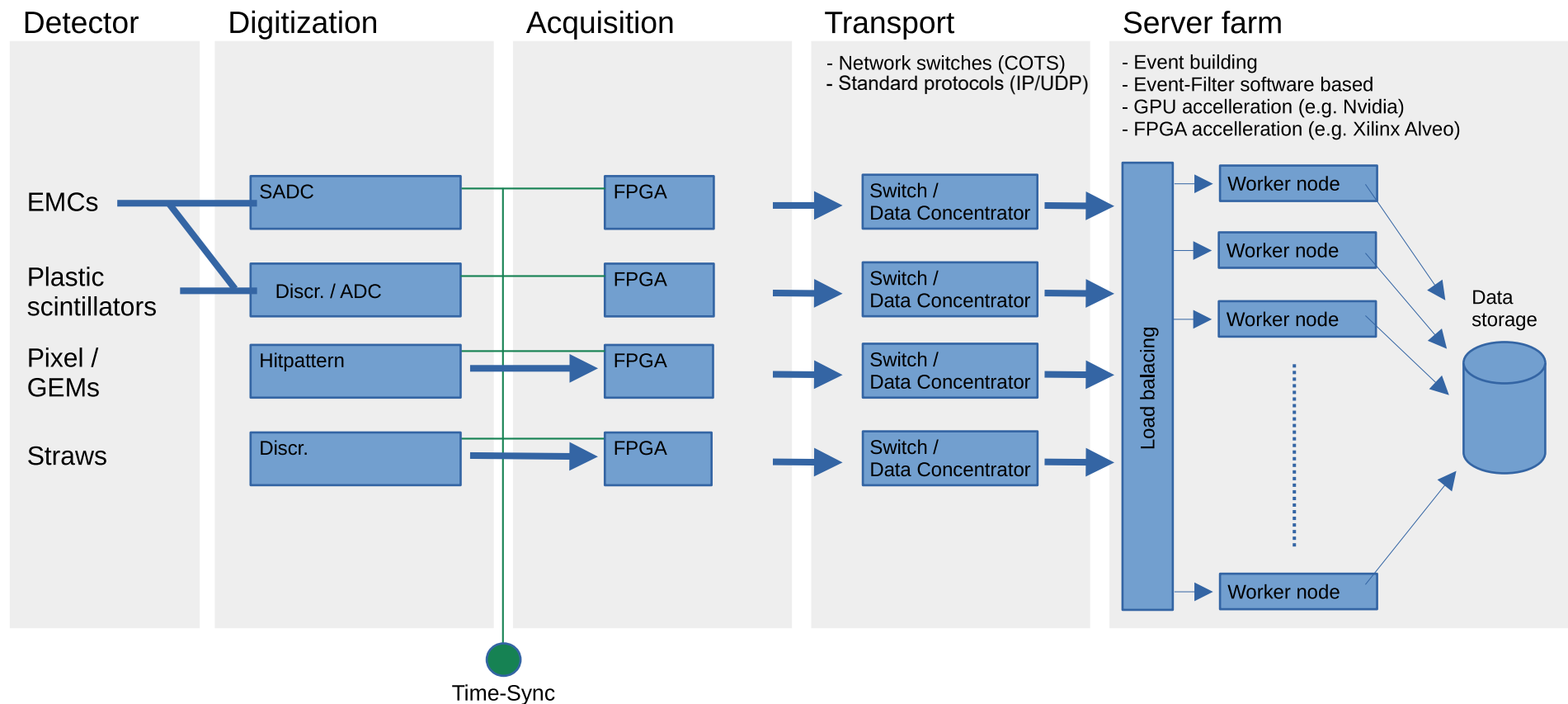
Design Considerations

- ▶ CB/TAPS experiment
 - ▶ triggered readout
 - ▶ low-latency hardware trigger
 - ▶ subdetectors must provide trigger signals
 - ▶ deadtime ($\geq 30 \mu\text{s}$) after each event
 - ▶ **max. event rate limited to $\sim 10 \text{ kHz}$**
- ▶ INSIGHT
 - ▶ total expected data rate: $\sim 2 \frac{\text{GB}}{\text{s}}$

INSIGHT DAQ Philosophy

- ▶ triggerless, streaming DAQ
- ▶ free-running subdetectors
- ▶ send every hit to back-end
- ▶ software trigger / event filter on server farm

INSIGHT DAQ pipeline



FPGAs at INSIGHT ...

... as DAQ workhorses

- ▶ bridge between custom FE electronics and the commercial network world
- ▶ handle synchronization of individual subdetectors

FPGAs at INSIGHT ...

... as DAQ workhorses

- ▶ bridge between custom FE electronics and the commercial network world
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... in special applications

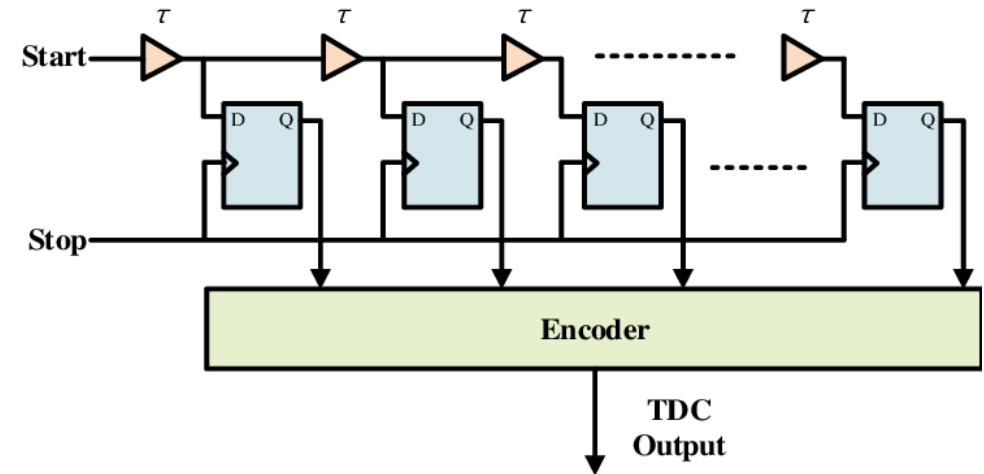
- ▶ tapped delay line TDCs for precise time measurements
- ▶ processing of SADC waveforms (filtering, deconvolution, and feature extraction)

Tapped Delay Line TDCs

- INSIGHT requires precise timing:

$$\sigma_{\text{ToF}} < 100 \text{ ps}$$

- period of FPGA clocks ($> 1.6 \text{ ns}$) is too coarse
- interpolate by measuring signal propagation through a delay line
- use FPGA resources (CARRY4) as a delay line



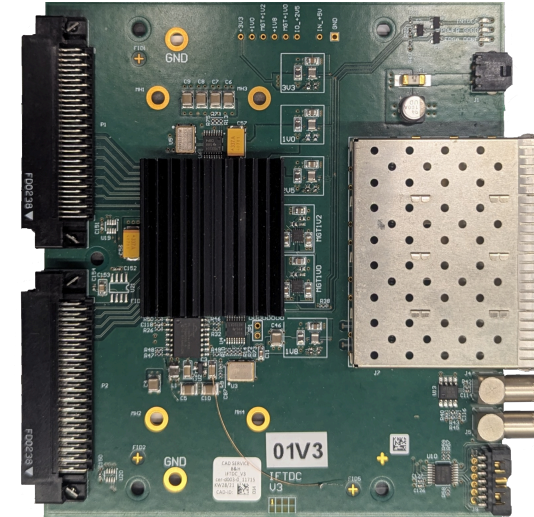
[1]

FPGA-based TDCs at INSIGHT



DiRICHd2 [2]

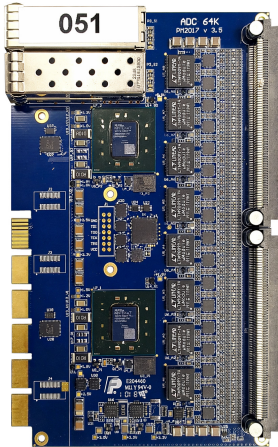
- ▶ Lattice EPC5
- ▶ part of the DOGMA ecosystem [3]
- ▶ developed at GSI



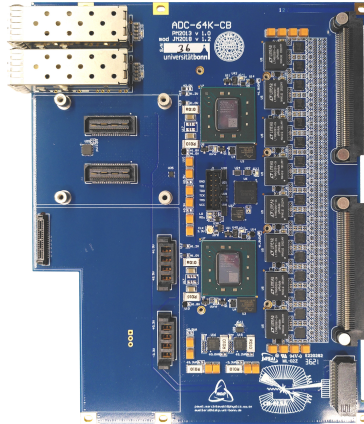
iFTDC [4]

- ▶ Xilinx Artix 7
- ▶ own HDL implementation
- ▶ *ones-counter*-based encoding [5]

The SADC



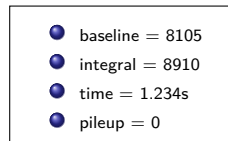
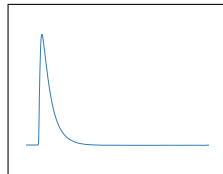
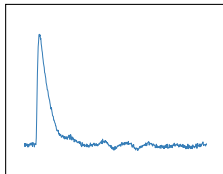
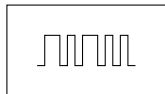
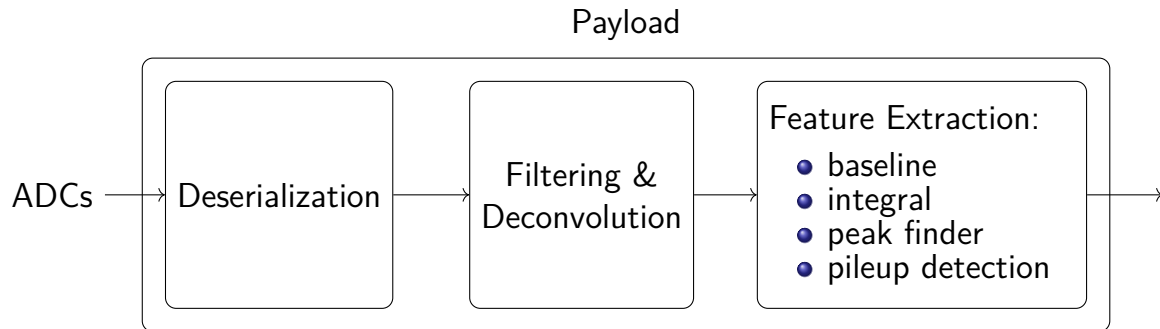
(a) Panda SADC by P. Marciniewski



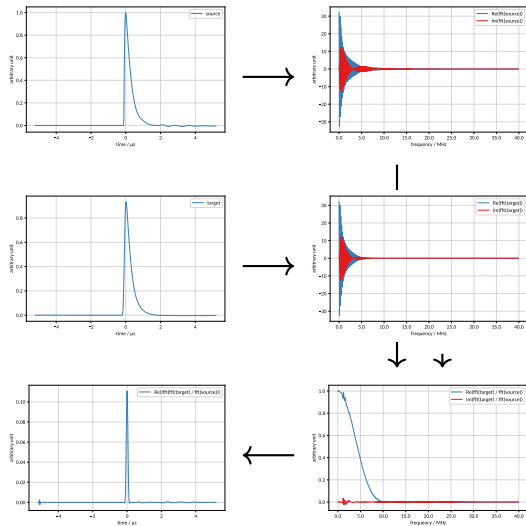
(b) CB SADC by J. Müllers

- 64 channels
- 14 bit @ 80MS/s
- 2 Xilinx Kintex 7 FPGAs

Firmware structure

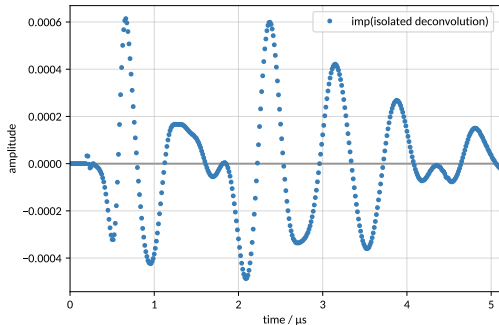


Deconvolution: Steps



- Define source and target waveforms
- Compute fft of both
- Divide ffts
- Perform inverse fft

Deconvolution: Optimization

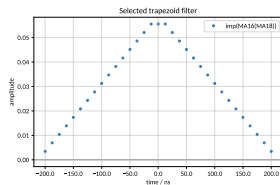
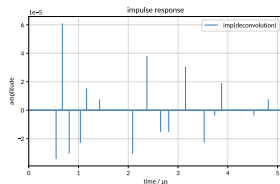
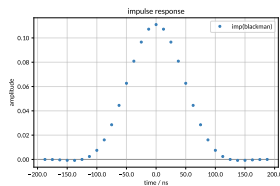


- 379 coefficients, not implementable, 600 DSPs available
- Observation: This deconvolution looks very triangular
- Fit coefficients with triangles
- Triangles can be implemented using two Moving Averages (MAs)
- MAs are easy to implement

Deconvolution: Parts

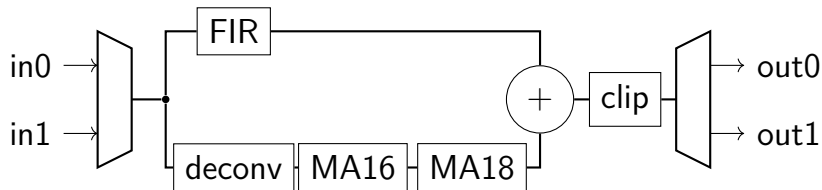
Custom filter c : $c = f + \underbrace{MA(16) * MA(18)}_{h^{-1}} * g$

- f : short FIR lowpass filter
- $MA(16) * MA(18)$: Trapezoid filter
- g : fitted deconvolution kernel
- not optimized: ≈ 400 coefficients
- my approach: 16 coefficients



Deconvolution: Implementation

- Coefficients and positions need to be quantized: 6 bit are enough
 - DSP are used when sensible
 - Don't need multiplication for powers-of-two
 - Can group coefficients when they are a factor of power-of-two apart: -12, 3
- ⇒ 2 channels per filter @ 160 MHz ⇒ 3 DSPs needed per channel



Summary – FPGAs at INSIGHT

... as DAQ workhorses

- ▶ move data from front end to the network
- ▶ synchronization of subdetectors

... in special applications

- ▶ tapped delay line TDCs
- ▶ processing of SADC waveforms

... supported by a small team

also interested in

- ▶ reusable HDL designs
- ▶ testing
- ▶ good HDL tooling

References

- [1] P. Chen *et al.*, “A 1-ps Bin Size 4.87-ps Resolution FPGA Time-to-Digital Converter Based on Phase Wrapping Sorting and Selection,” *IEEE Access*, vol. 10, pp. 126429–126439, 2022, doi: [10.1109/access.2022.3225873](https://doi.org/10.1109/access.2022.3225873).
- [2] M. Becker *et al.*, “Qualification of DIRICH readout chain,” *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 1056, p. 168570, Nov. 2023, doi: [10.1016/j.nima.2023.168570](https://doi.org/10.1016/j.nima.2023.168570).
- [3] M. Traxler and others, “The DOGMA DAQ System.” [Online]. Available: <https://dogma.gsi.de/>
- [4] I. Konorov, J. Friedrich, K. Eichhorn, M. Losekamm, T. Maehrholz, and S. Paul, “The iFTDC front-end cards for the COMPASS and AMBER experiments,”

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- [5] Y. Wang, J. Kuang, C. Liu, and Q. Cao, “A 3.9-ps RMS Precision Time-to-Digital Converter Using Ones-Counter Encoding Scheme in a Kintex-7 FPGA,” *IEEE Transactions on Nuclear Science*, vol. 64, no. 10, pp. 2713–2718, Oct. 2017, doi:
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Backup

INSIGHT Rates

