UNIVERSITÄT BONN

Analog & Mixed-Signal ASIC Design

current activities, interests, and future collaboration

University of Bonn

Ichi Kishishita

Topics

- Fast ADC
- Cryogenic ASIC

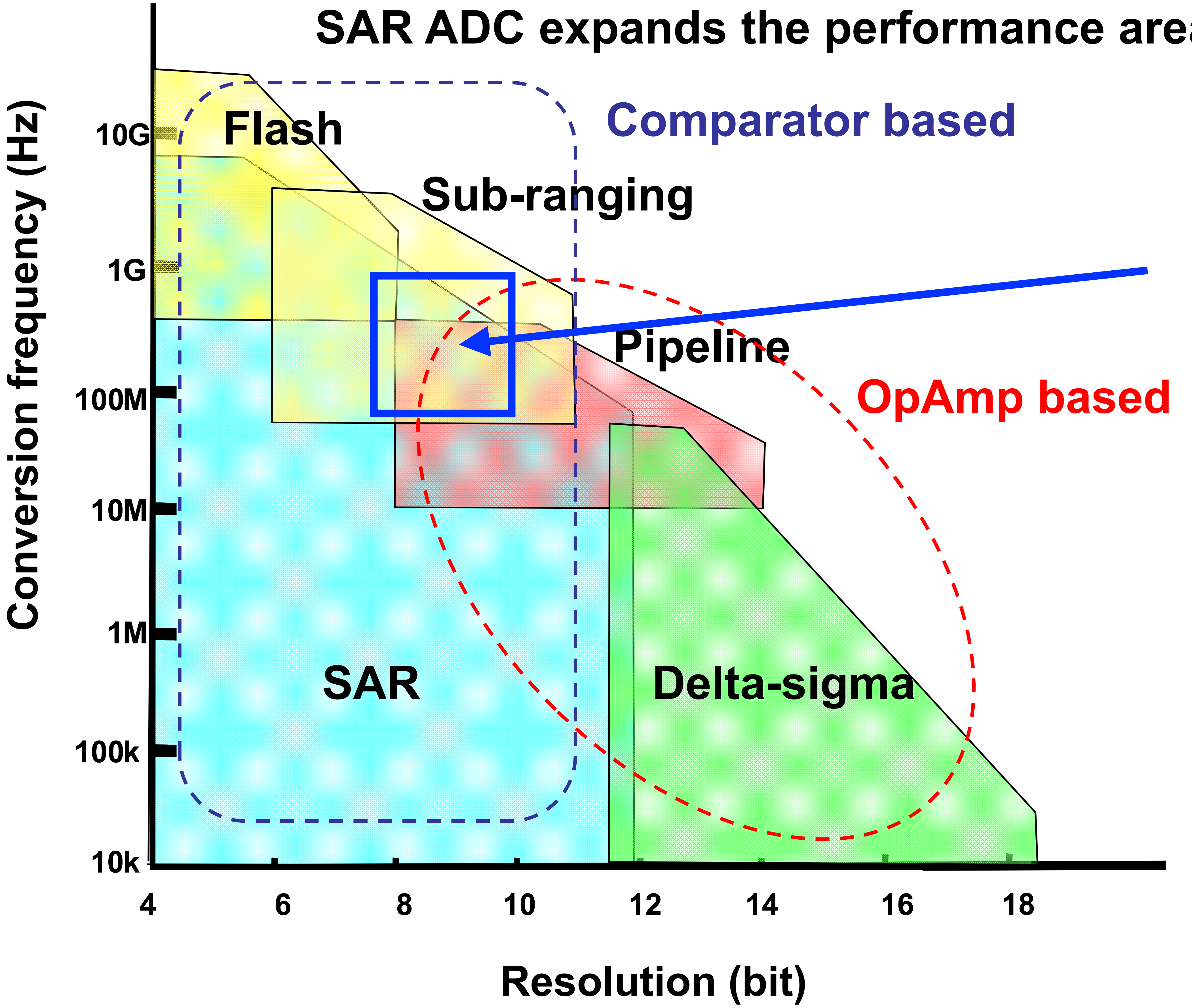
IHL Kickoff Meeting, 17. July, 2026

Current activities: Fast ADC design

Rad-hard, Fast ADC is still crucial component in big-data experiments (eg, ECAL upgrade).

A. Matsuza

ADC has a suitable performance domain.

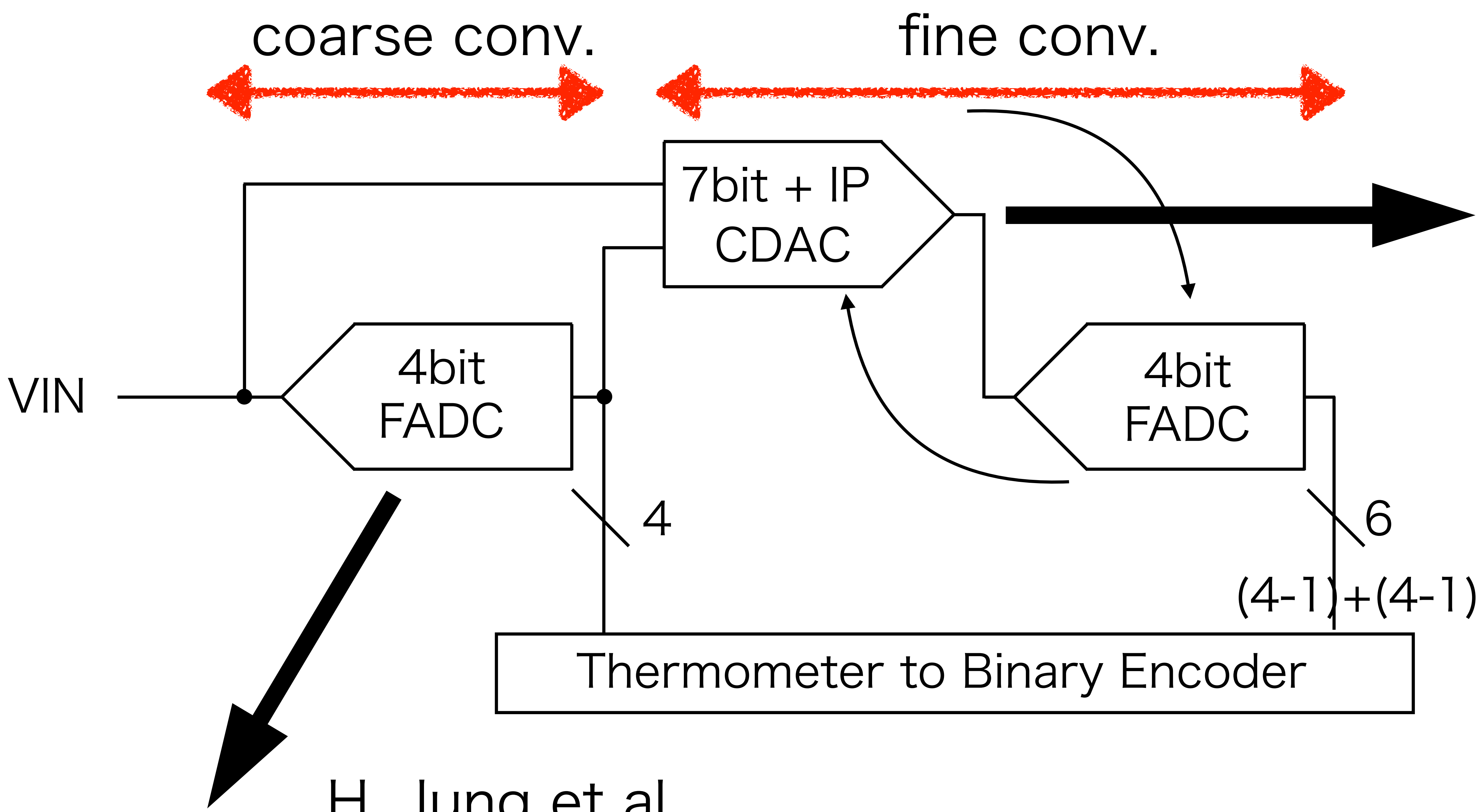


Our target range (8-10b, 100M-1GS/s)

- **Electron microscope with DEPFET**
- **Quantum computing**

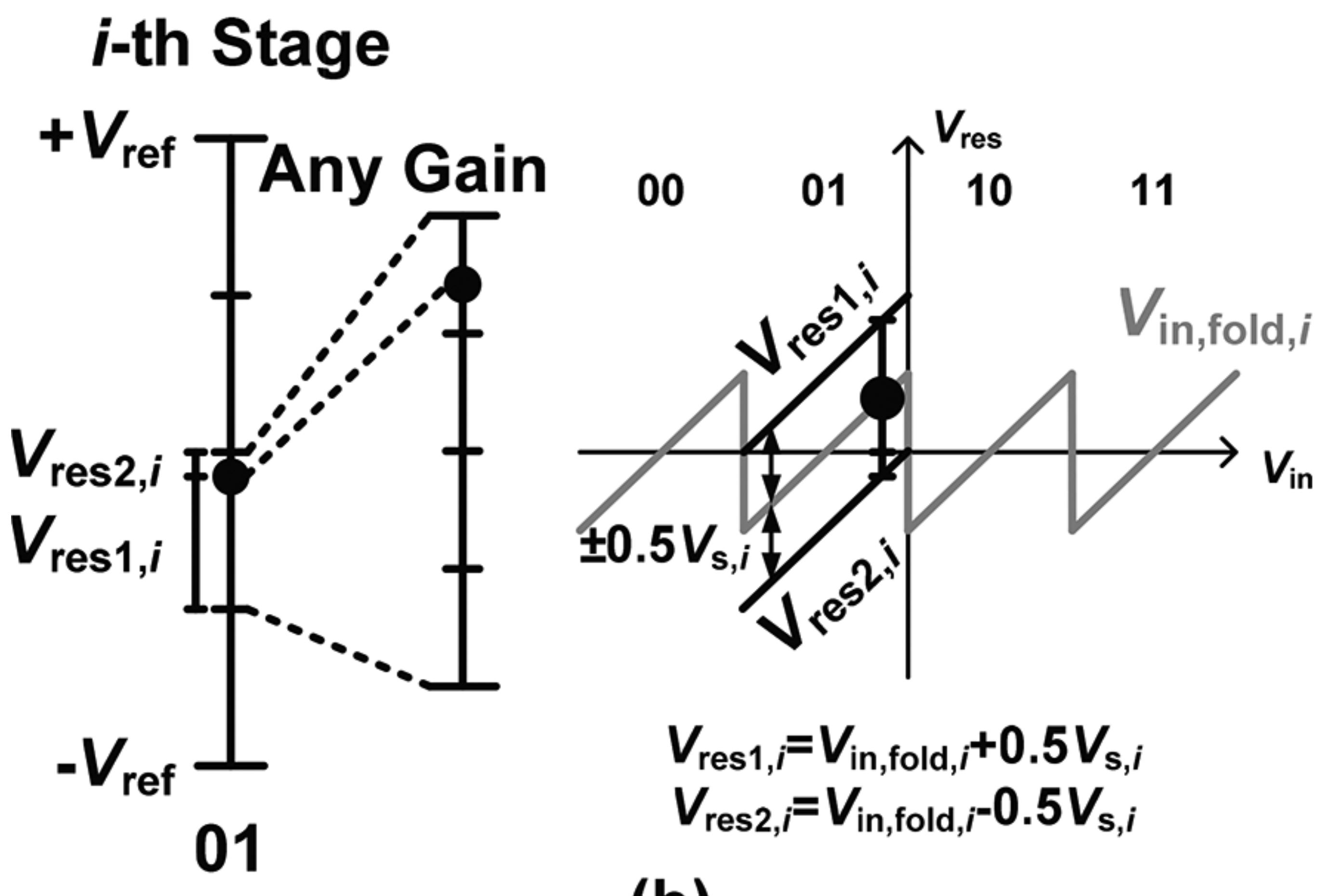
Uni. Bonn is working on different architectures: SAR (T65N, C. Kennedy) and FLASH (T28N, me).

Block diagram of our ADC



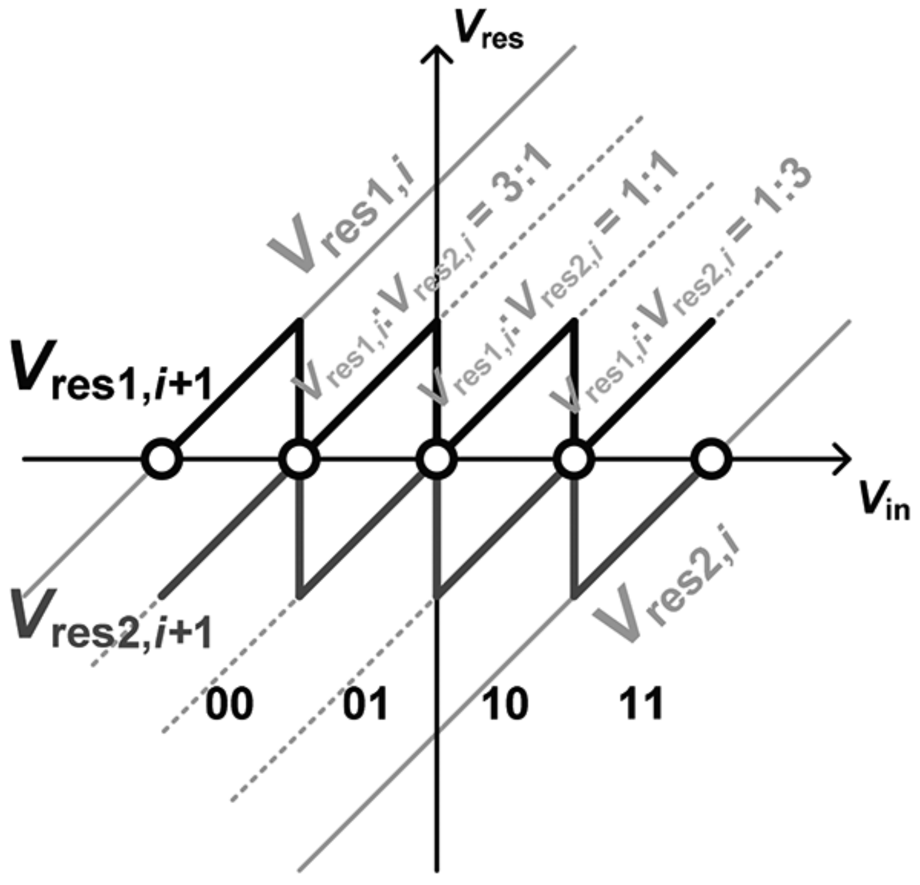
J. Lin et al.

Interpolated Pipeline



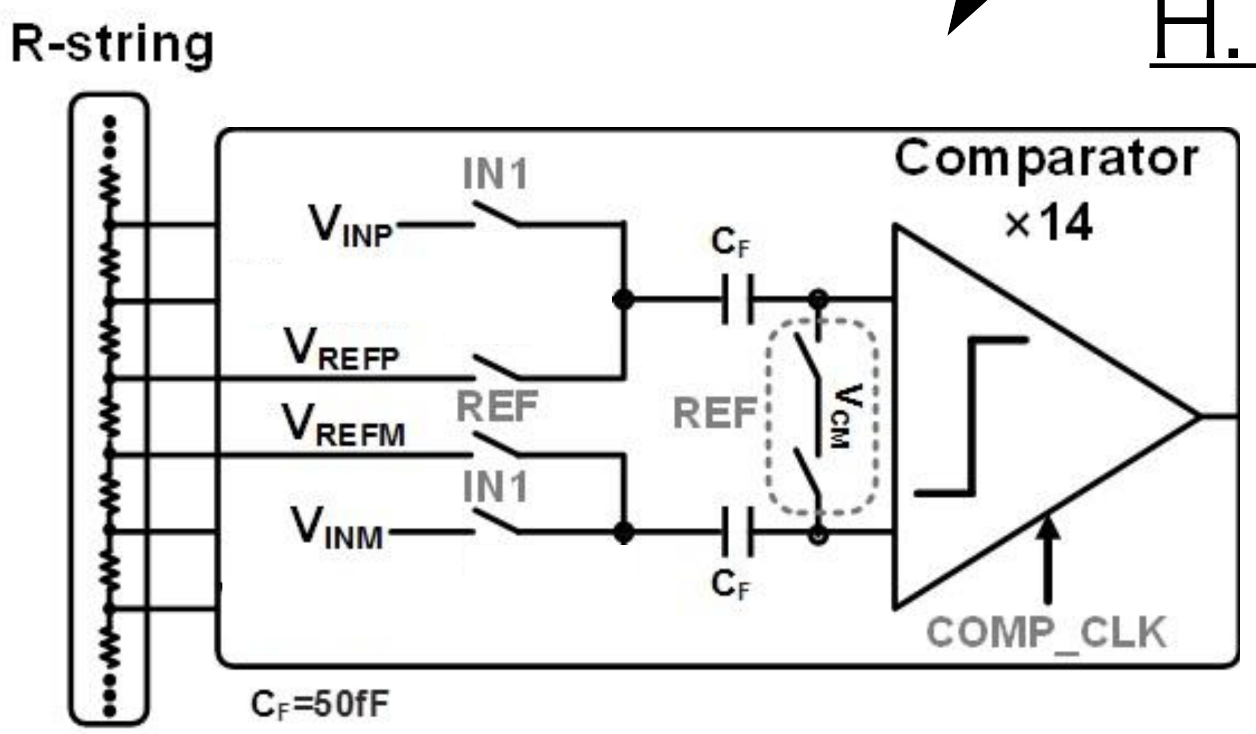
(b)

Interpolation (IP)



(c)

H. Jung et al.



- 10-bit: 4b FLASH + 3b FLASH (after residue calc.) + 3b FLASH (IP)
- VDD: 0.9 V in T28N CMOS, Target speed around 200 MS/s

Schematic simulation

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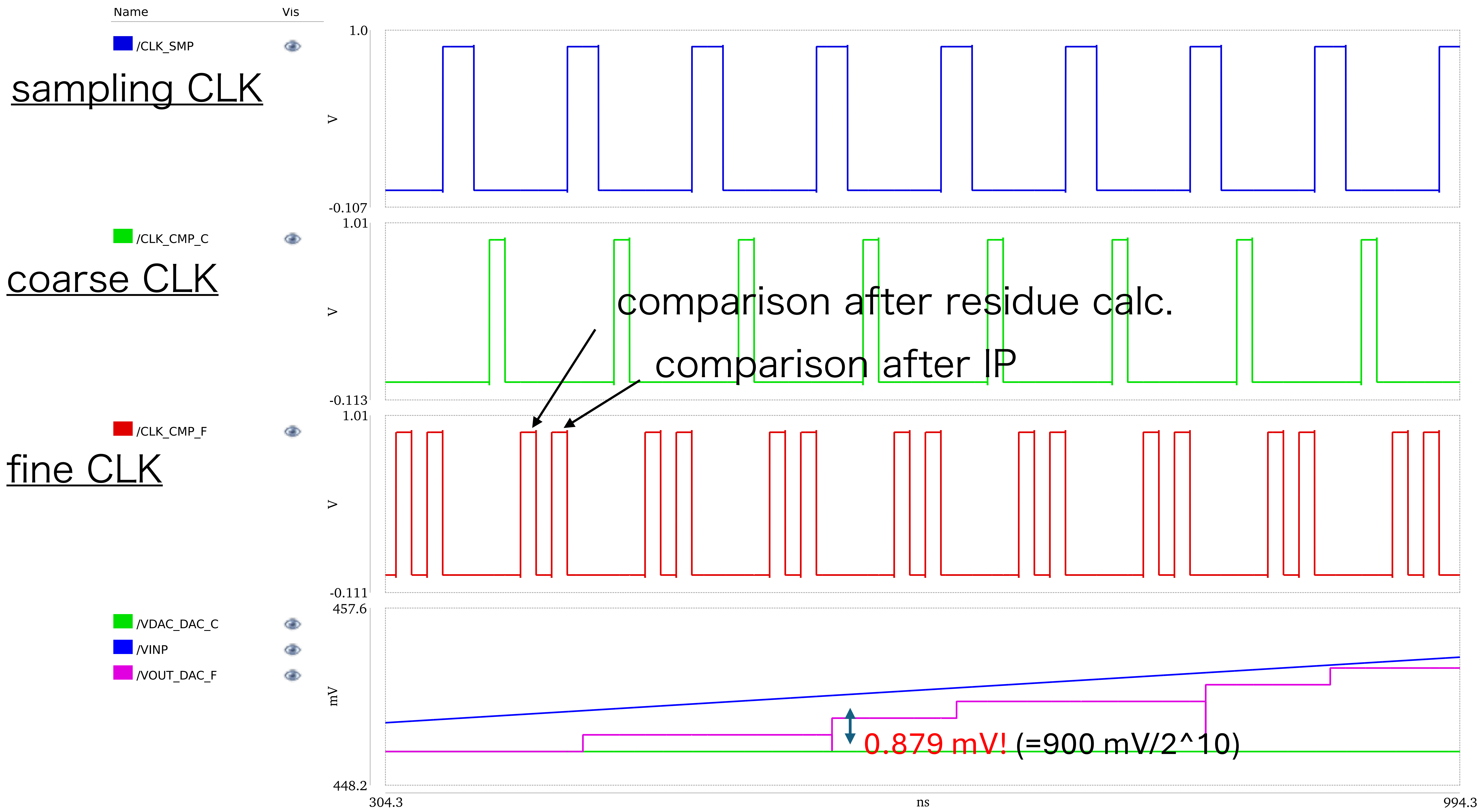
T28N

(1) 1st flash-ADC (**4 bits**) (2) calculate residue (3) 2nd flash-ADC (**3 bits**) (4) calculate residue (5) 2nd flash-ADC (**3 bits**)



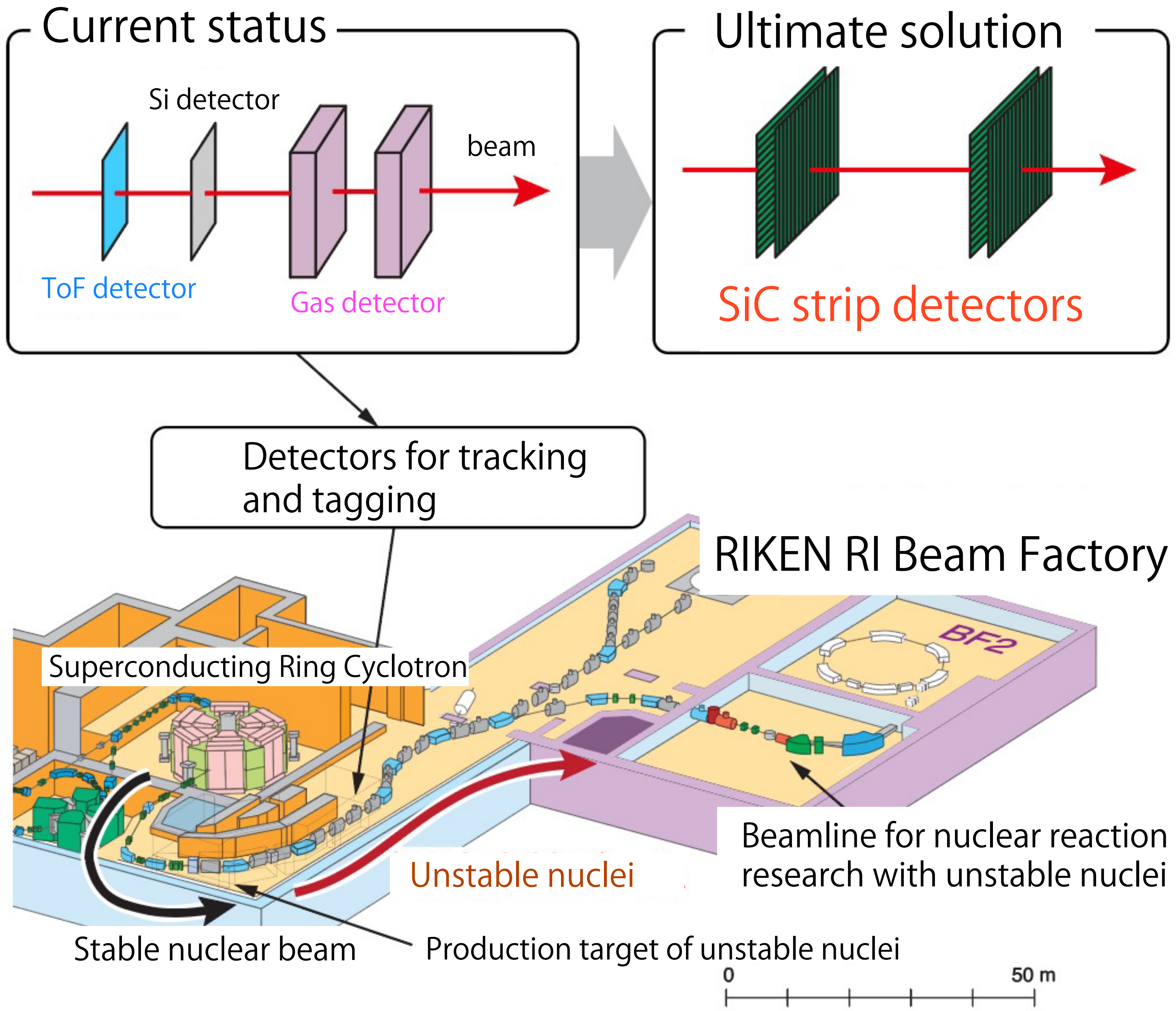
- Average power consumption: 690 uW (17.3 fJ/conv. step) @125MS/s, including control circuits.

will be submitted in Nov. 2026

Near future application

Combination of Fast ADC + SiC sensor for TOF detector

- Nuclear Physics Experiment, e.g., @RIKEN RI Beam Factory
- Replace conventional detectors with SiC strip sensor (timing+position)



Fukuda et al., NIM B, 317 (2013) 323-332

- Large signals in SiC sensor—> direct readout with fast ADC (timing + position)
- Interleaving approach (200 MS/s x 5 = 1GS/s)

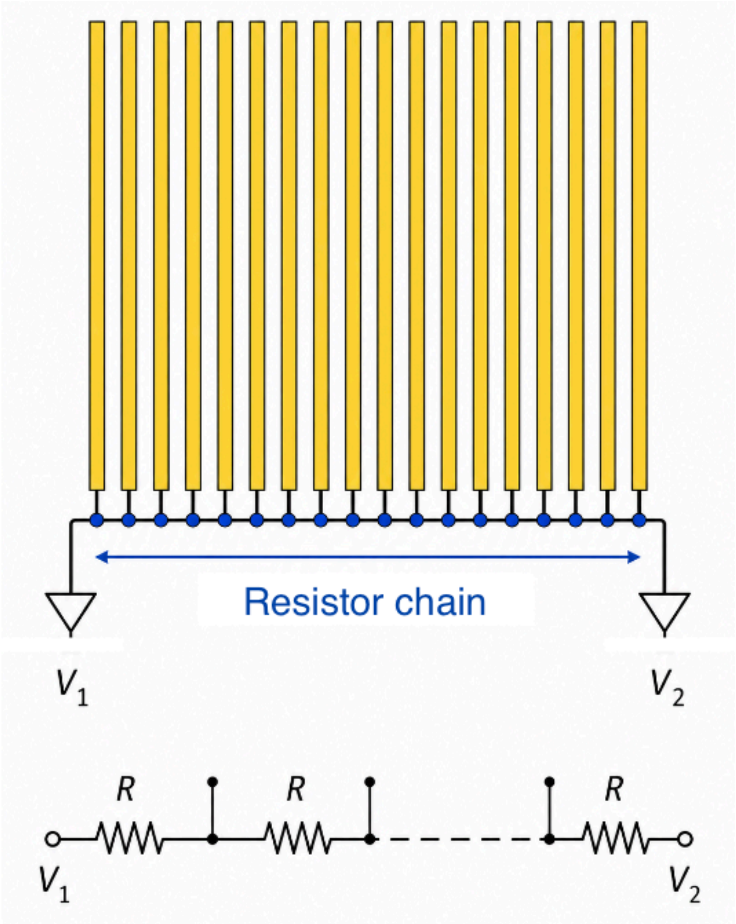
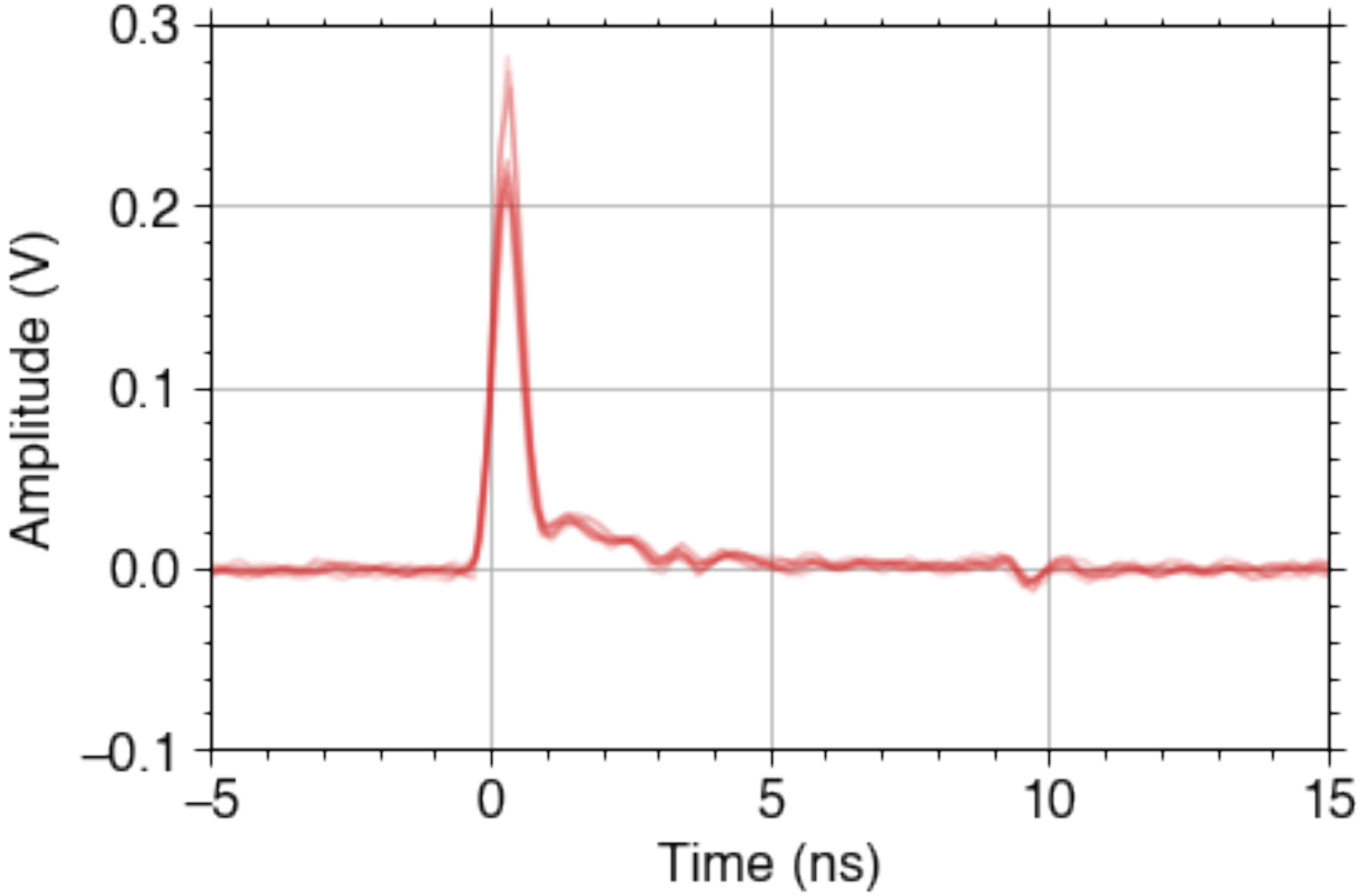


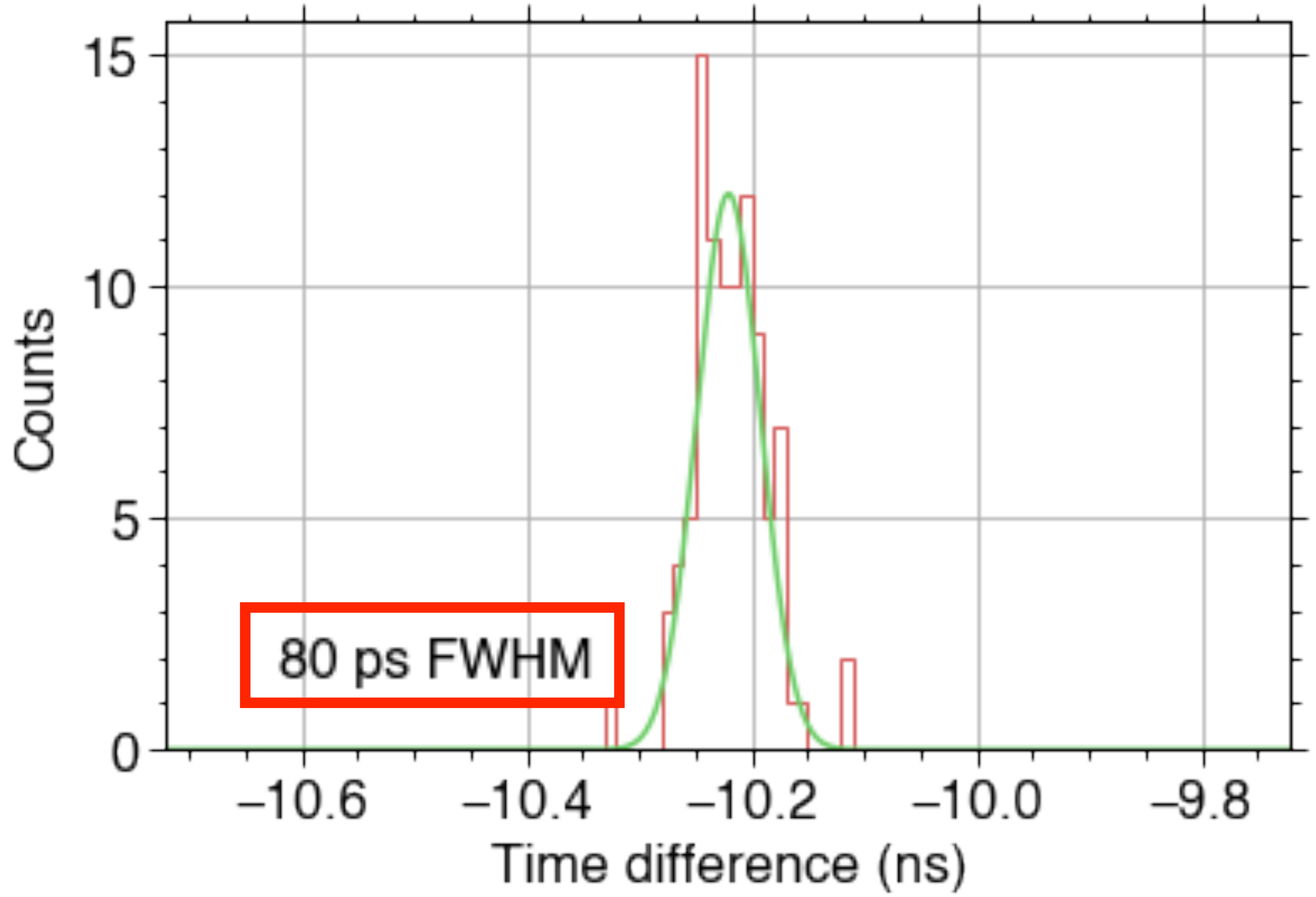
Figure 1: Example of the configuration of the detectors for beam measurement in the unstable nuclear experiment (RIKEN RIBF)

Timing performance (sensor side)

- Conducted beam test with 40Ar ions at 6 MeV/nucleon→ energy deposition of 240 MeV to SiC!
- Close to the time resolution of a polycrystalline diamond



Transient response of the SiC sensor without amplification, recorded with an oscilloscope.

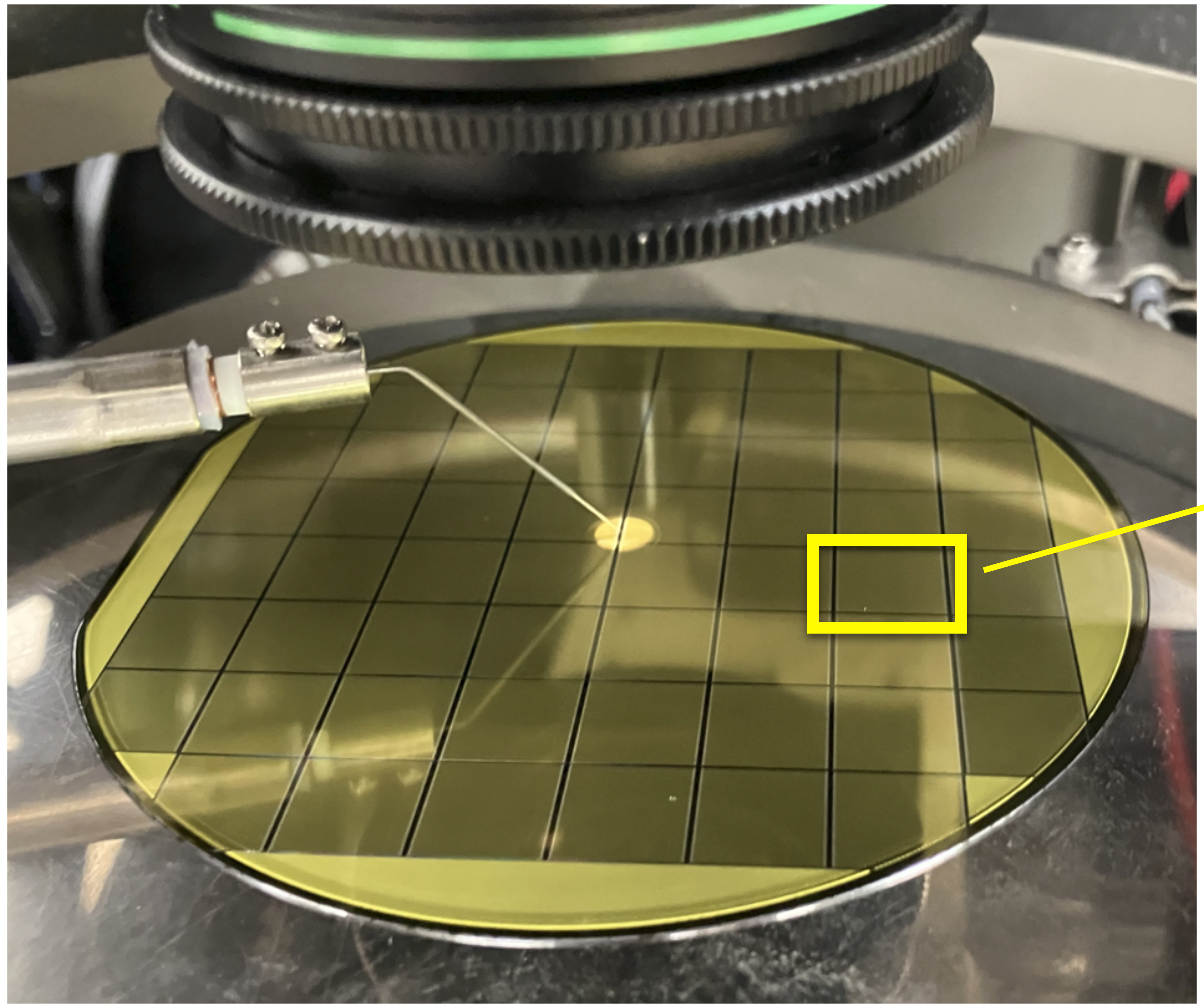


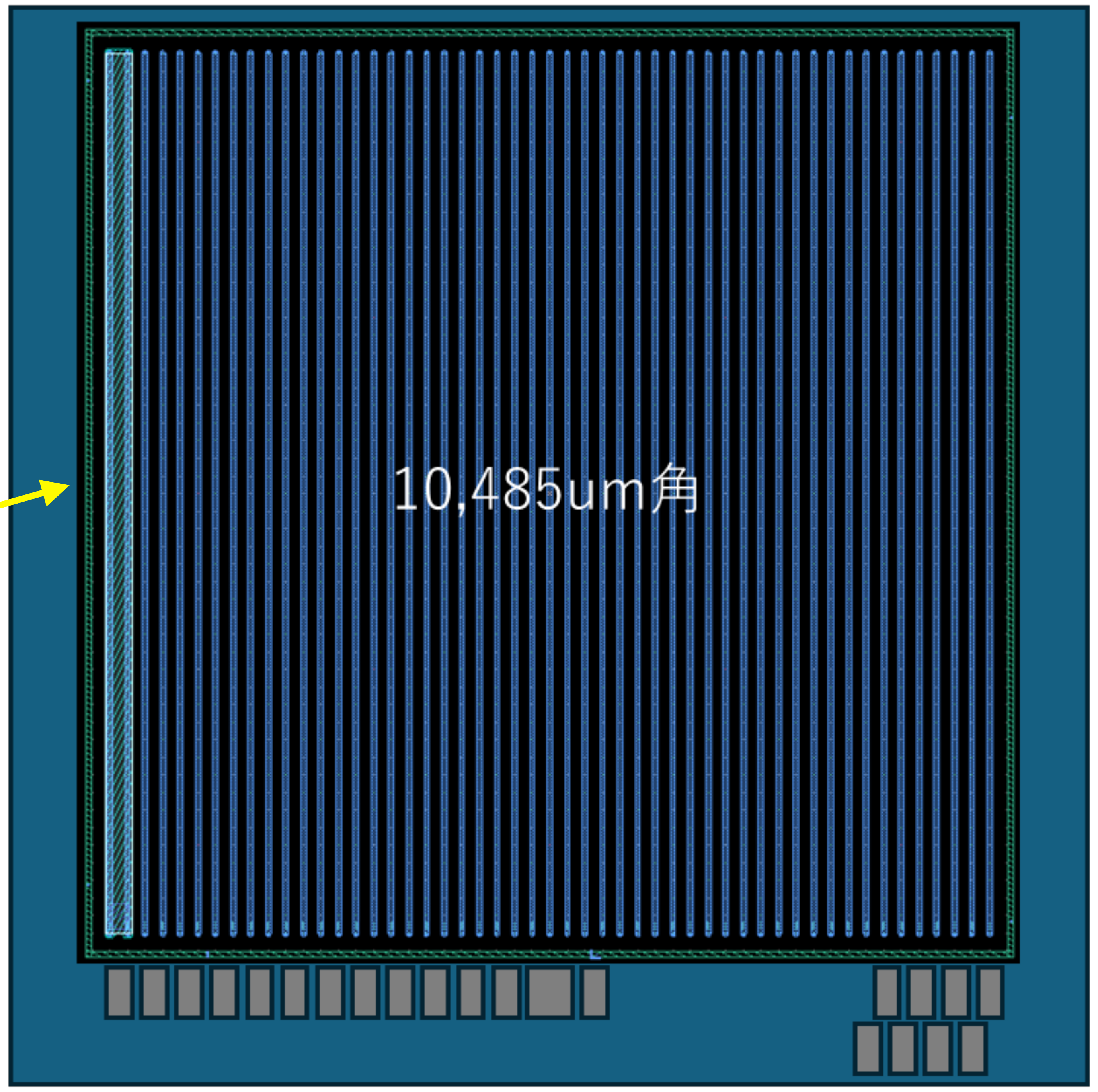
Time difference between the SiC and scintillator+PMT, after correcting the slewing effect.

Useful as TOF-start counter in heavy-ion nuclear experiments.

Sensor status

SiC-strip sensor (1 cm x 1 cm, 52 strips with 200 um pitch) under testing.

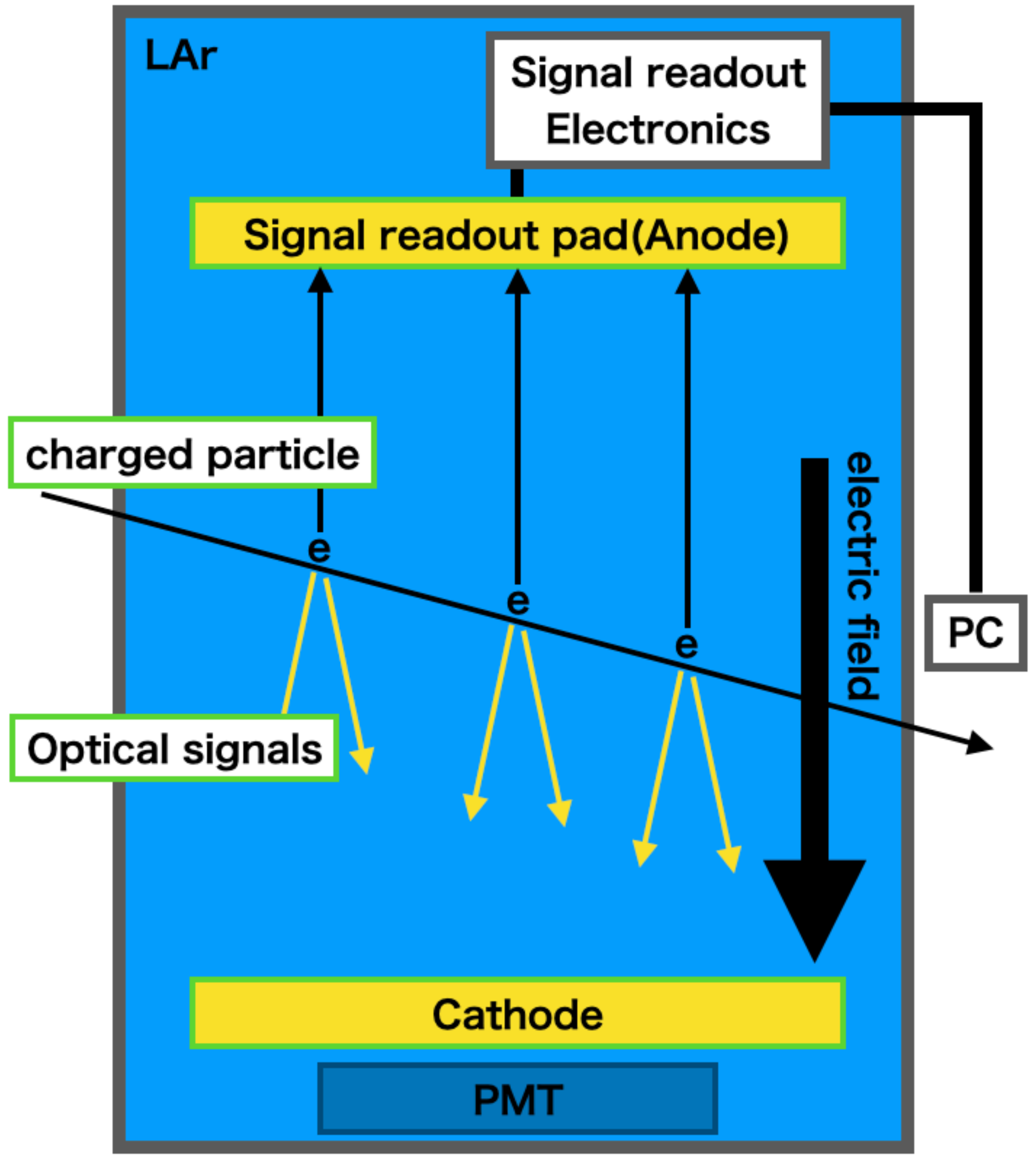




investigated in DFG Japan-Germany Collaboration program

Another interests: Cryogenic CMOS

- Cryogenic liquid-Ar (LAr) Time Projection Chamber
- 3D Tracking for neutrino studies (eg. hadronic interaction with neutrinos).
- Collaboration with KEK



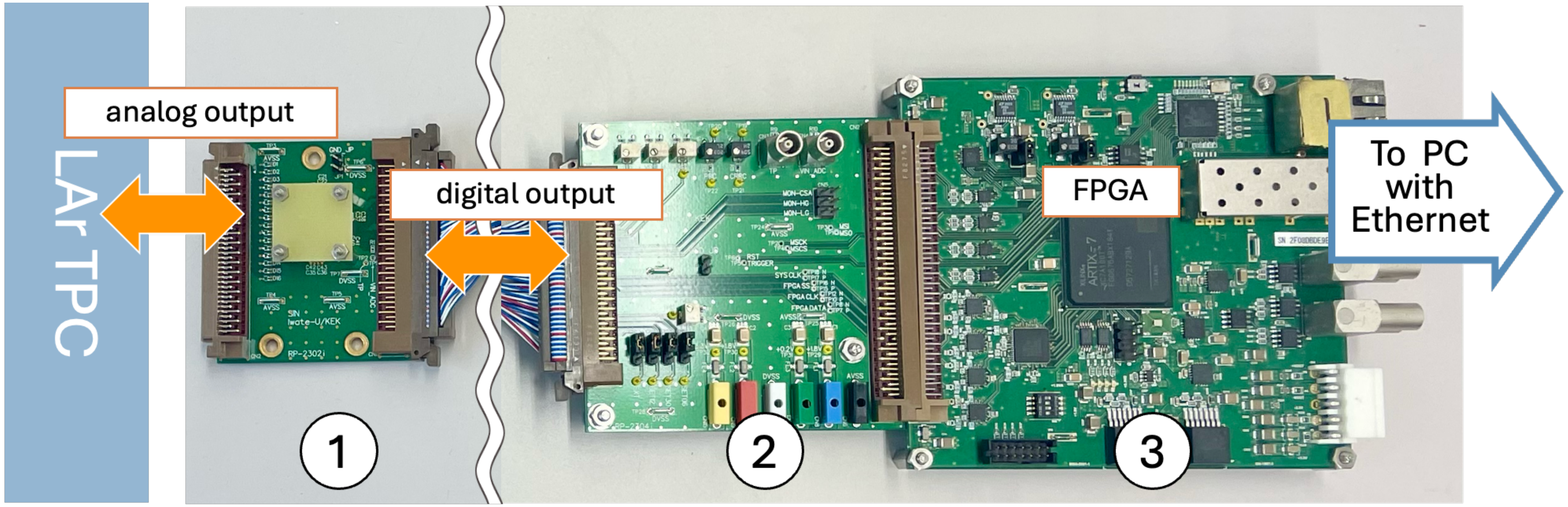
Liquid Ar TPC
(LAr-TPC)

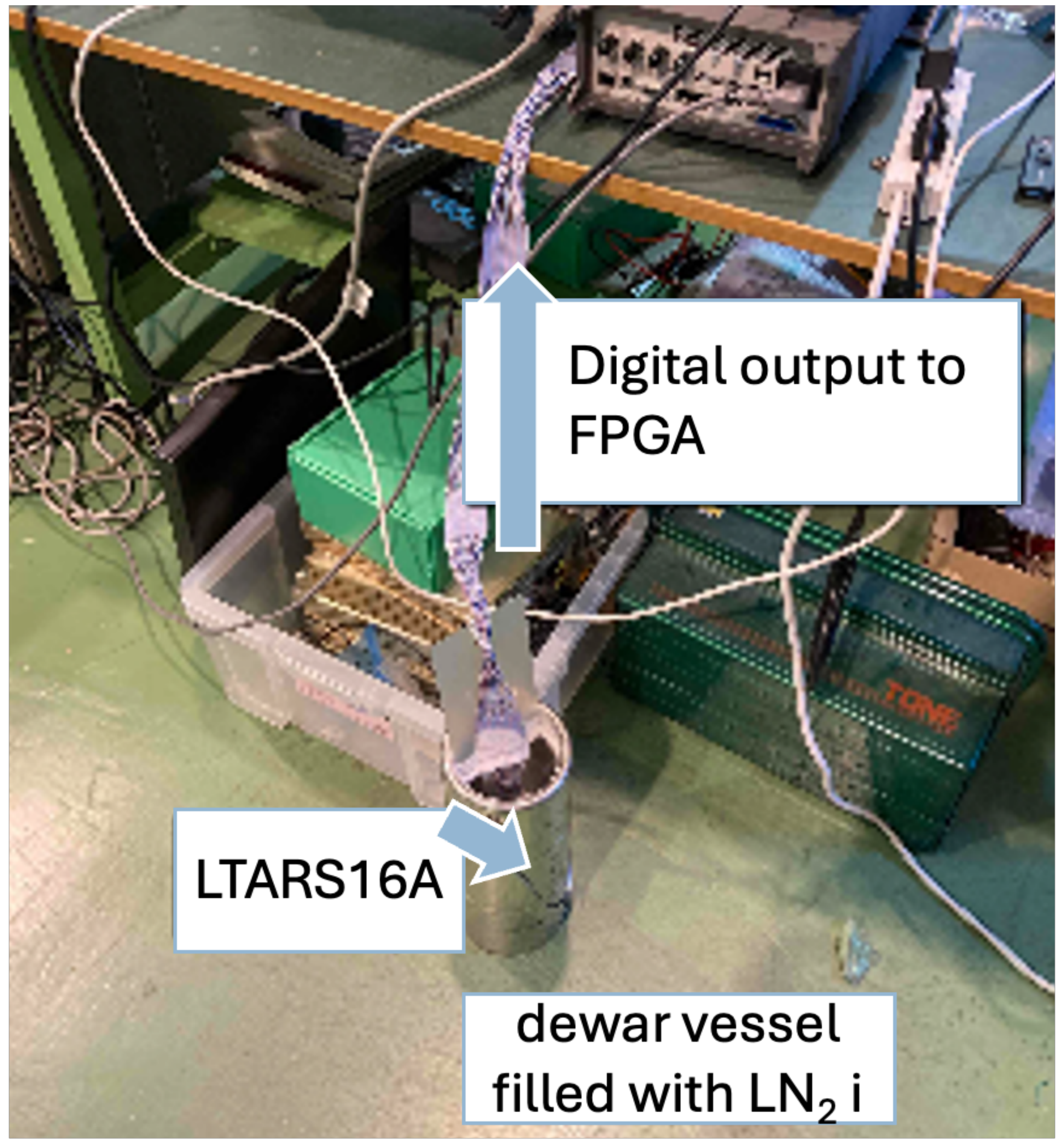
R&D goals of signal readout electronics

- high integration
  - multi-channel signal readout
- low power consumption
  - No bubbles in LAr to reduce HV discharge risk.
- High gain
- Wide dynamic range
  - To detect shower events with about 50 times larger than MIP signal.
- Low noise
  - To read out the MIP signal with the signal-to-noise ratio of higher than 10.
- stable operation in low temperature environment.

Cryogenic test setup

-T180N, 16 ch CSA+Shaper: 10mV/fC (high gain), 0.5mV/fC (low gain) + ADC+TX: 10 MS/s (8b)

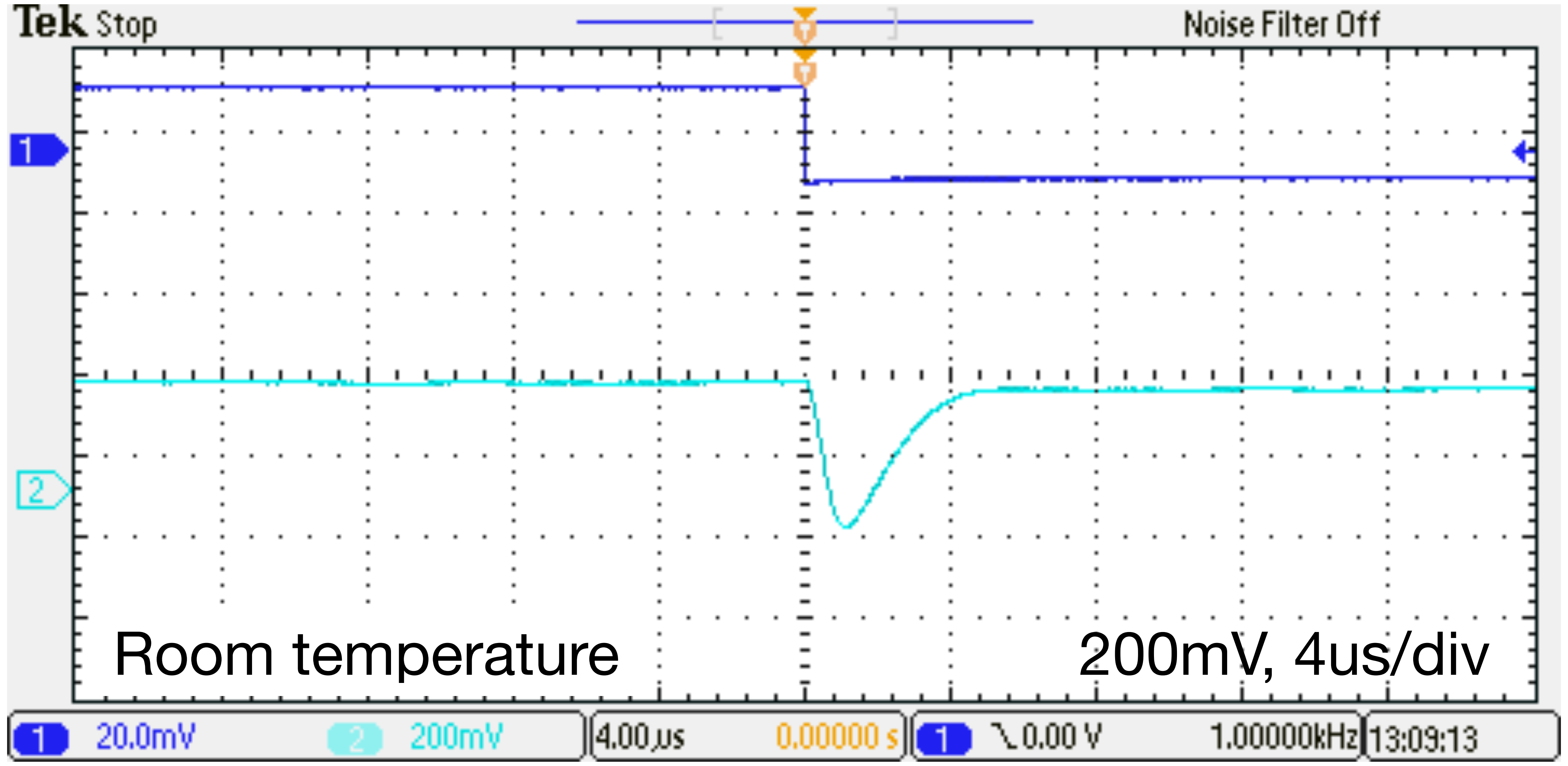


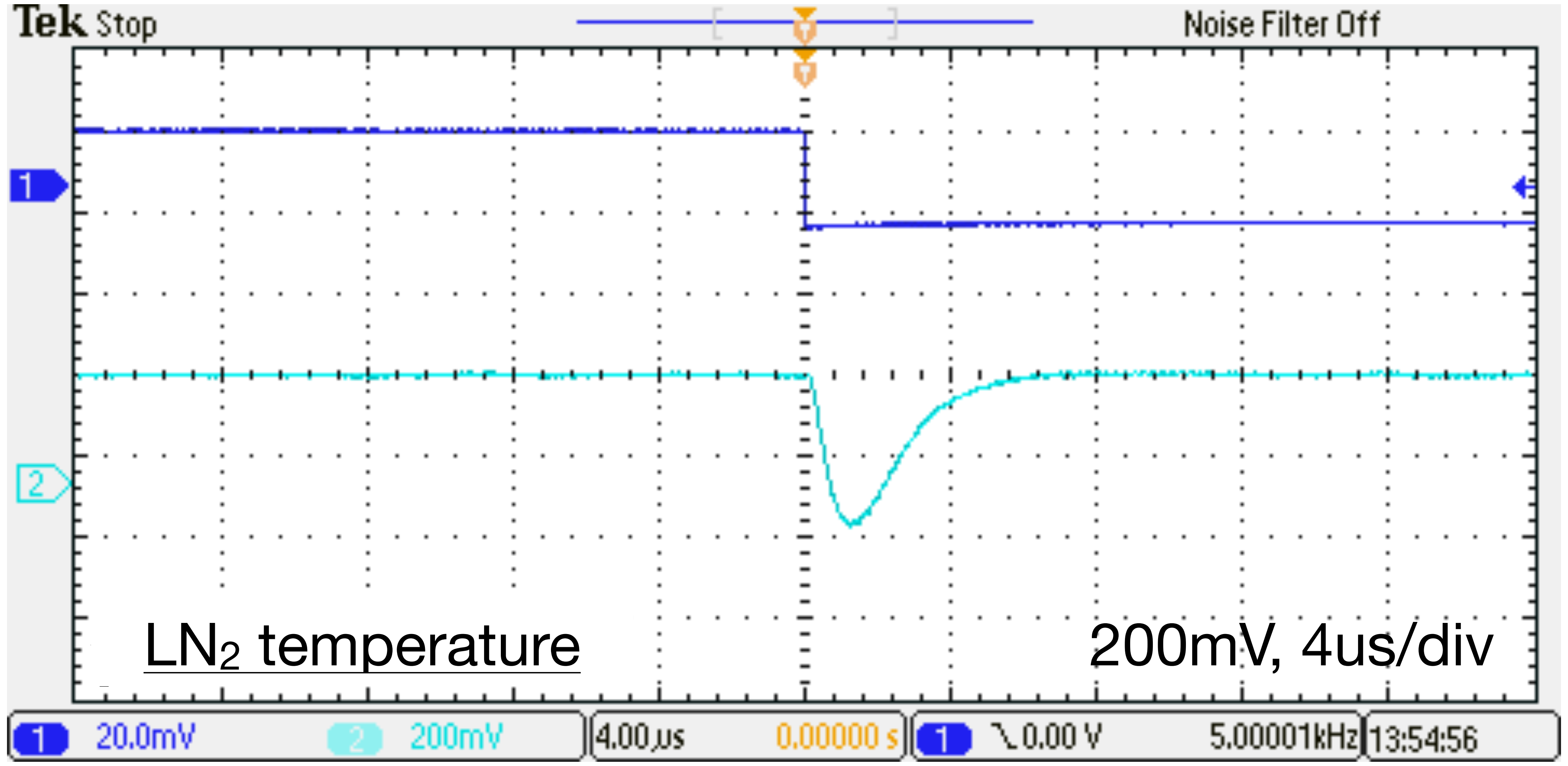


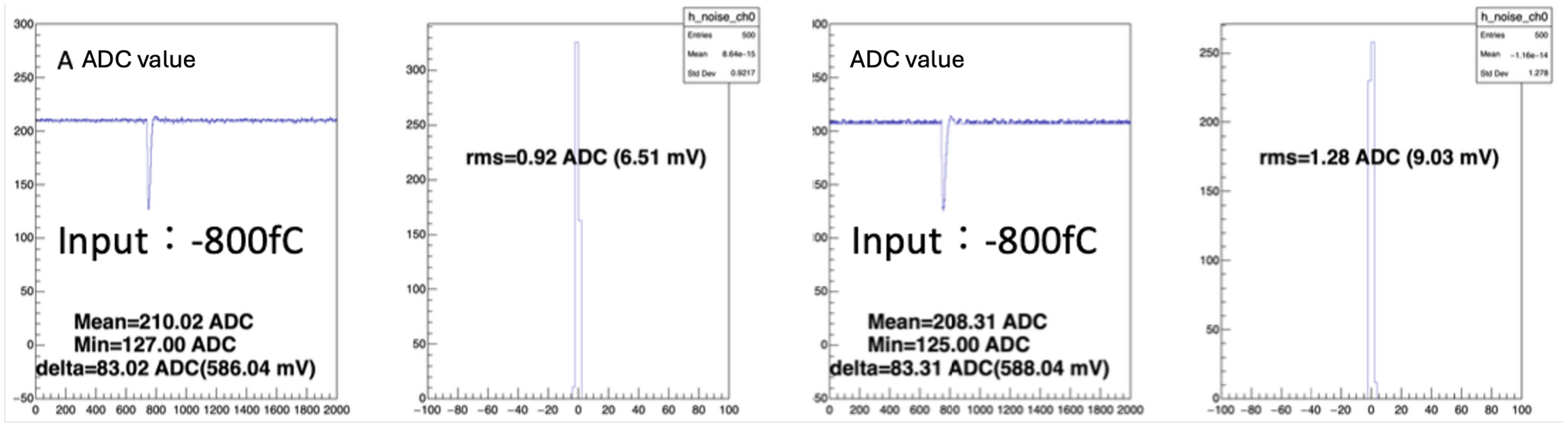
① ASIC board
② Power supplies and parameter tuning board
③ Custom FPGA board for DAQ

Direct immersion of the ASIC in a dewar vessel filled with LN_2 (77K).

Waveform comparison



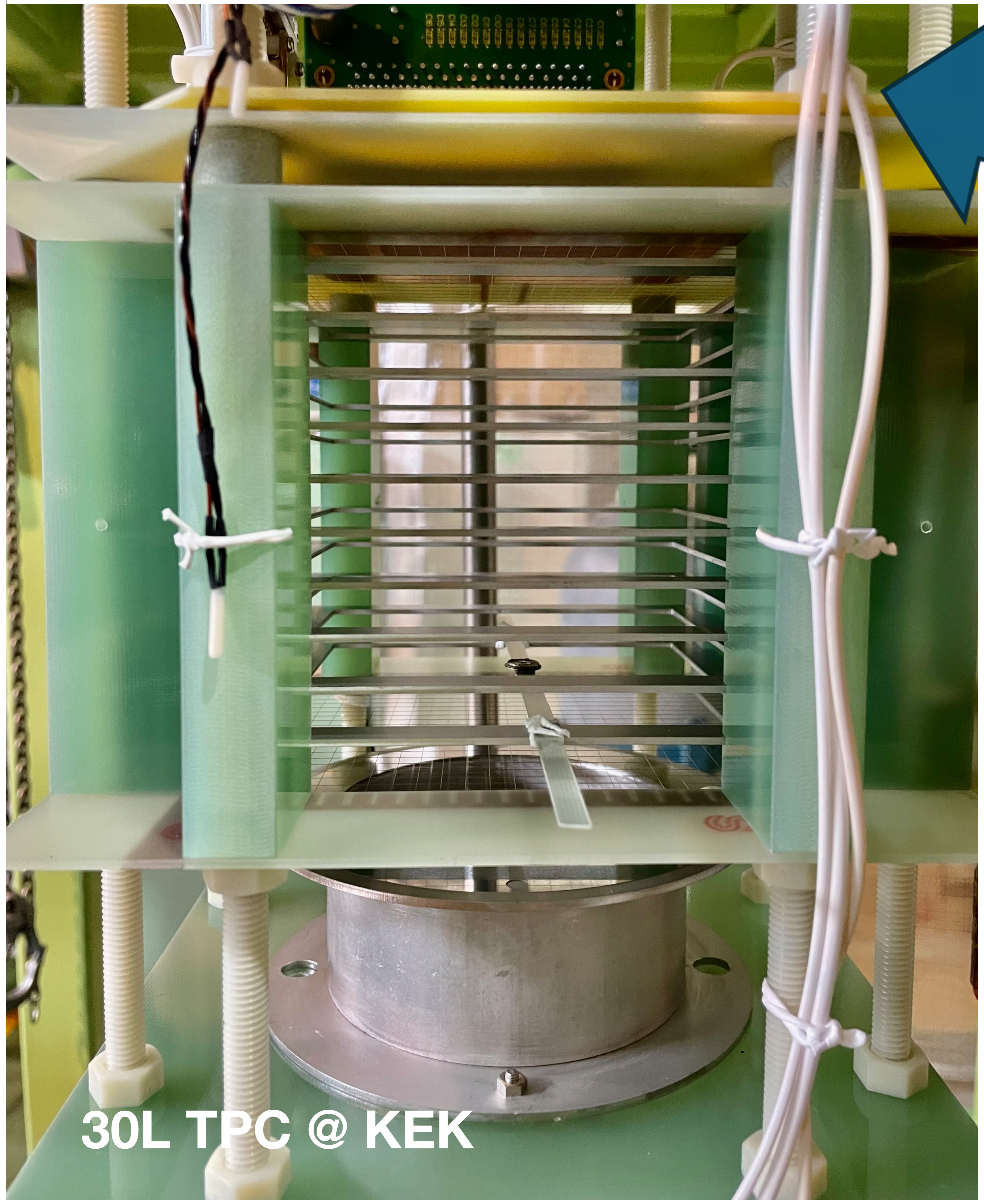




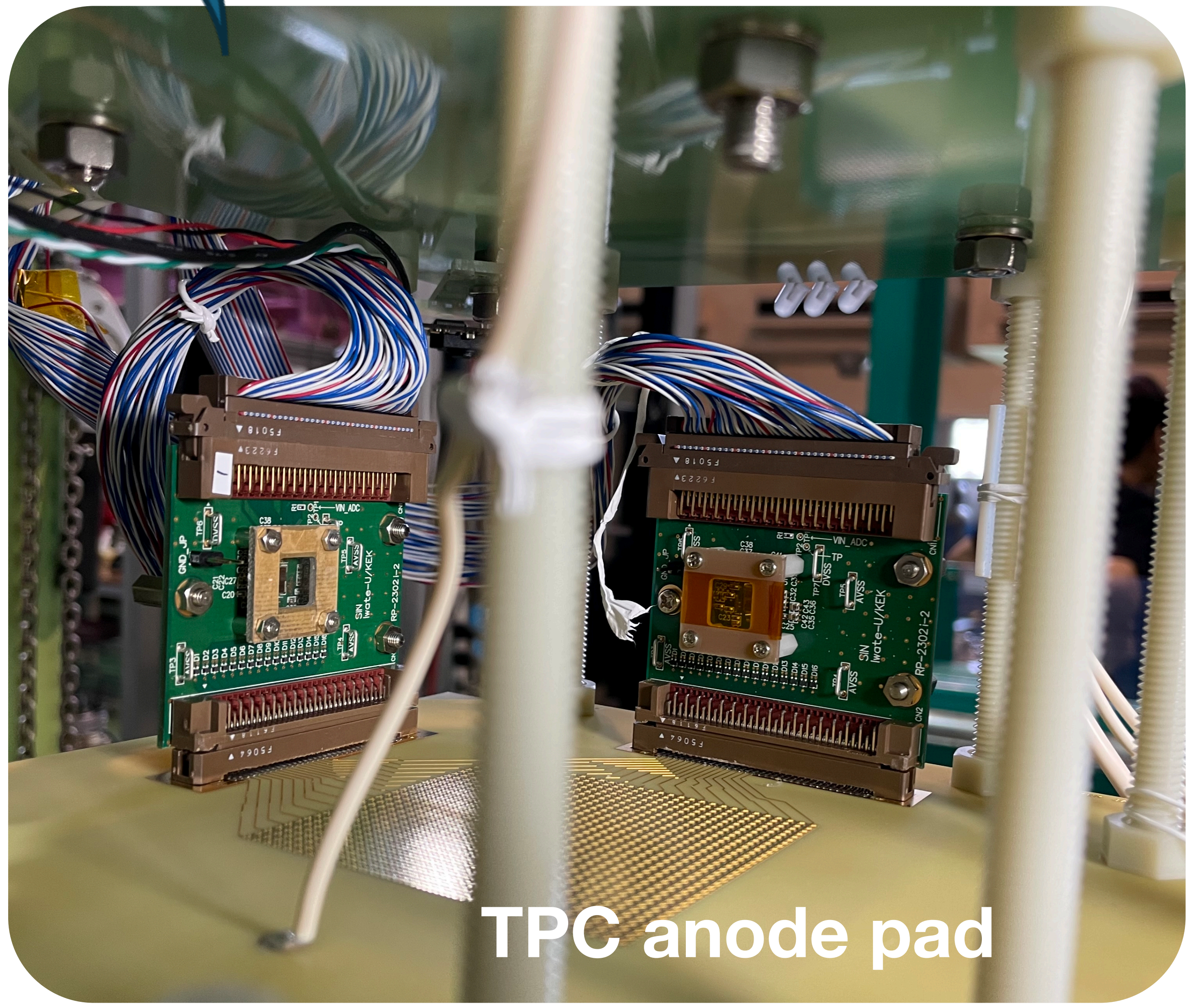
No clear degradation is found between room temperature and LN_2 temperature.

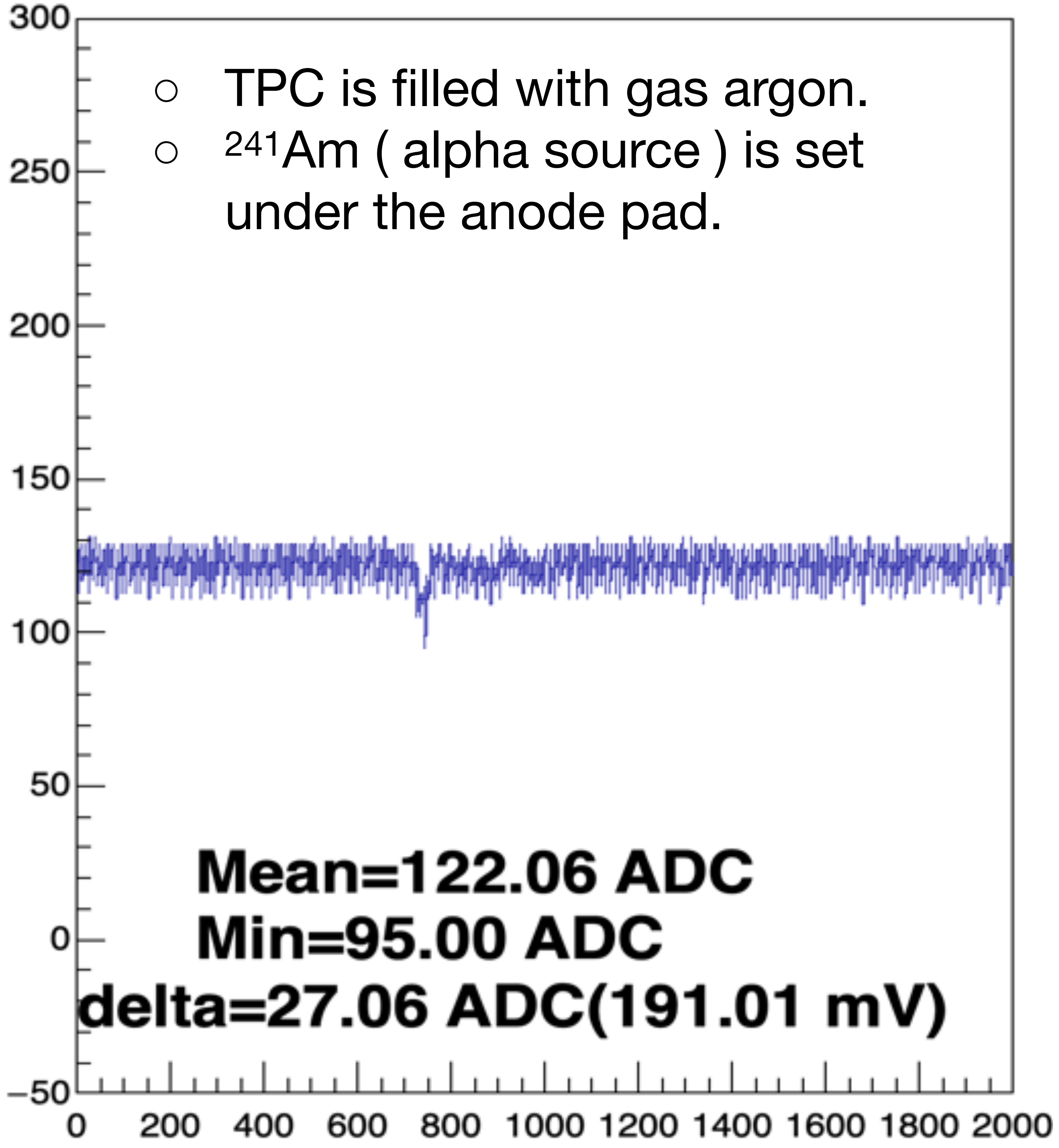
Testing with TPC

ASIC was mounted on 30L sized TPC.



2 ASIC boards for X Y directions are mounted directly above anode.





New chip submitted in Jan. 2026 including newly designed PLL.

Can we apply the cryogenic know-how to other experiments?

Thank you very much.