UNIVERSITÄT BONN FTD

Next-Generation Front End Readout Electronics for Particle Physics Experiments

Marie Skłodowska-Curie Postdoctoral Fellowship

Scientific Area: Particle Physics • Detector Instrumentation • Semiconductor Electronics

- ✓ *Development of advanced **front-end readout** electronics, focusing on innovative digitization systems for detector readout.*
- ✓ ***Broadly applicable to other fields**, including medical imaging and nuclear physics*

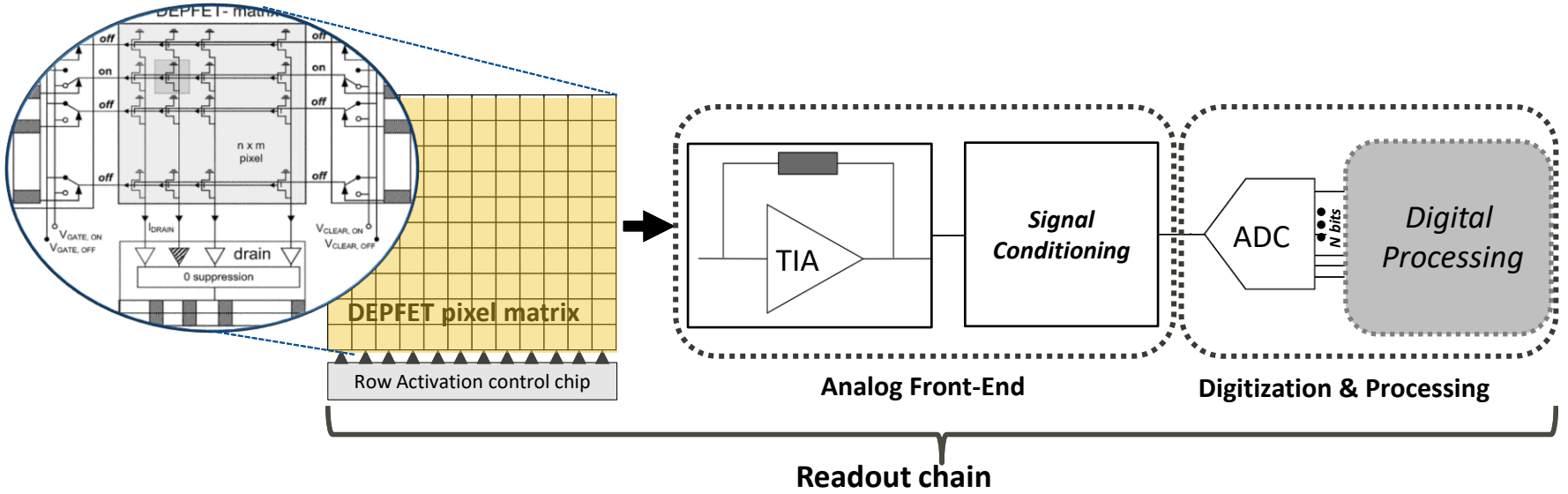
Funded by the European Union

NEXGENRE

FRONT-END READOUT ARCHITECTURE

→ The **DEPFET detector readout chain** is used as a **representative case study** to validate low-noise front-end architectures

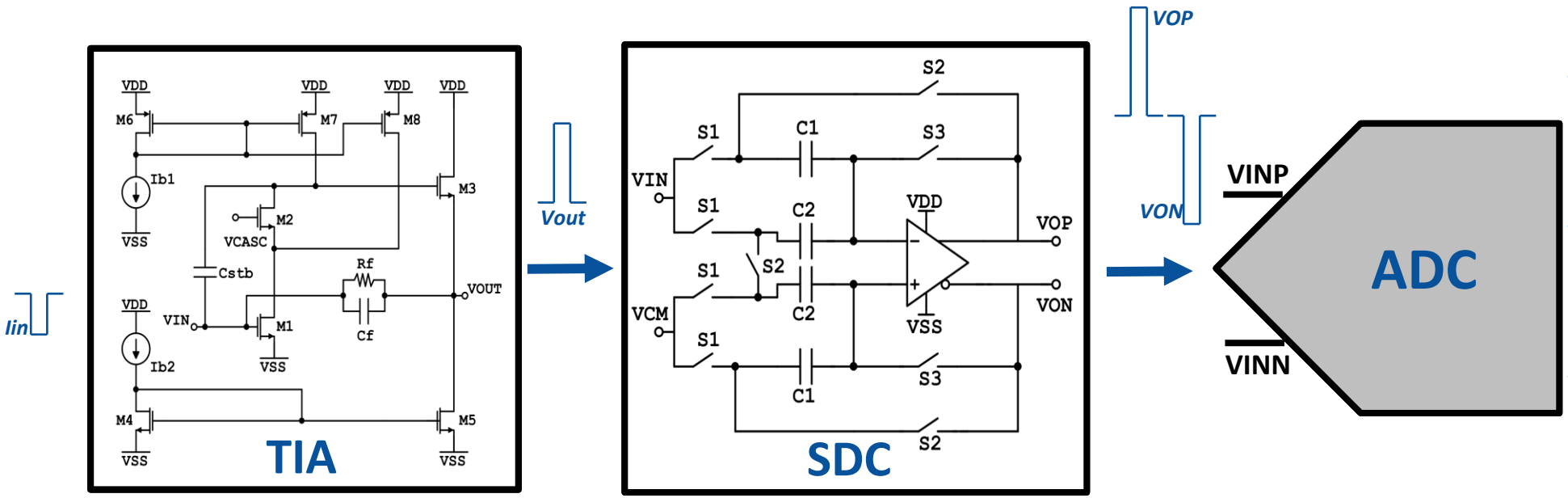
→ **Target**: upgrade of the DCDv4 chip



- **Concept:**
  - **Row-wise readout (rolling shutter):** pixels in one row of the DEPFET matrix are activated and read sequentially while other rows continue integrating charge.
  - **Analog front-end processing:** the TIA converts the small DEPFET drain current to a voltage. Subsequent analog circuitry conditions and manipulates the signal to provide an optimized input for the following processing stage.
  - **Digitization**: the ADC converts the processed analog signal into digital data for DAQ systems

READOUT DESIGN TARGETS

→ **TIA:** Low-noise, high-bandwidth current-to-voltage conversion under large detector capacitance with tight power constraints.
→ **SDC:** Compact low-noise single-ended-to-differential conversion within strict silicon area.
→ **ADC:** Low-power with sufficient resolution under tight area and power constraints.



$$V_{\text{out}} = -I_{\text{in}} \cdot R_f$$

- **Design Challenges:**
  - **Power vs. channel density:** a growing number of parallel channels must operate within strict power budgets.
  - **Power vs. noise:** preserving low noise performance while operating at very low power and increasing readout speed.
  - **Integration constraints:** shrinking silicon area per channel while integrating more functionality on-chip.
  - **Input capacitance vs. noise:** larger input capacitances degrade noise performance and limit achievable resolution.

FUTURE WORK AND APPLICATION EXPANSION

→ Modular readout chain enables adaptation to different detector systems

TIA

- Programmable **gain / feedback impedance** for different detector signals
- **Adjustable bandwidth** to support different shaping times and event rates
- **Bias tuning** for noise-power optimization across operating modes

SDC

- Configurable **gain and output swing f**or different ADC input ranges
- **Tunable sampling r**ate and **capacitor sizing** for noise-speed trade-offs
- Adaptable **common-mode level** for different digitizers

ADC

- Configurable **sampling speed and resolution** depending on throughput needs
- Adjustable **input range and reference settings** for different detector systems
- **Scalable power modes** for high-rate vs low-power operation

Complementary Expertise for Collaborative Projects:

→ Background in **energy harvesting circuits and power management systems**, including low-power and autonomous operation design

Power Management ICs
- DC-DC converters (inductive and fully integrated / switched-capacitor)
- Low-dropout regulators (LDOs)
- Bandgap references (BGRs)

Analog / Sensor Interfaces
- Voltage and current sensing circuits

Protection & Robustness
- Over-voltage and over-current protection circuits
- Power monitoring and safety supervision

This project has received funding from the European Union's Horizon 2024 Research and Innovation programme under the Marie-Sklodowska-Curie grant agreement No.101209036 (NexGenRE).