Integrated Computing Architectures at FZJ

18.05.2026 | André Zambanini

Jülich Forschungszentrum | Integrated Computing Architectures ICA

Integrated Computing Architectures

Semiconductors enable Future Computing architectures

→ High integration, VLSI scalability

Quantum Computing

Neuromorphic Computing

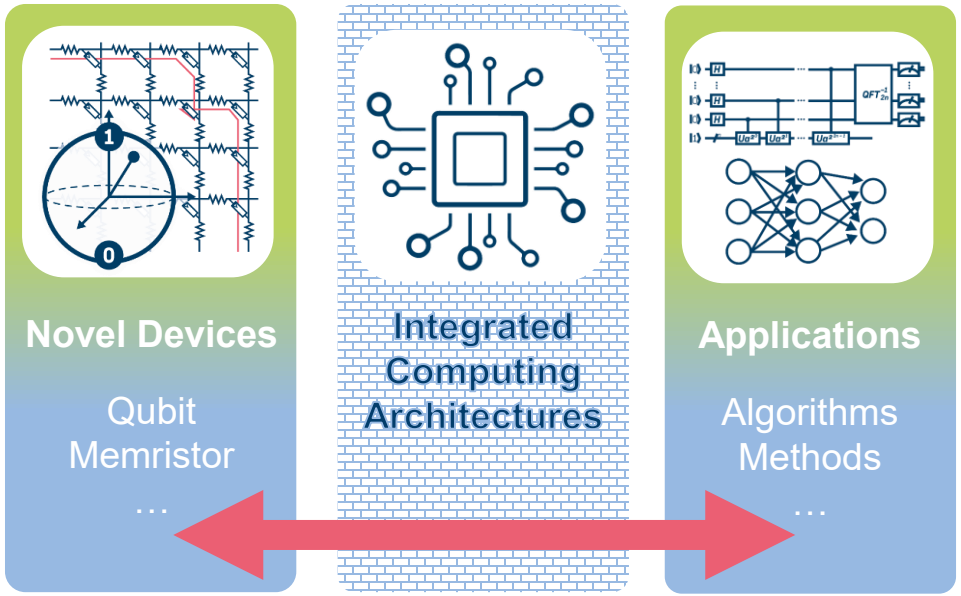
System integration of memristors, qubits, etc.

→ Algorithms, hardware and physics co-design

System modeling of hardware implementations

→ Application requirements and error mitigation / correction

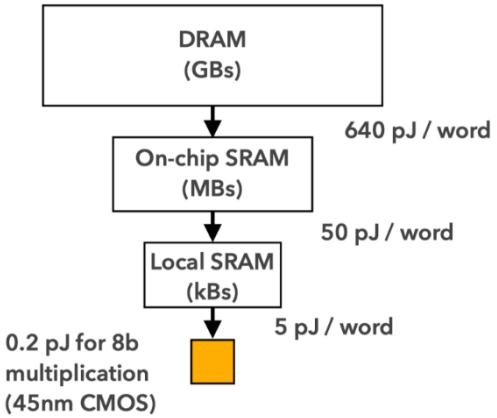
~60 people (staff, post-docs, PhDs)



JÜLICH Forschungszentrum | Integrated Computing Architectures ICA

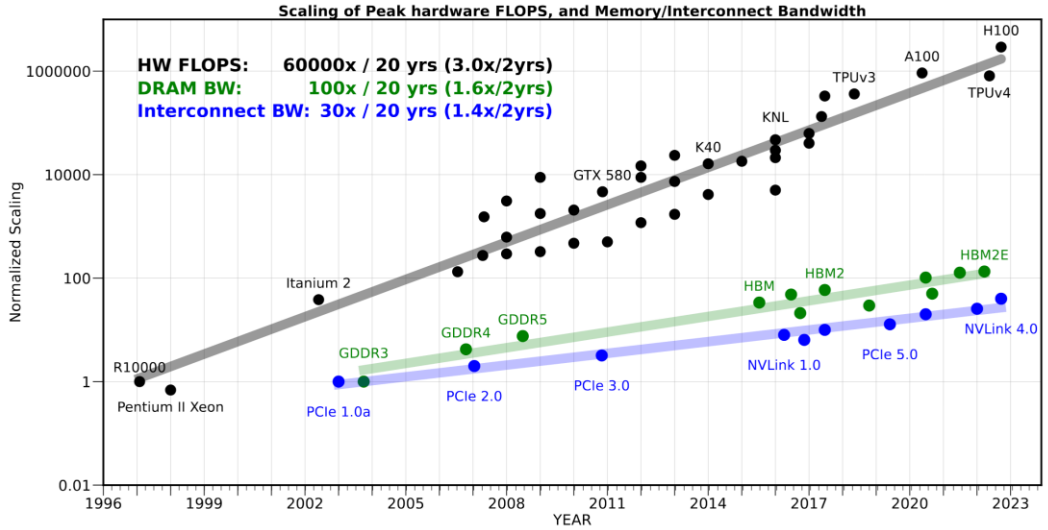
Performance Scaling Limited by Memory?

Energy Footprint of Computing vs. Data Movement



Horowitz, M., "Computing's Energy Problem (and what we can do about it)", IEEE ISSCC, 2014

Scaling of Computing vs. Memory Bandwidth



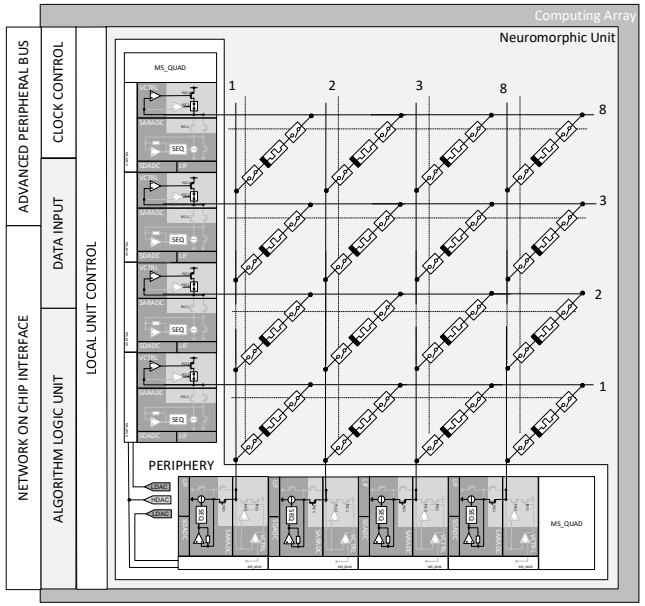
Gholami A, *et al*. „AI and Memory Wall", arXiv (2024). [https://arxiv.org/abs/2403.14123]

How to overcome the memory limitations?

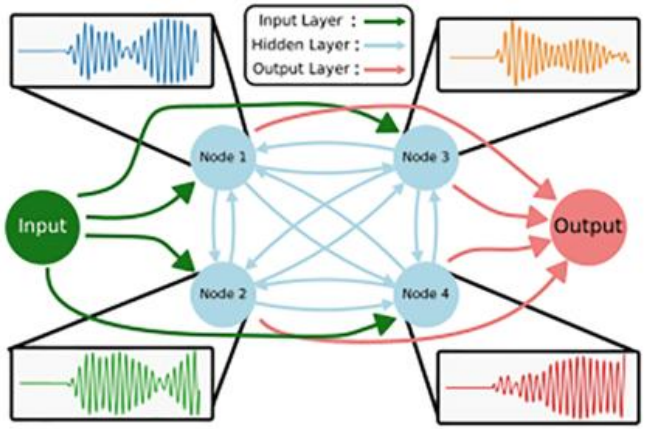
BIOLOGICAL INSPIRATION:
Memory Integral Part of the Computing

NC!

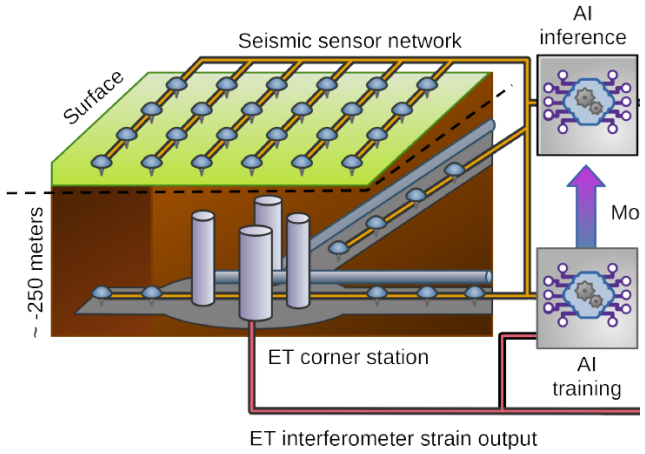
Focus Topics in Neuromorphic Computing



Crossbar Arrays

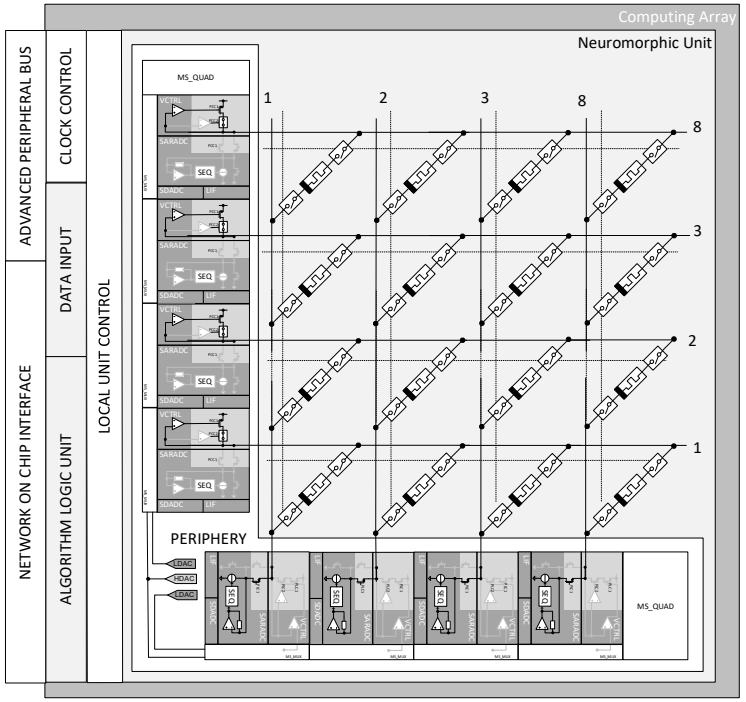


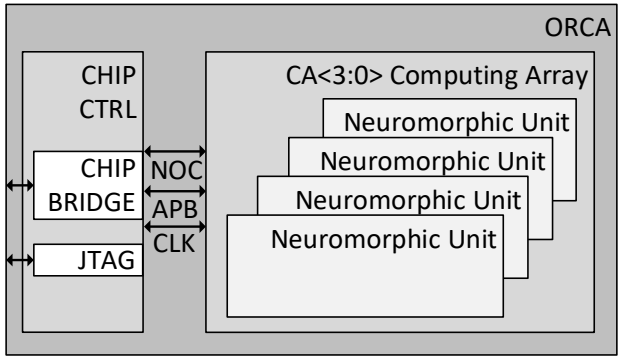
Oscillatory Neural Networks



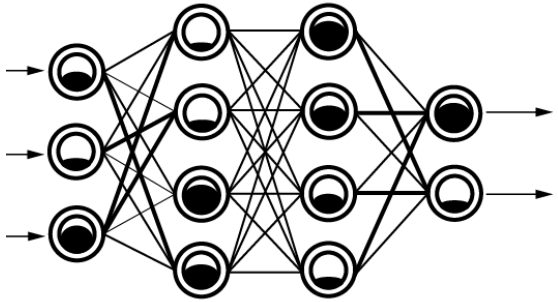
Edge AI Applications

CROSSBAR ARRAYS USED FOR COMPUTING IN MEMORY





ORCA / D1: Integrated Memristors



Neural Network

Crossbar arrays are the basis for computing in memory (CIM)

- *Memristors:* non-volatile, high-density
- Alternative nodes possible

System design important (network on chip, analog interconnects)

Crossbar Arrays | Oscillatory Neural Networks | Edge AI Applications

NEUROTEC II: DEMONSTRATOR SYSTEM

Platform for Multiple Bio-Inspired Computing Paradigms

Versatile Demonstration Vehicle

4 programmable memristive crossbar arrays with

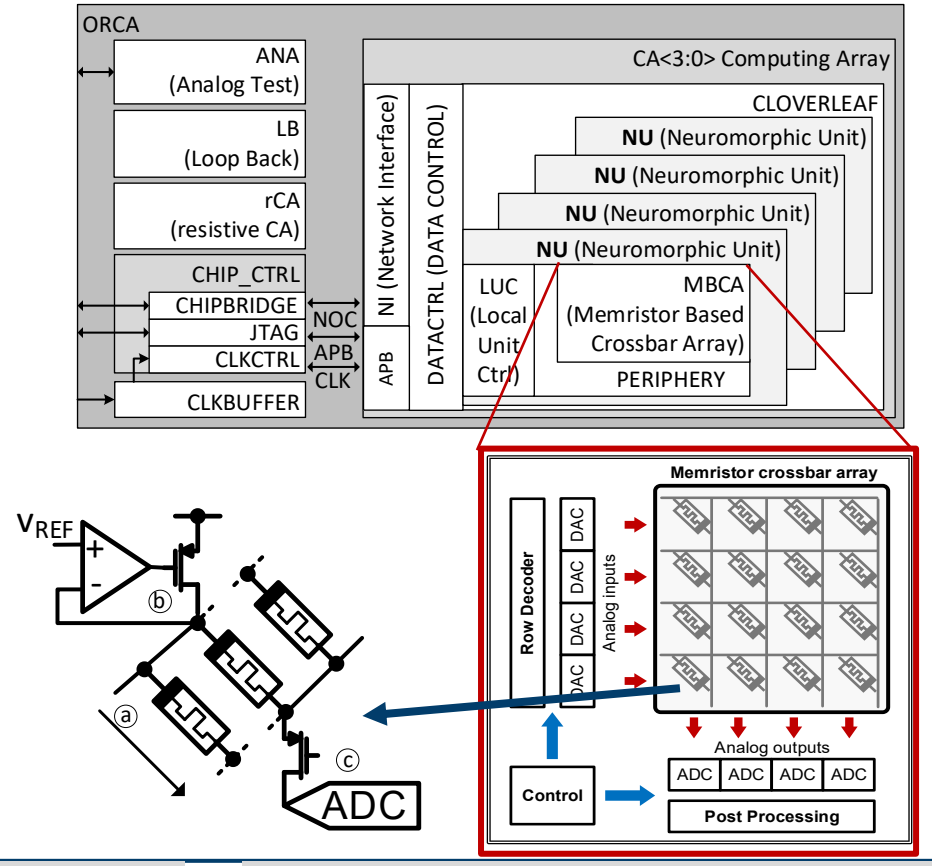
- > **65.000 memristors** co-integrated (post-processing)
- **2560 8-bit ADC** and **4-bit DAC** integrated
- Automatic memristor control enabled

Flexible Interfaces

- Network on Chip (NoC)
- Chipbridge for direct NoC access
- Standard JTAG programming interface

→ **Different bio-inspired computing paradigms**

Concept developed in close collaboration within FZJ



Crossbar Arrays | Oscillatory Neural Networks | Edge AI Applications

NEUROTEC II: MEMRISTOR INTEGRATION

NEUROTEC

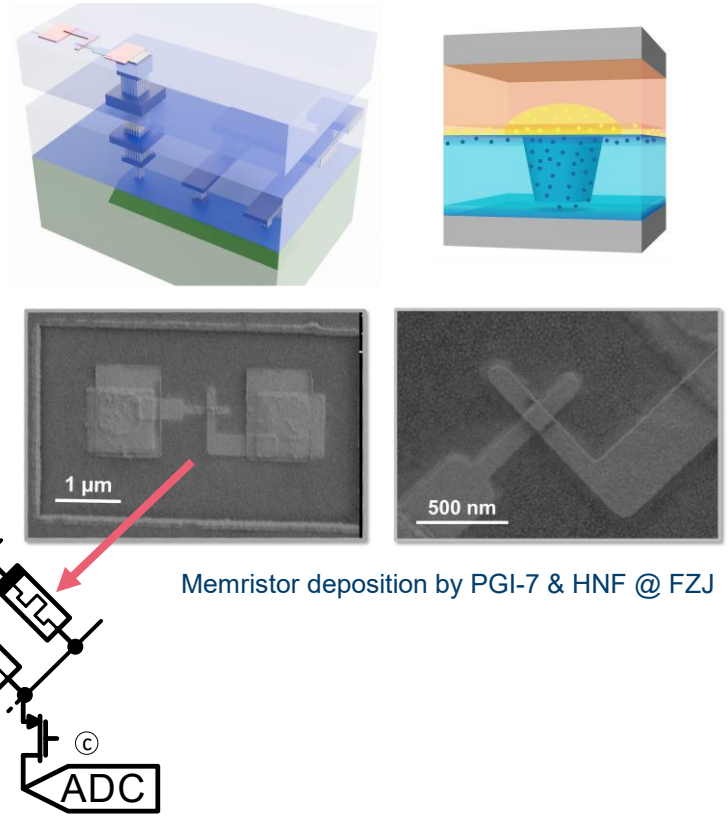
Federal Ministry of Research, Technology and Space

State-of-the-Art Memristor Integration

- Fab-level RRAM: binary memory with controller
  → no access to the device
- Research-level: memristor off-chip, wirebonding at best
  → scale-up issues and strong parasitic effects

Goal: True Memristor Integration into/onto CMOS

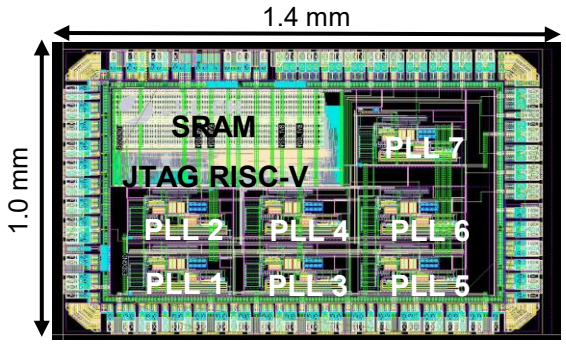
- Robust 180 nm CMOS for prove of principle
- Modern 28 nm CMOS for scalable and high-performance
  - Issues: full wafer (too)expensive, MPW chiplets small and fully processed, copper complicated in clean rooms, …
    → tricky integration, but doable
- Outlook: integration into BEOL on 22 nm FD-SOI planned



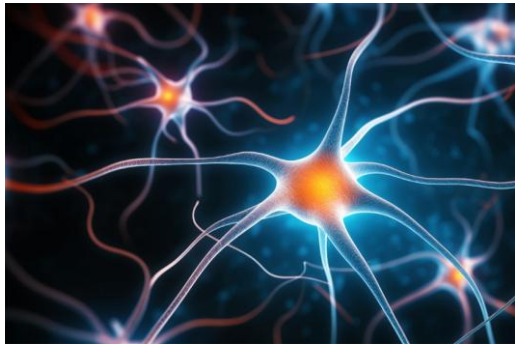
Memristor deposition by PGI-7 & HNF @ FZJ

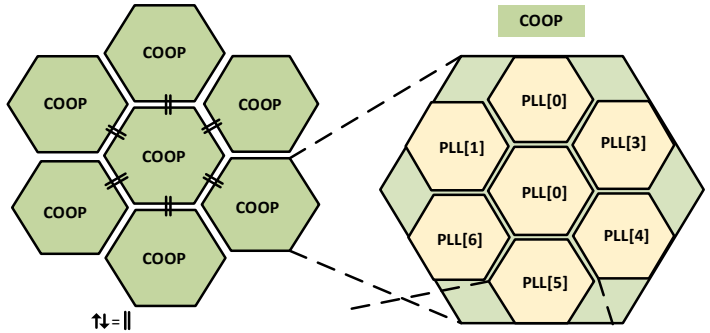
Crossbar Arrays | Oscillatory Neural Networks | Edge AI Applications

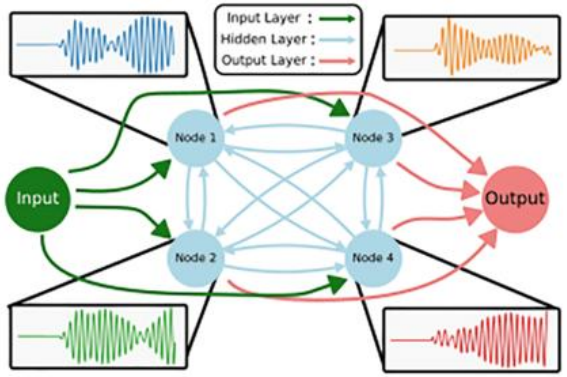
The Magic Lies in the Coupling



Chip Layout







Brain-inspired computing: processing based on overlay of oscillations

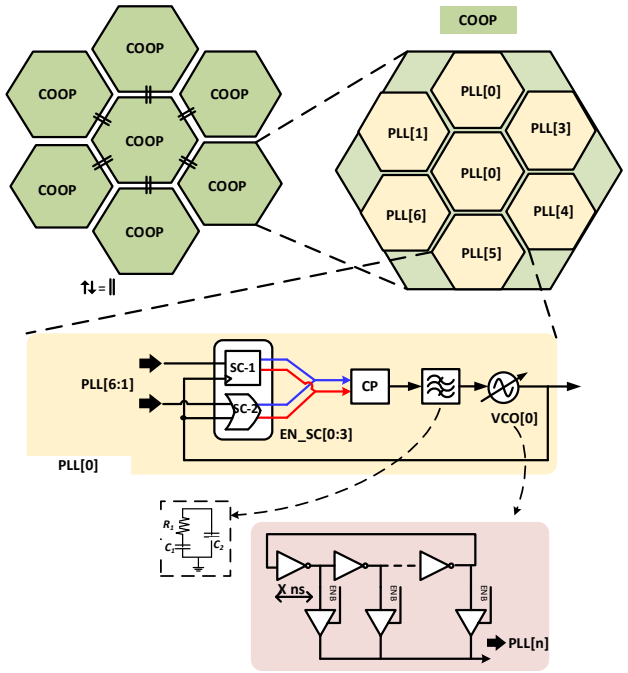
- Coupling of oscillators
- Information is in the phase

Analog and mixed-signal circuits for **Pattern Recognition**

Crossbar Arrays | **Oscillatory Neural Networks** | Edge AI Applications

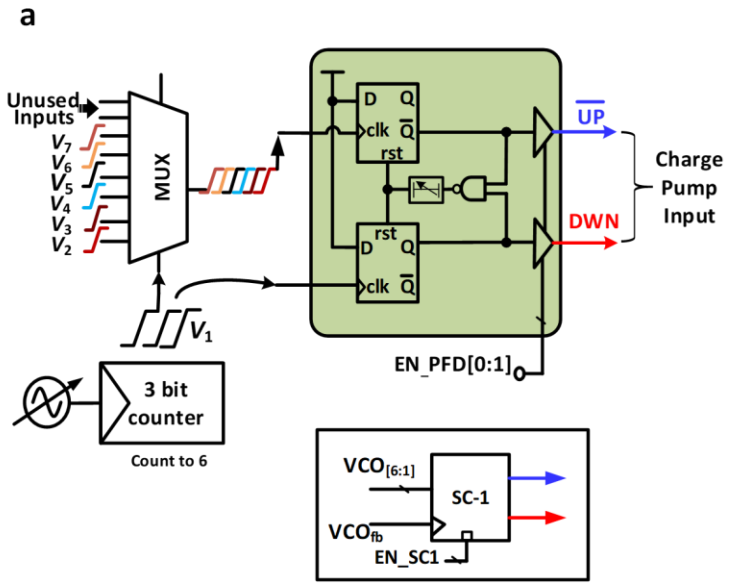
COUPLED OSCILLATOR SYSTEM

ARCHITECTURE

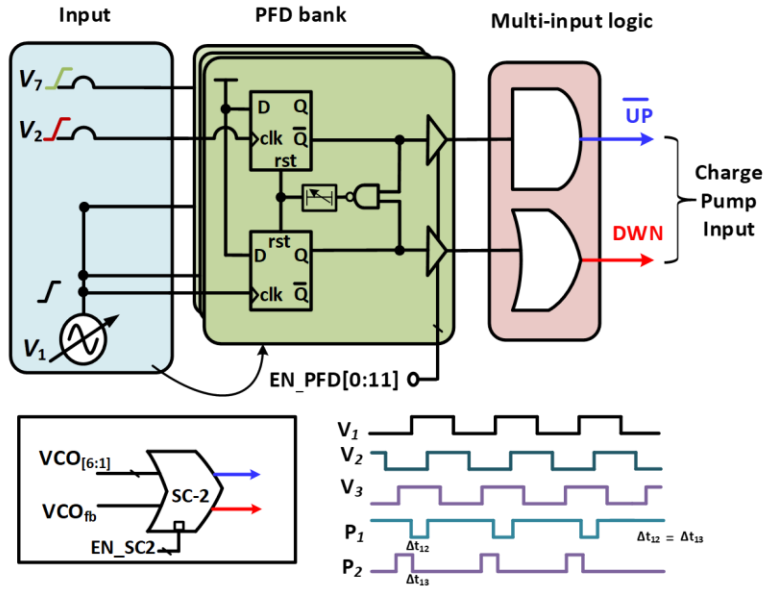


CONFIGURABLE COUPLING

Parallel to Serial (S1)



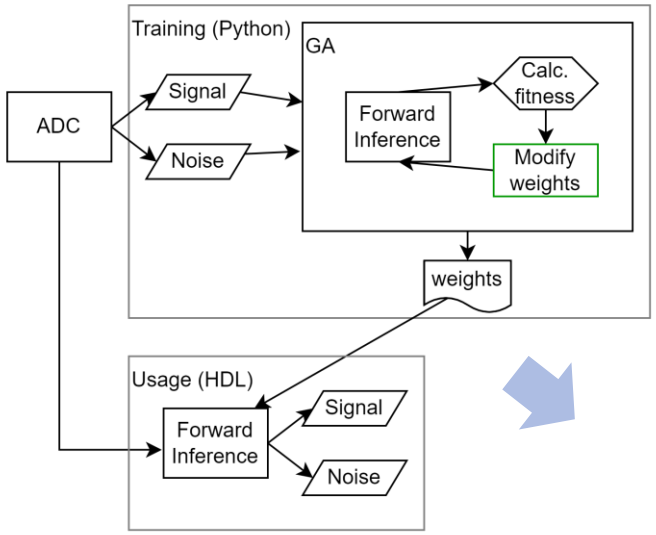
Parallel (S2)



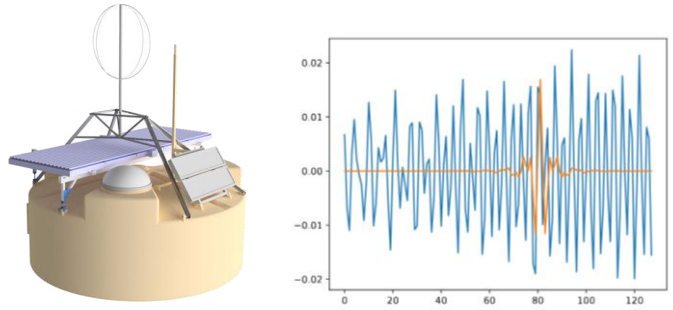
Crossbar Arrays | **Oscillatory Neural Networks** | Edge AI Applications

S.Y. Nayaz, A. Ashok, et.al, „Scalable 28nm IC implementation of coupled oscillator network featuring tunable topology and complexity“, https://arxiv.org/abs/2505.10248

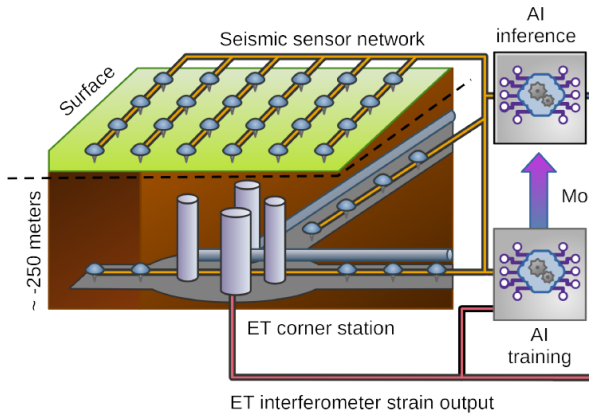
Edge AI Applications: Reuse of our Developments



Algorithm Development and On-Device Training



Online Feature Detection @ Pierre Auger Observatory



Online Noise Mitigation @ Einstein Telescope

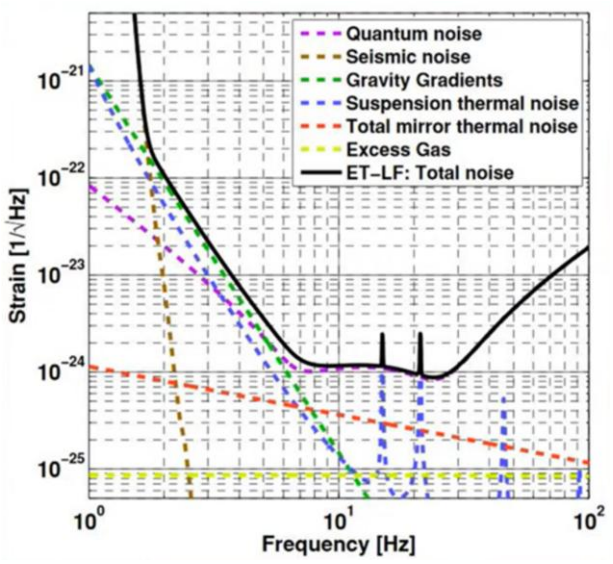
Applications, demo'ing the potential of **Edge AI,** e.g. Einstein Telescope

Low-energy, low-latency use cases

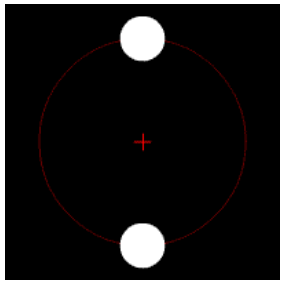
Goal: Systems with crossbars or ONNs
→ **Hardware Demonstrator**

Crossbar Arrays | Oscillatory Neural Networks | **Edge AI Applications**

Online Newtonian Noise Prediction for ET

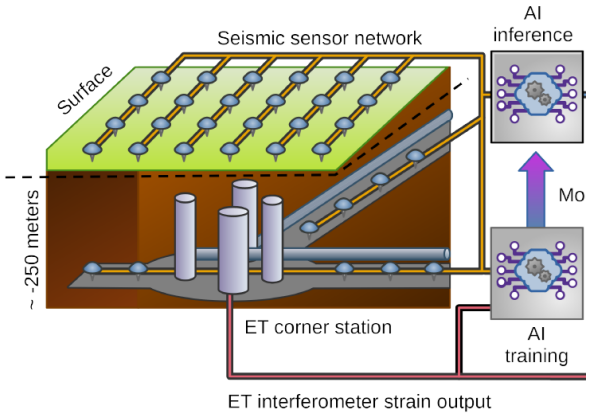


Einstein Telescope Noise Impacts
→ Low-freq. dominated by seismic noise



Binary Star System
When approaching:
increasing frequency

(src: Wikimedia)



Seismic Sensor Network around Detector
→ Enable noise prediction based on AI

Multi-Messenger Observation

- Gravitational waves can predict collision
- → The earlier we get aware of an event, the more time we have to redirect other detectors

Goal: Online Newtonian Noise Mitigation

- Real-time readout and data processing of sensor network
- Complex transfer function for noise prediction
- Approach: FPGA-based Neural Networks

In collaboration with: RWTH AACHEN UNIVERSITY, Universität Siegen

Crossbar Arrays | Oscillatory Neural Networks | Edge AI Applications

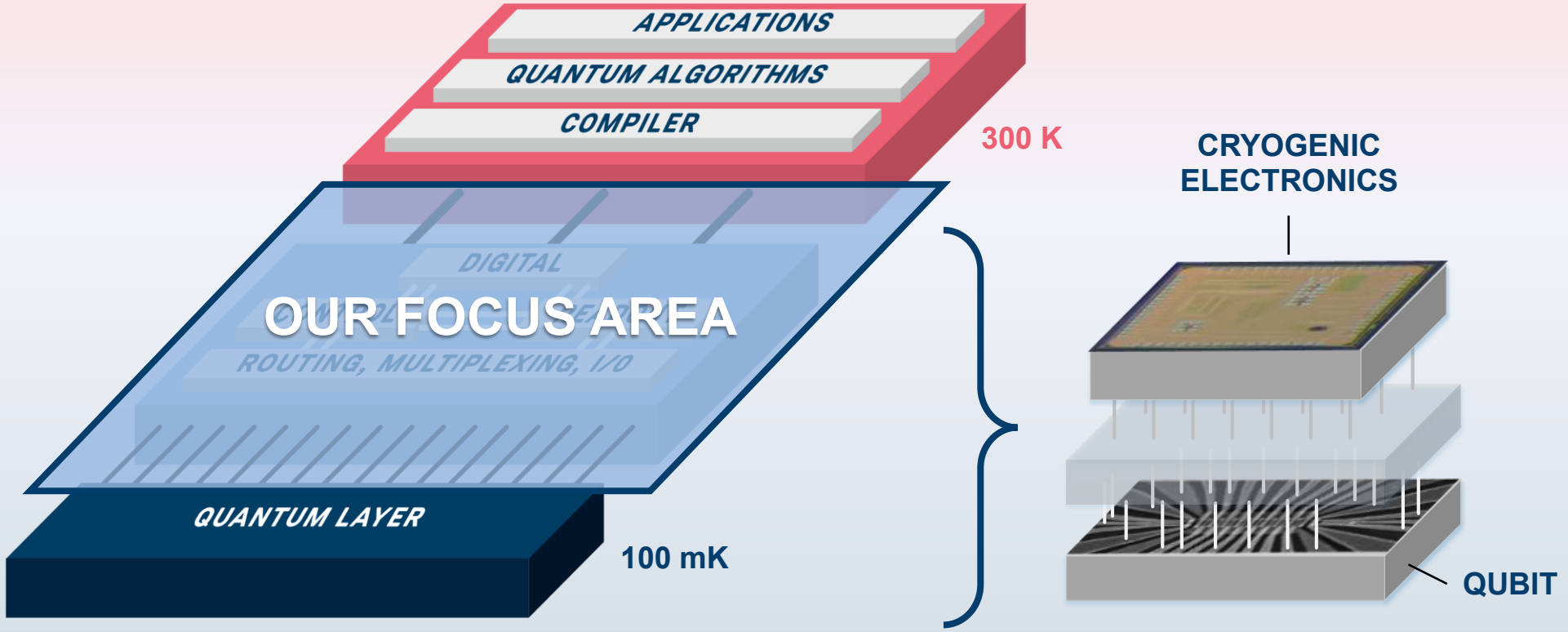
INTEGRATION WITH CMOS ELECTRONICS

Benefit From Existing Infrastructure To Scale Up

CLASSICAL COMPUTER

QUANTUM-CLASSICAL INTERFACE

QUANTUM PROCESSOR



System Modelling, Design and algorithmics

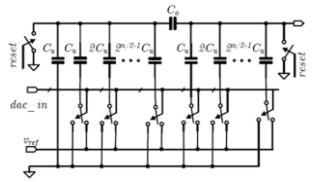
MODELLING

CO-SIMULATION

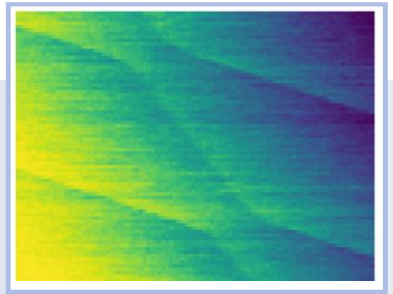
MODELLING / SIMULATION

TRAINING / DETECTION

cadence

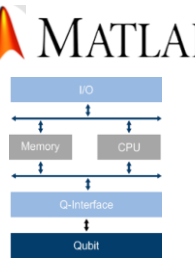


SCHEMATIC



CSD DATA

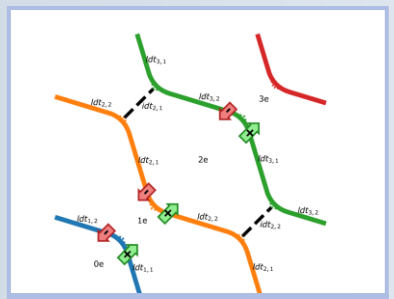
MATLAB



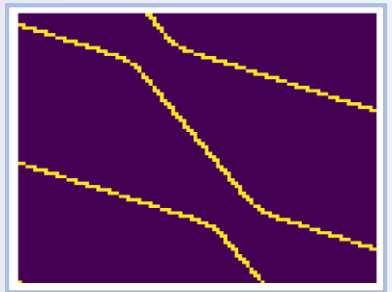
ELECTRONIC ARCHITECTURE

python

PHYSICS MODEL



GEOMETRIC MODEL



AUTOMATED DETECTION

SYSTEM DESIGN

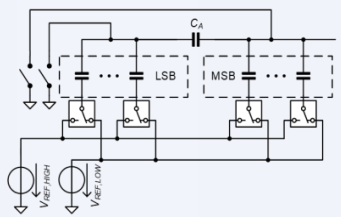
AUTOMATED TUNING

JÜLICH Forschungszentrum | Integrated Computing Architectures ICA

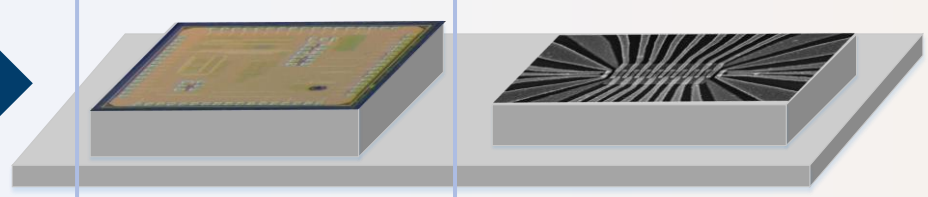
CRYOGENIC CIRCUIT DESIGN AND MEASUREMENT

CRYOGENIC CIRCUIT DESIGN

SCHEMATIC DESIGN

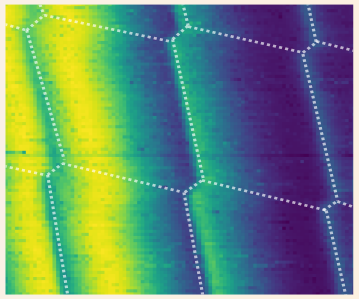


IMPLEMENTED CIRCUITS



TEST DEVICE SETUP

CRYO SETUP



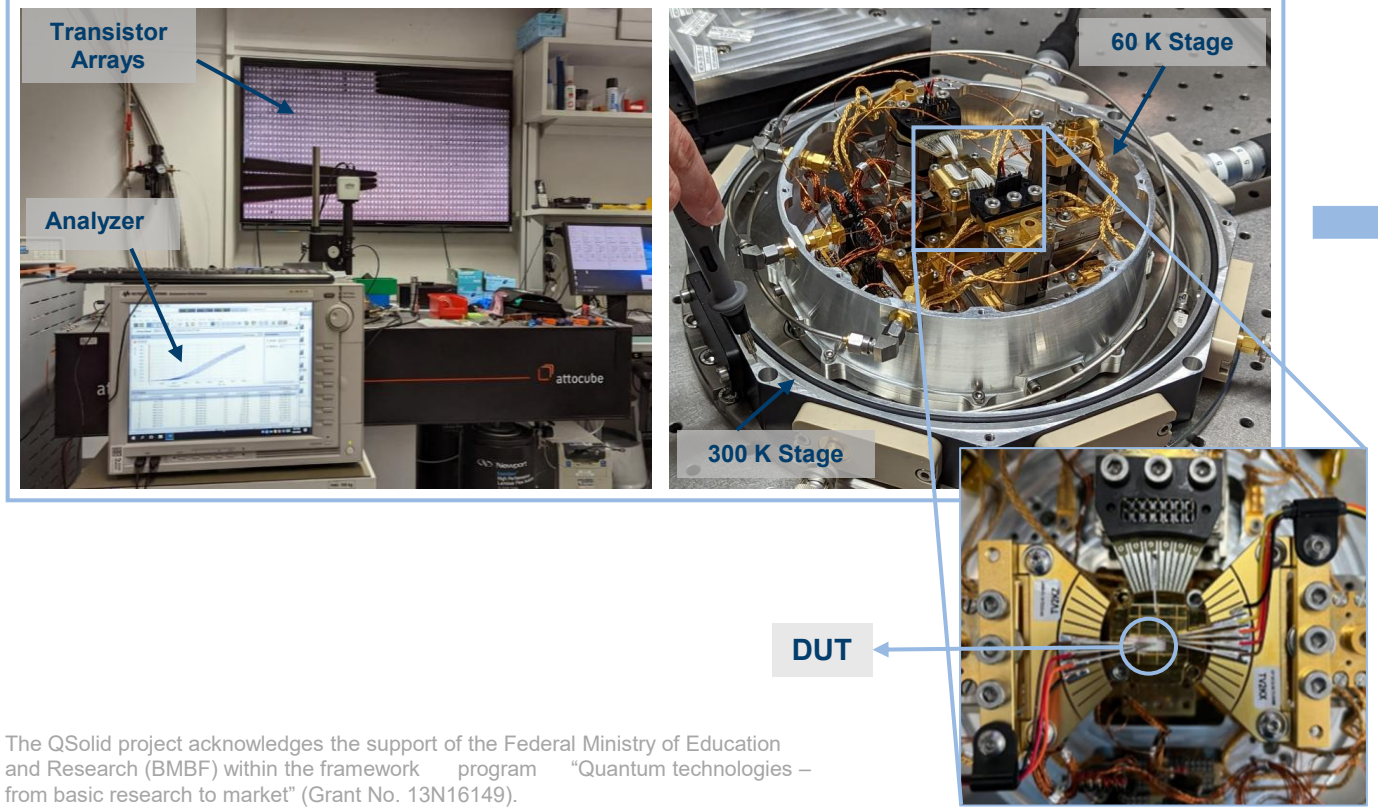
VERIFICATION RESULTS

CRYOGENIC MEASUREMENTS

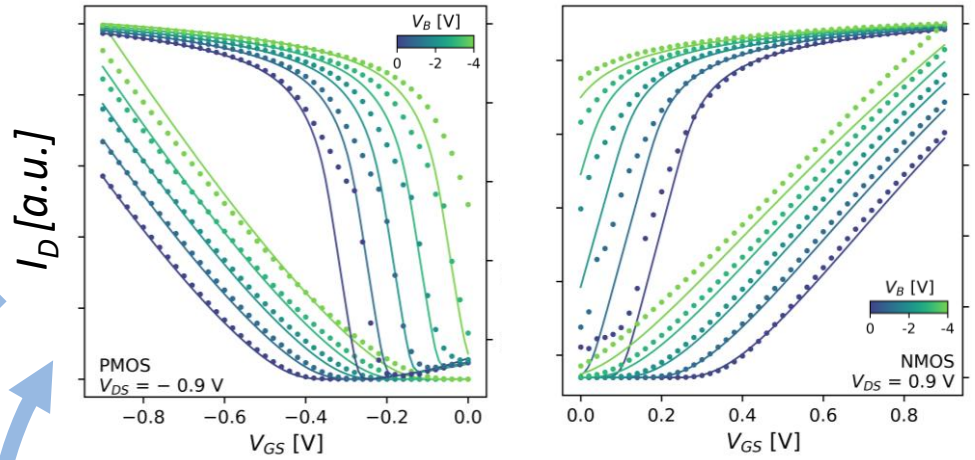
Cryogenic Measurements

Inputs for a Cryo-PDK for 22 nm CMOS

Setup @ ICA | FZJ: T_{min} ~ 7 K



Short-Channel I-V-Curves [1]



Input Data for BSIM-IMG Based Modeling

AdMOS — done by AdMOS GmbH

Cryogenic Model Library

The QSolid project acknowledges the support of the Federal Ministry of Education and Research (BMBF) within the framework program "Quantum technologies – from basic research to market" (Grant No. 13N16149).

DRD7 **Related to DRD7.4a**

SUMMARY

Integrated Computing Architectures

Semiconductors Enable Future Computing Architectures

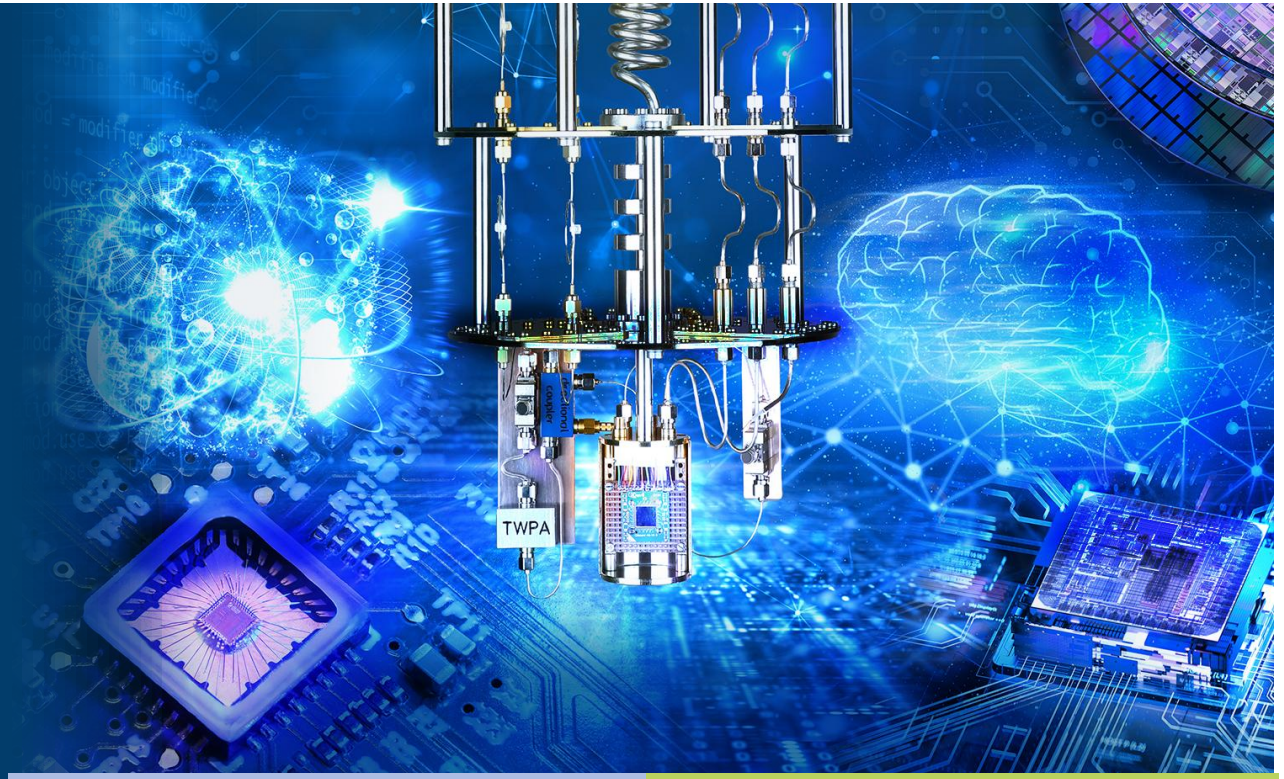
→ High integration, VLSI scalability

System Integration of Memristors, Qubits, etc.

→ Algorithms, hardware and physics co-design

System Modeling of Hardware Implementations

→ Application requirements and error mitigation / correction



Quantum Computing | Neuromorphic Computing