ARISTOTLE UNIVERSITY OF THESSALONIKI

UniBonn Workshop
2026 International Fellowship Framework

AUTH Electronics Lab

Chip Design towards AI enablement

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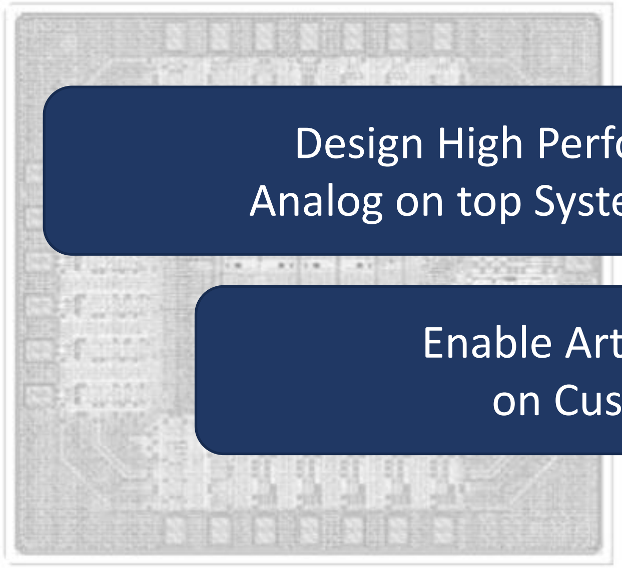
ΤΜΗΜΑ ΗΛΕΚΤΡΟΛΟΓΩΝ ΜΗΧΑΝΙΚΩΝ & ΜΗΧΑΝΙΚΩΝ ΥΠΟΛΟΓΙΣΤΩΝ

School of Physics
Aristotle University of Thessaloniki

ATLAS IC

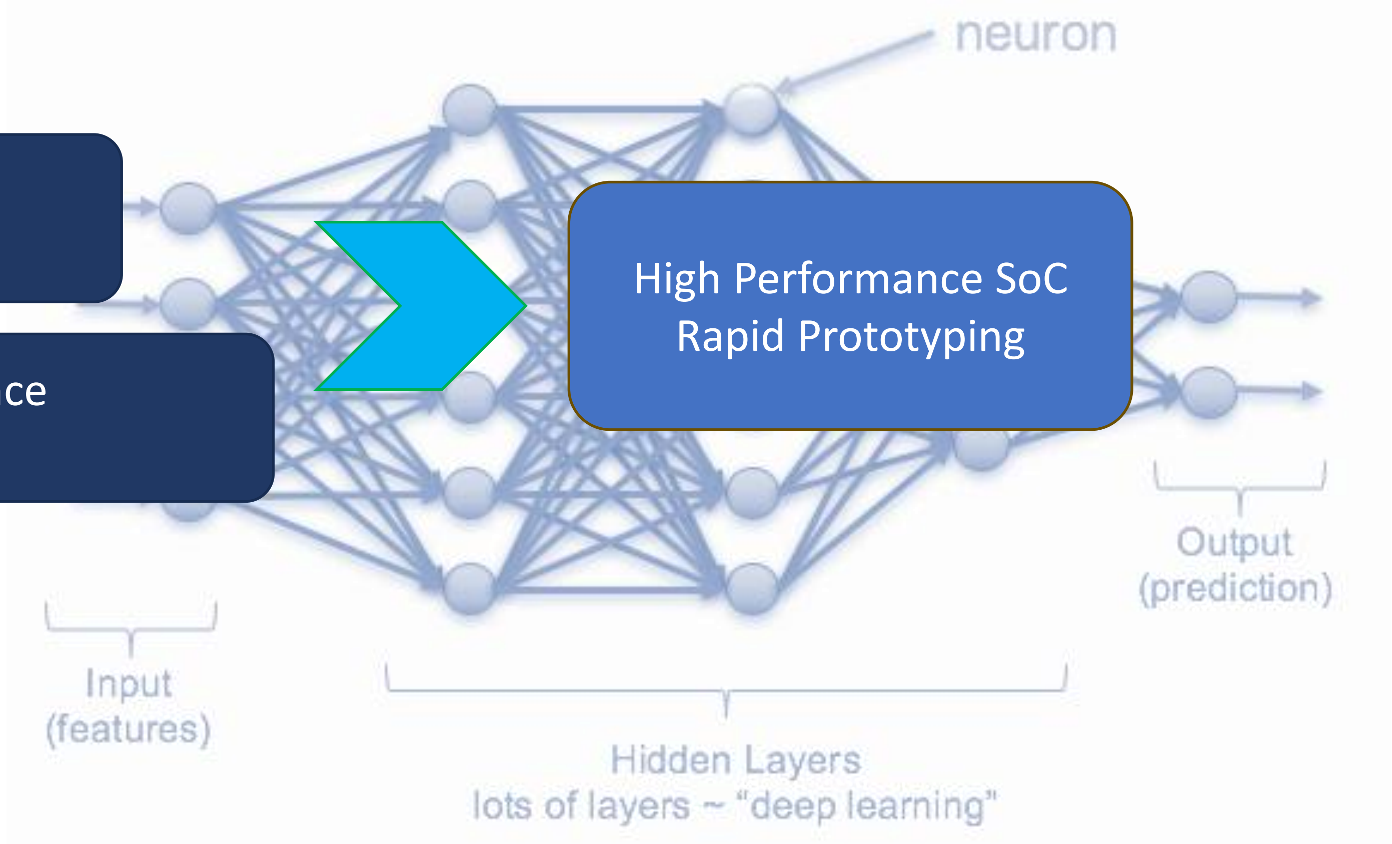
ASIC Lab Mission



Design High Performance
Analog on top System on Chip

Enable Artificial Intelligence
on Custom IC Design

High Performance SoC
Rapid Prototyping

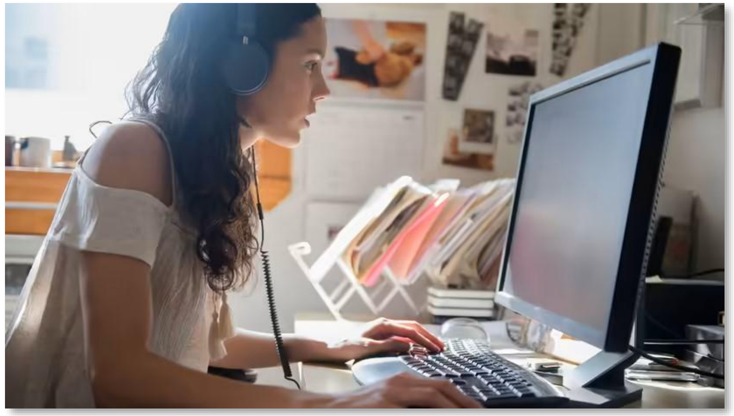


How will we design Analog chips in the Future?

https://blog.baruthotels.com/en/the-spectacular-life-story-of-the-famous-artist-salvador-dali

1. The Hand-crafted Artistic Way?

https://computer.howstuffworks.com/10-types-of-computers.htm

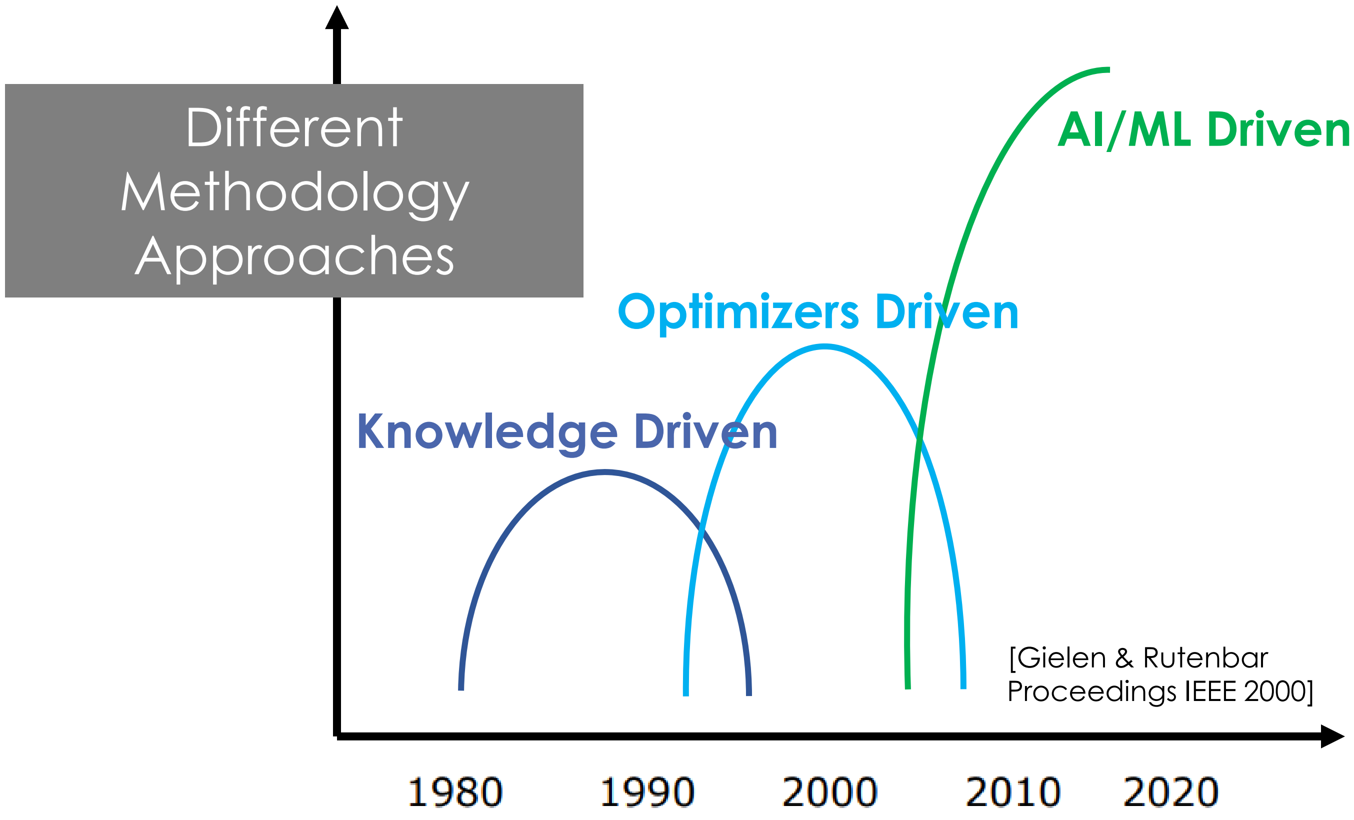


2. Tool Assisted "hand crafted" way?

https://www.fenews.co.uk/wp-content/uploads/2023/03/Canva-AI-digital-1-768x512.jpg

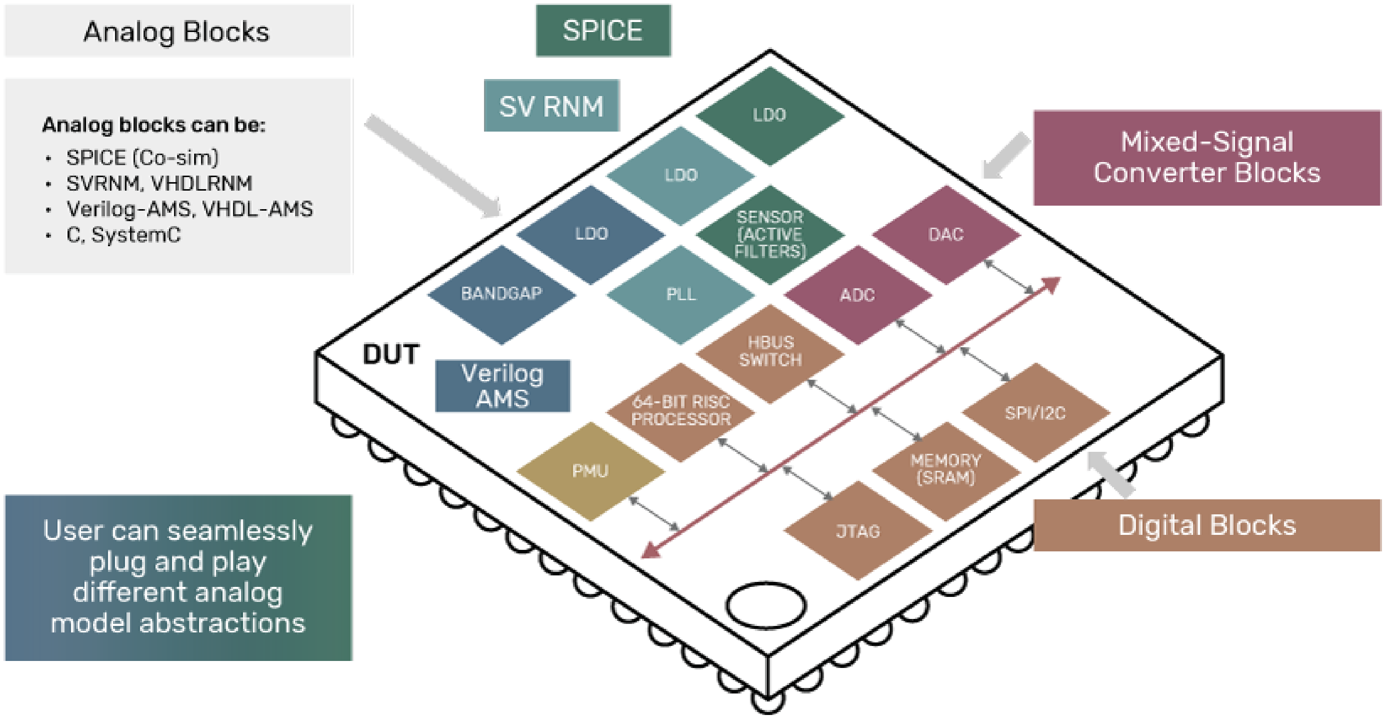
3. AI/ML inspired way?

Three Waves of Analog Synthesis



1. **Knowledge Driven**
   Heuristic way of designing circuits, hand calculations based – book driven
2. **Optimizers Driven**
   Gm/Id methodology, ADT toolbox, and many other EDA solutions
3. **AI/ML Based**
   Under development!

Baseband Analog on Top SoC



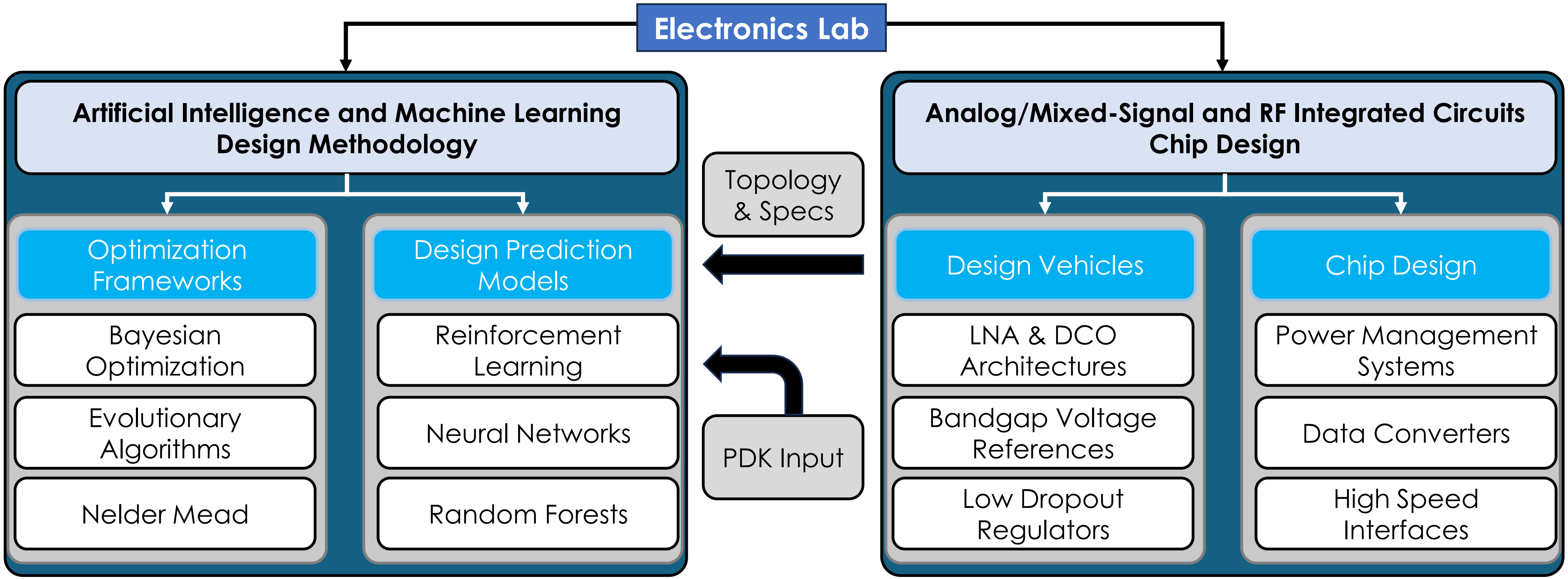
Focus on the Analog/RFMS blocks such as voltage references, LDOs, ADC/DAC, Baseband (Amps and filters) and Wireless (RX/TX)

https://www.cadence.com/content/dam/cadence-www/global/en_US/images/resources/whitepaper/demystifying-mixed-signal-simulation-for-digital-verification-engineers-wp-fig-2.png

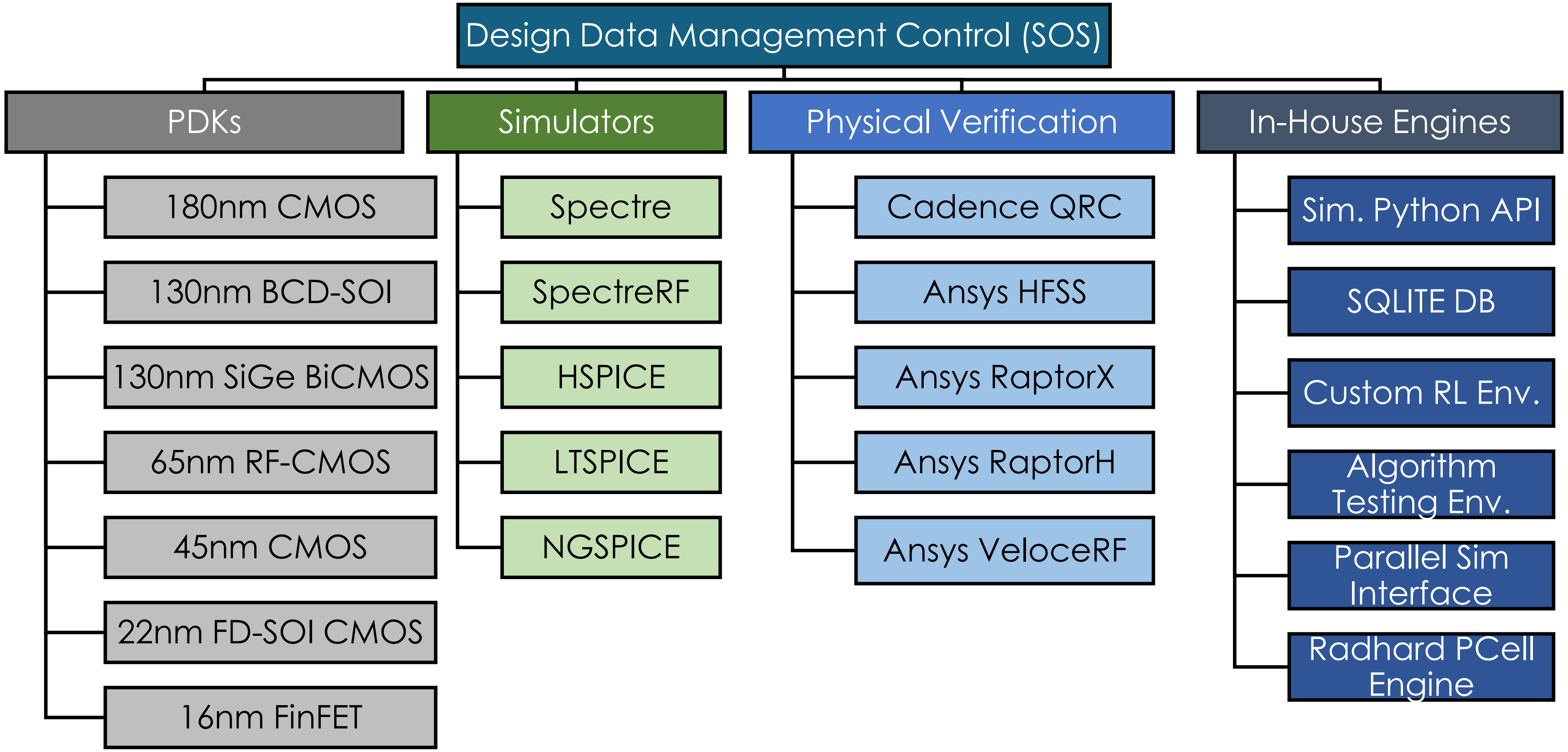
Analog/RFMS Blocks

Data Converters	Analog-to-Digital Converters (ADCs) Digital-to-Analog Converters (DACs)
Power Management Units (PMUs)	Low Dropout (LDO) Regulators, DC-DC Converters, Voltage References,
Radio Frequency (RF) Blocks	Low Noise and Power Amplifiers VCOs/DCOs, Mixers and Dividers
Timing and Frequency Generation	Phase-Locked Loops (PLLs) Oscillators
Sensor Interfaces/Analog Front Ends (AFEs)	Operational Amplifiers and PGAs Integrated Filters

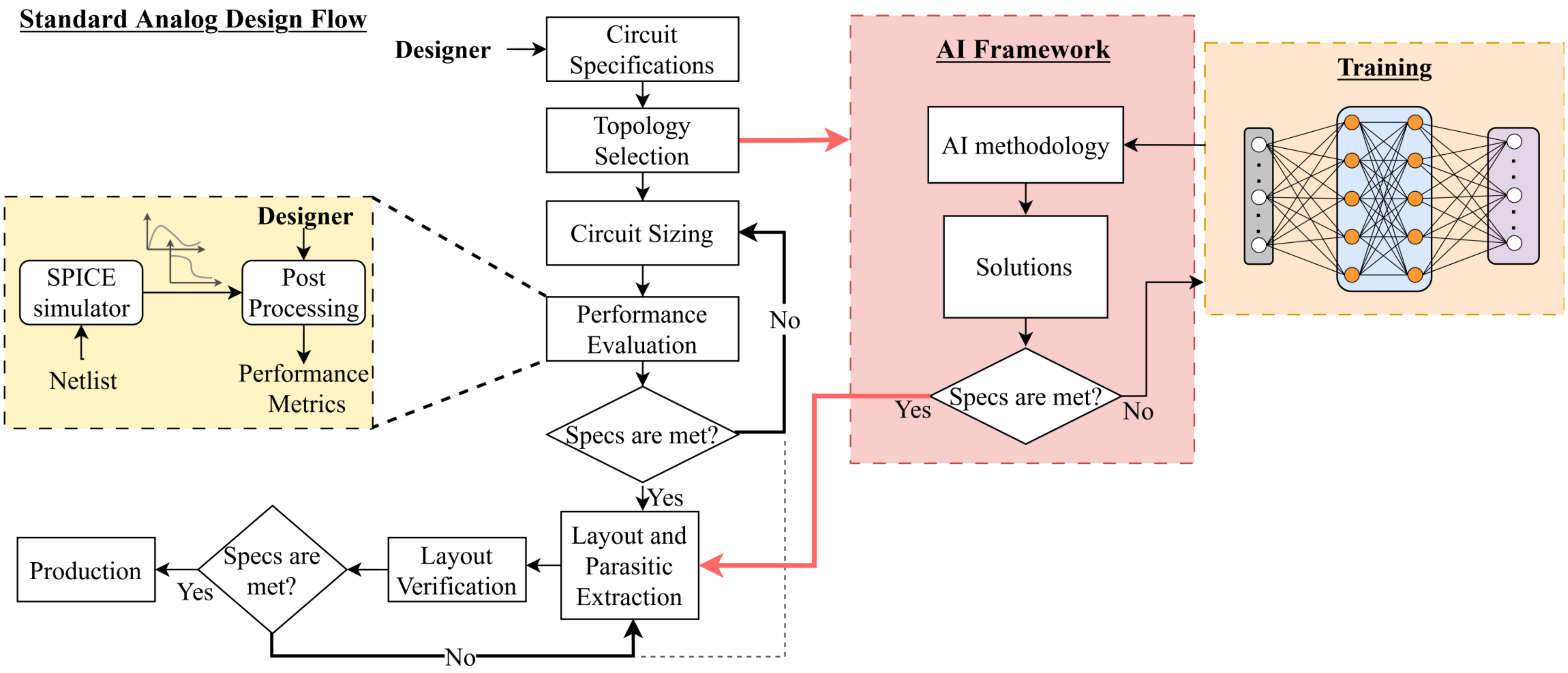
Analog Design/AI Team Expertise



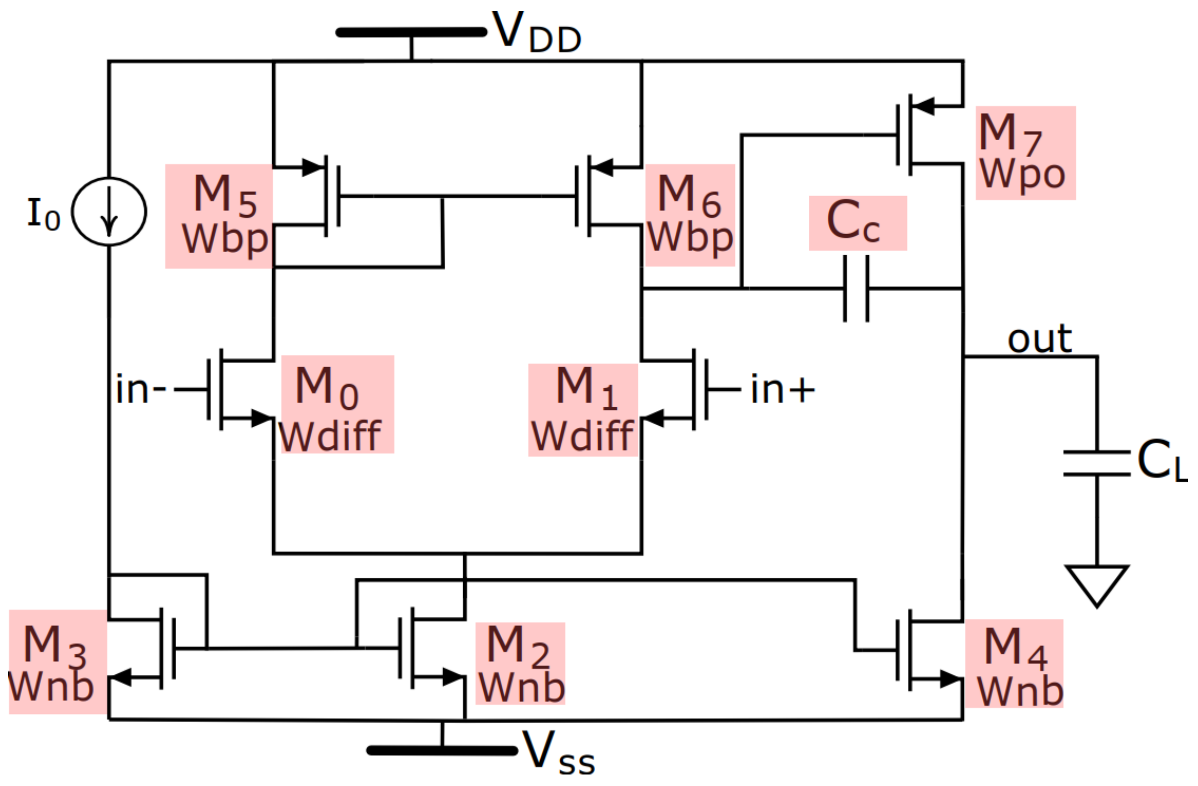
Infrastructure



AI/ML Custom Design Engine

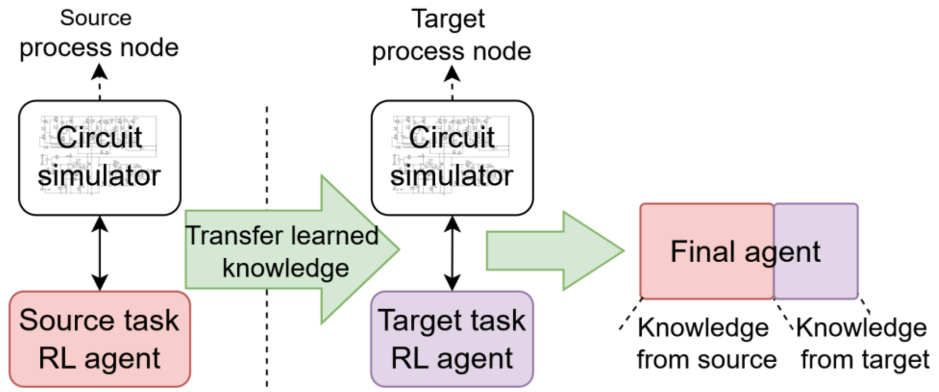


OpAmp AI Design

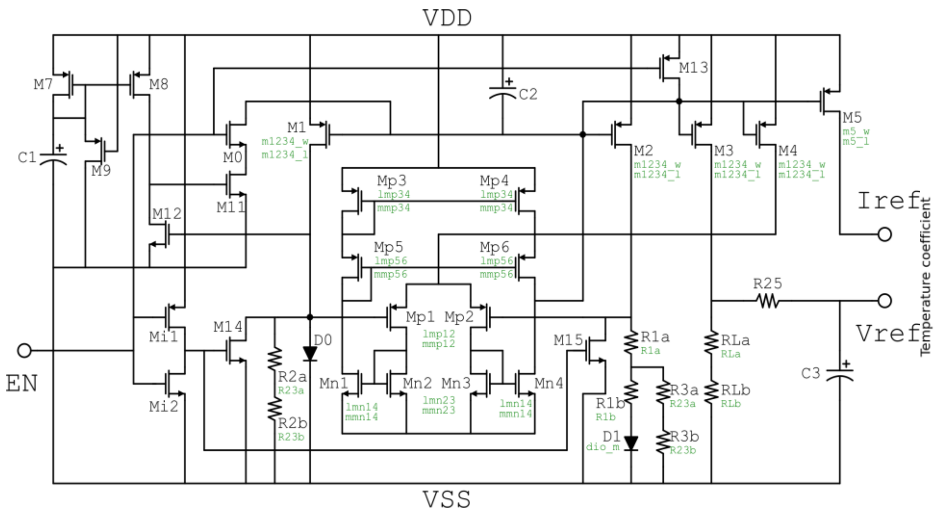


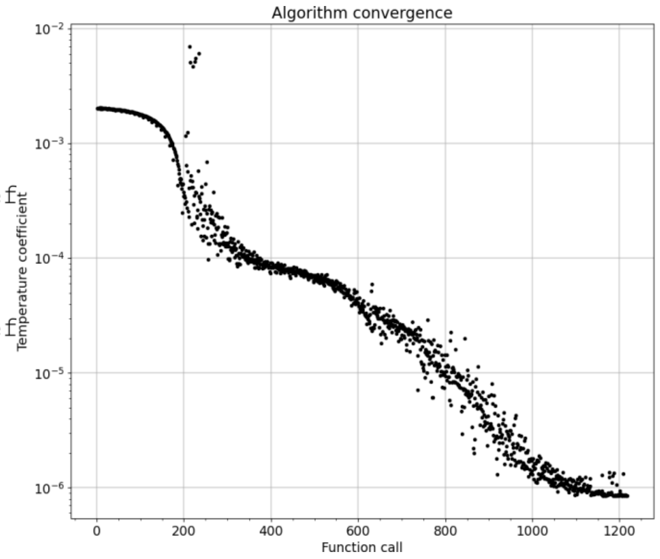
Adjustable Parameters	Performance metrics
Wbp	Phase margin
Wdiff	Unity gain bandwidth
Wnb	Gain
Wpo	ICMR
Cc	Vout swing
	Slew Rate

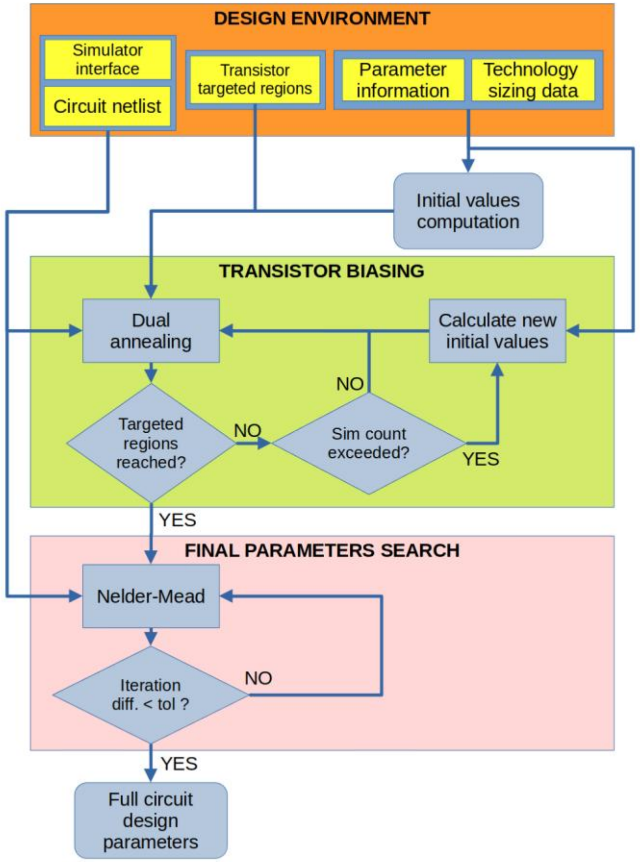
Knowledge transfer between technology nodes



Bandgap AI Design



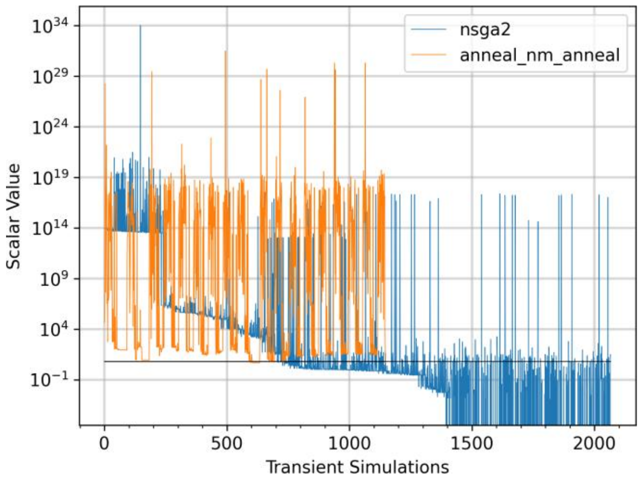


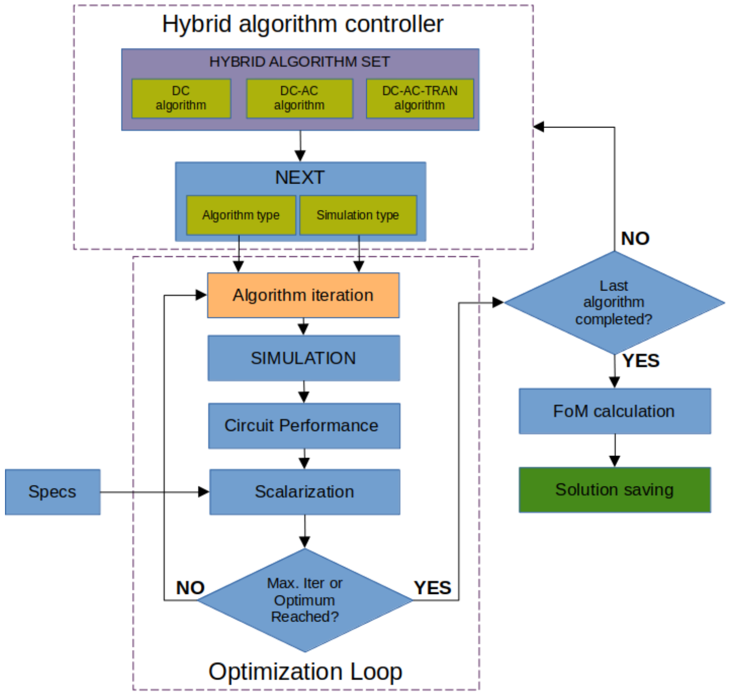


- 21 parameters
- 0.84 ppm final temperature coefficient (instead of 10)
- 12 µW power (instead of 20)
- 1260 simulations (~26 minutes)

LDO AI Design

- 30 free parameters
- full complexity LDO design [1]
- 10 outputs
- 14 hybrid algorithm setups (including transient analysis!)
- 31% savings in transient analysis (~1150 sims on avg) compared to state-of-the art NSGA-II optimizer (~1660)
- State of the art specs (table below)

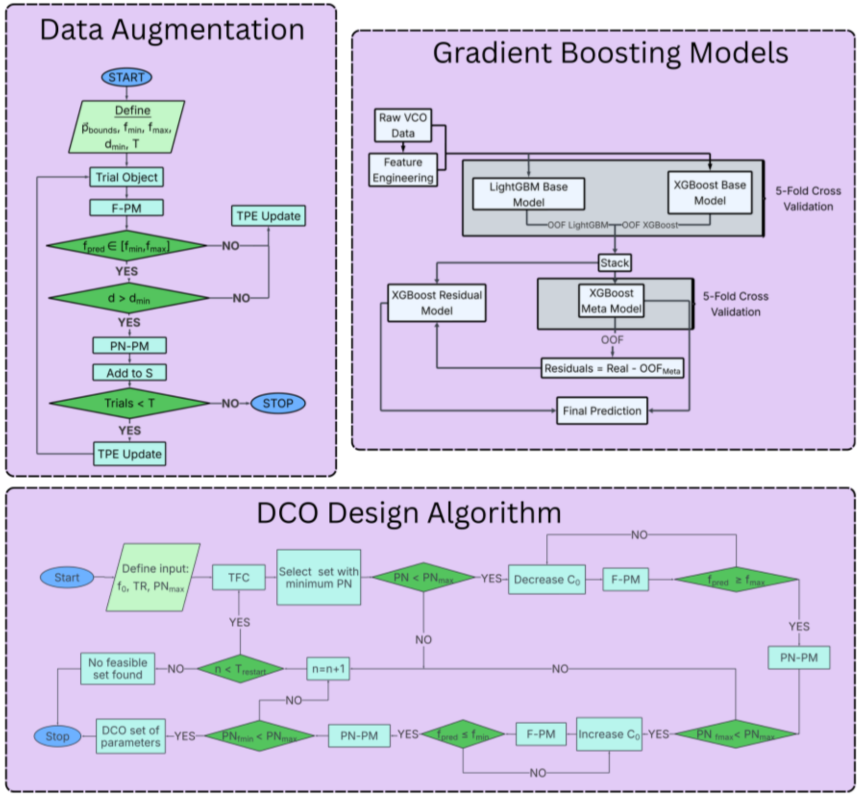


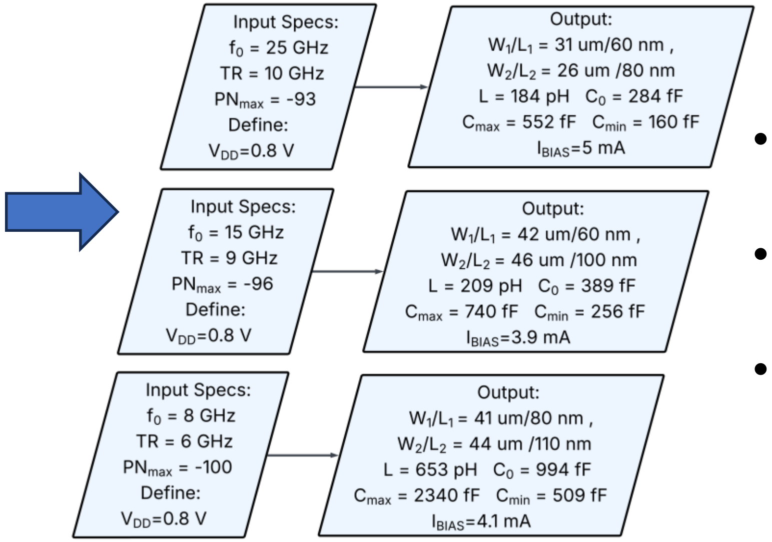


METRIC NAME	DESCRIPTION	[1]	Algorithm result	Improvement [%]
OTA_DC_GAIN	Gain of the Error amplifier	80	80.96	+1.19
PSRR	PSRR at zero frequency [dB]	-70	-78.01	+11.42
PHASE_MARGIN	Phase margin [deg]	45	77.74	+76
LNR	Line regulation [mV/V]	0.01992	0.01543	+22.85
LDR	Load regulation [μV/mA]	0.25	0.1437	+42.52
QUESC_CUR	Quiescent current [μA]	6.3	36.30	-476
LNR_LOW_RECTIME	LNR rec. time from low [μs]	22	1.635	+92.00
LDR_LOW_RECTIME	LDR rec. time from low [μs]	10	1.668	+83.33
LNR_HIGH_RECTIME	LNR rec. time from high [μs]	22	12.83	+41.68
LDR_HIGH_RECTIME	LDR rec. time from high [μs]	10	7.640	+23.00

[1] Nikolaos Zachos, Vasiliki Gogolou, and Thomas Noulis. A fully integrated 1.8 v low-power ldo regulator with dynamic transient control for soc applications. Electronics, 13(23), 2024.

DCO AI Design





- *From user-defined specifications to schematic design.*
- *Predictive models with RMSE > 0.15*
- *Performance error below 5% across the 5-30 GHz frequency range.*

State-of-the-Art Comparison

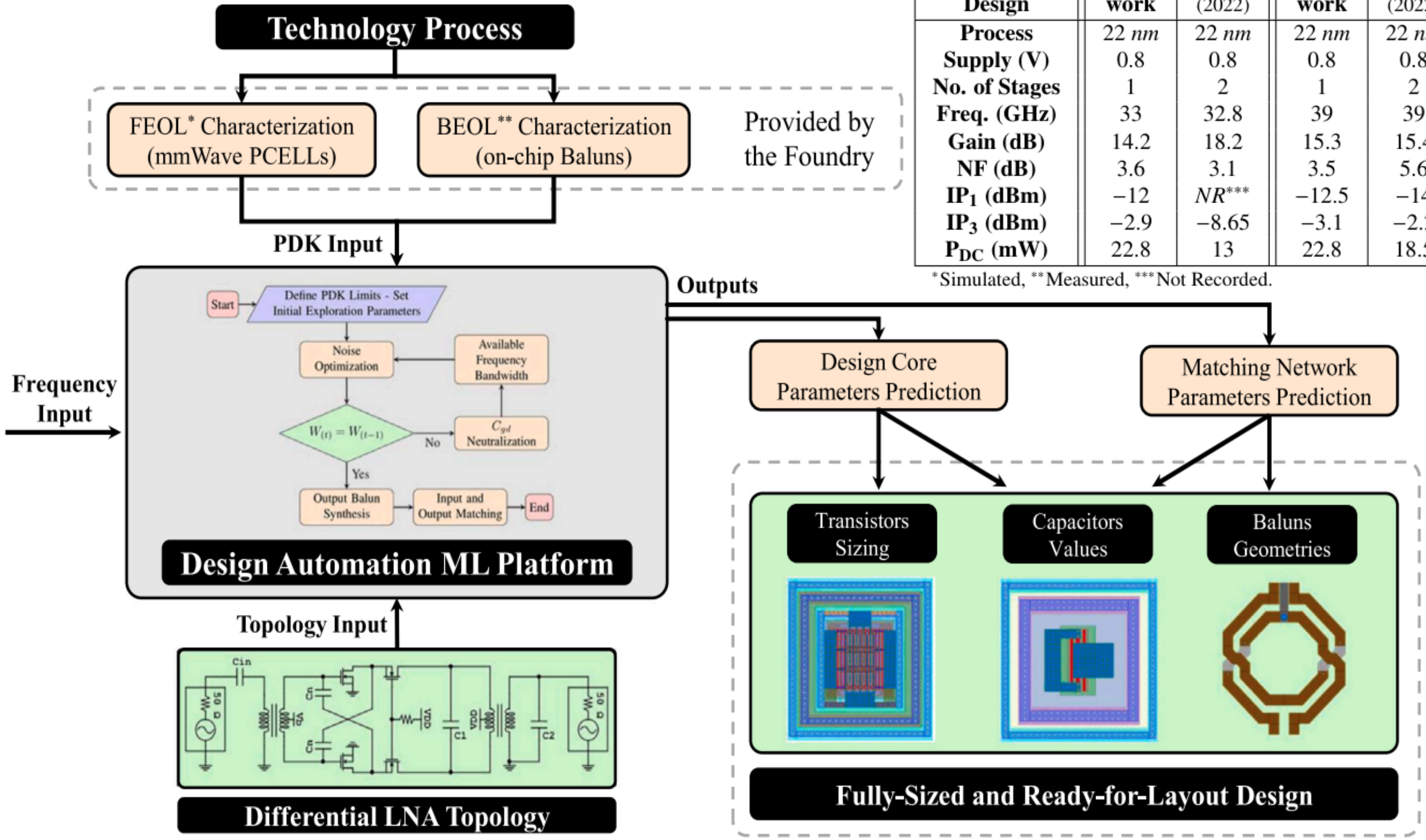
Performance Metrics	HFB DCO	MFB DCO	LFB DCO	[27]	[28]	[29]	[30]	[31]
CMOS Process	22 nm FDSOI	22 nm FDSOI	22 nm FDSOI	65 nm	55 nm	22 nm FDSOI	28 nm	22 nm FDSOI
Center Frequency [GHz]	24.9	14.1	8	24	10	23.8	16.25	19.8
Tuning Range (%)	35	63.1	71.2	29	9	5	20.3	23.5
Phase Noise [dBc/Hz]	-100	-101.8	-109.5	-104	-106.3	-96.6	-117.3	-112.1
Power [mW]	8.5	7.8	7.3	16.9	7.3	14.4	22.1	24
Area [mm^2]	0.02	0.022	0.025	0.6	N/A	0.026	0.16	0.596
FoM_T [dBc/Hz]	-189.5	-191.9	-196.0	-188.6	-176.8	-166.5	-194.2	-191.7

LNA AI Design

User-defined

Application [39]

Frequency Ranges (GHz)	Candidate Bands for 5G (GHz)
24	24.25 – 24.45, 25.05 – 25.25
LMDS	27.5 – 28.35, 29.1 – 29.25, 31 – 31.3
39	38.6 – 40
37/42	37 – 38.6, 42 – 42.5
60	57 – 64, 64 – 71
70/80	71 – 76, 81 – 86

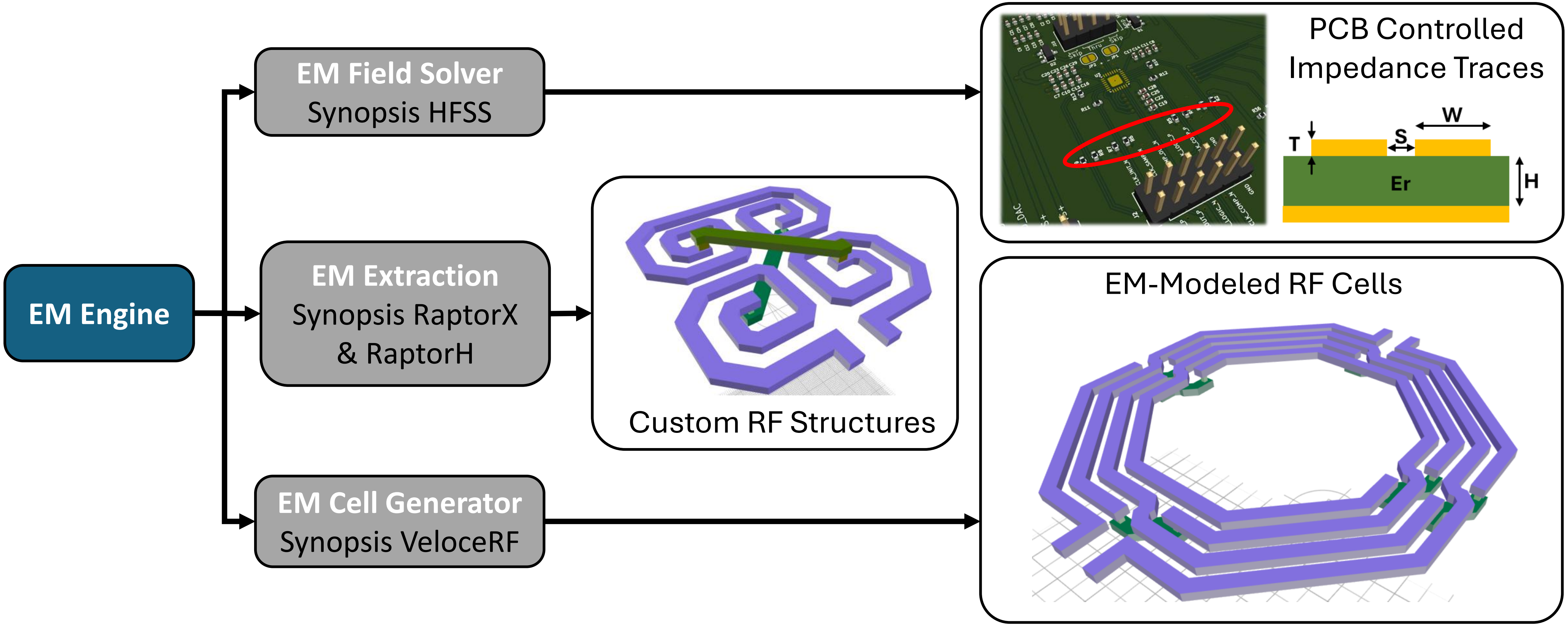


State-of-the-Art Comparison

LNA Design	This* work	[34]* (2022)	This* work	[35]** (2022)	This* work	[36]** (2021)	This* work	[37]** (2018)	This* work	[38]** (2020)
Process	22 *nm*	22 *nm*	22 *nm*	22 *nm*	22 *nm*	22 *nm*	22 *nm*	22 *nm*	22 *nm*	22 *nm*
Supply (V)	0.8	0.8	0.8	0.8	0.8	0.85	0.8	1	0.8	1.6
No. of Stages	1	2	1	2	1	2	1	2	1	3
Freq. (GHz)	33	32.8	39	39	60	60	73.5	73.5	91	92
Gain (dB)	14.2	18.2	15.3	15.4	16.5	18.1	16.3	20	15.3	18.2
NF (dB)	3.6	3.1	3.5	5.6	3.7	4.9	3.9	4	4.4	5.8
IP_1 (dBm)	−12	*NR****	−12.5	−14	−15.3	−21.1	−17.4	−22.8	−18.5	−22.8
IP_3 (dBm)	−2.9	−8.65	−3.1	−2.2	−5.8	*NR****	−8.2	−3.9	−9.7	*NR****
P_{DC} (mW)	22.8	13	22.8	18.5	22.8	3.6	22.8	10.8	22.8	16

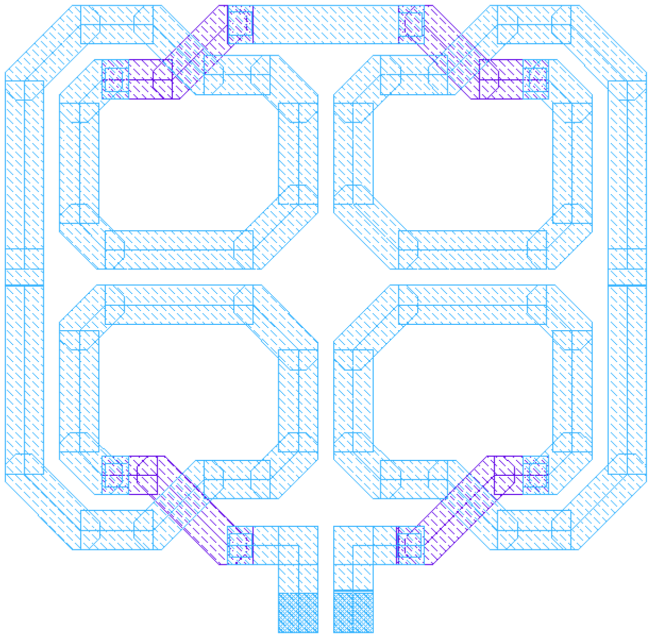
*Simulated, **Measured, ***Not Recorded.

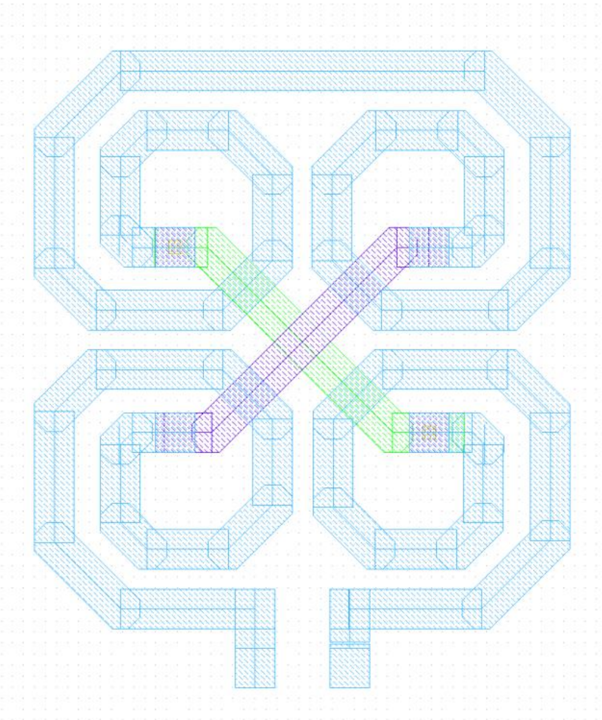
EM Extraction

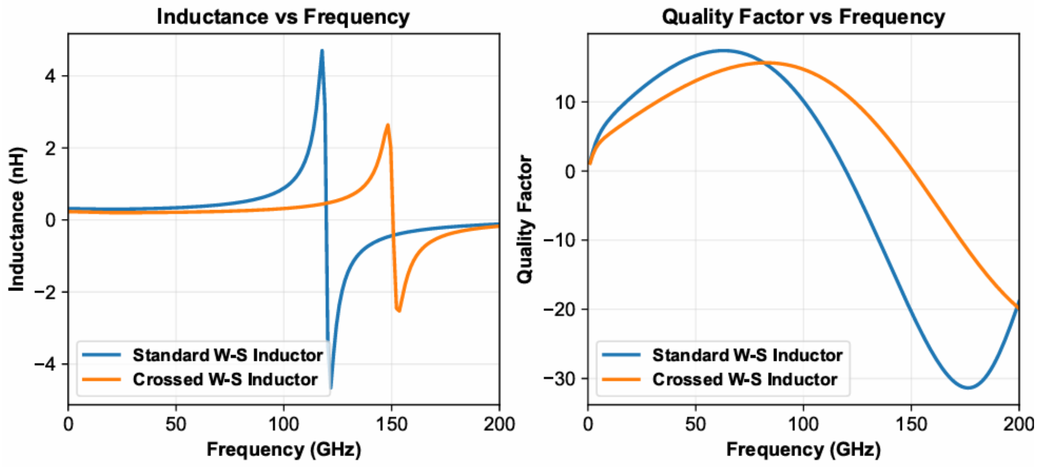


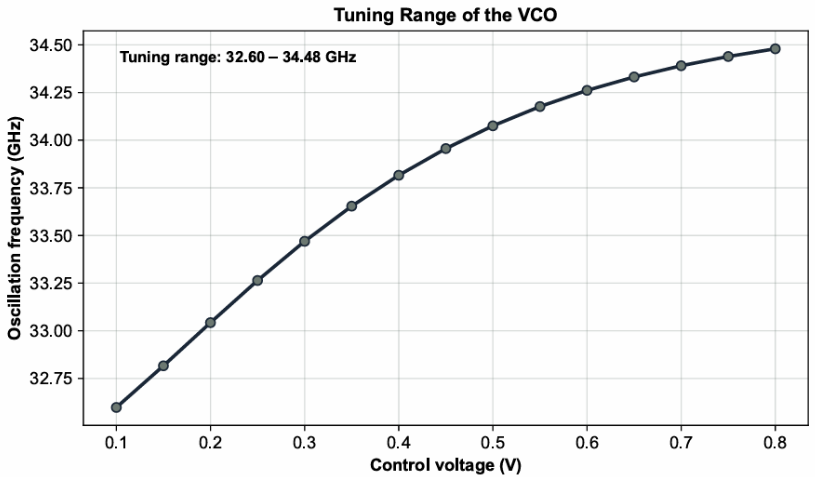
Chip Design – RF Front-Ends

-90 dBc/Hz @ 1MHz Window-Shaped Inductor EM Characterization for 33GHz VCO in 22nm CMOS FD-SOI



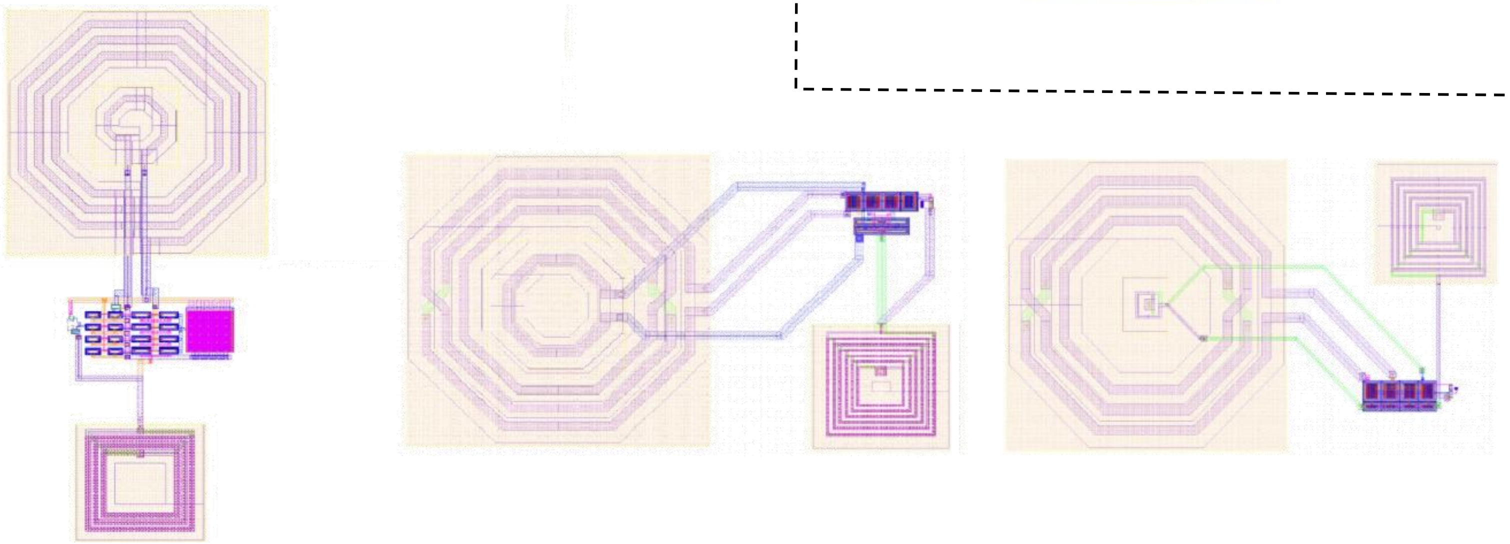


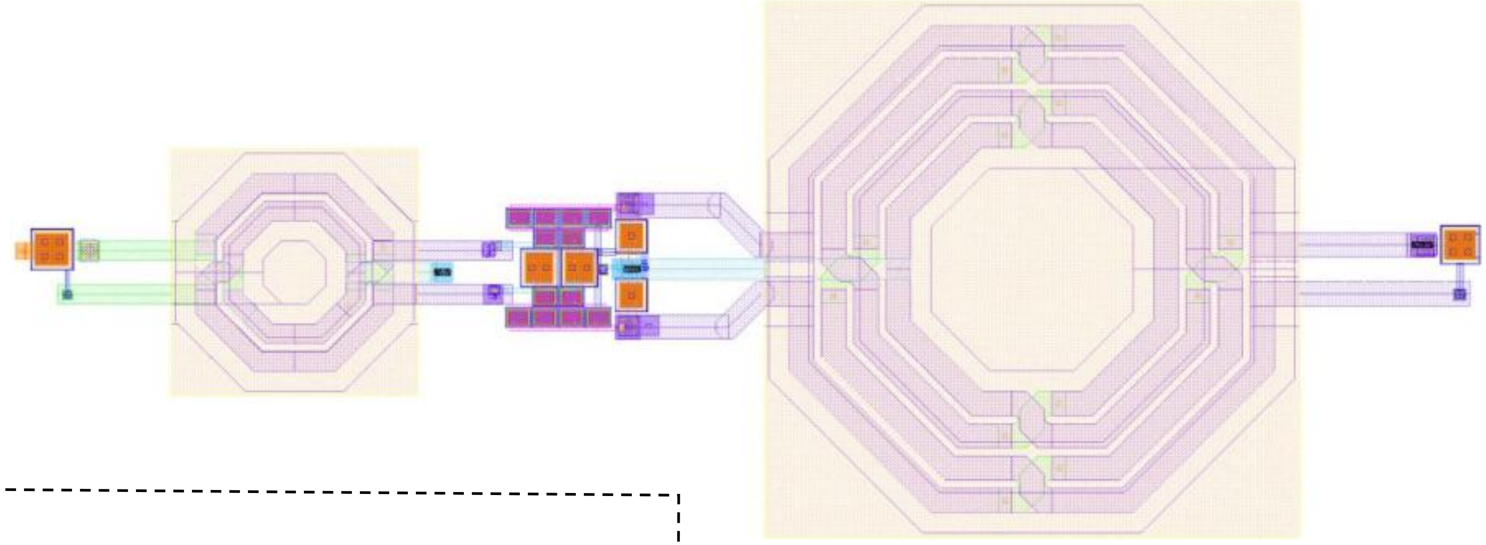




Chip Design Activities – RF Front-Ends

2.5GHz, 5GHz and 10GHz Nested Single-Ended LNAs with 15dB Gain and NF < 3dB in 22nm CMOS FD-SOI

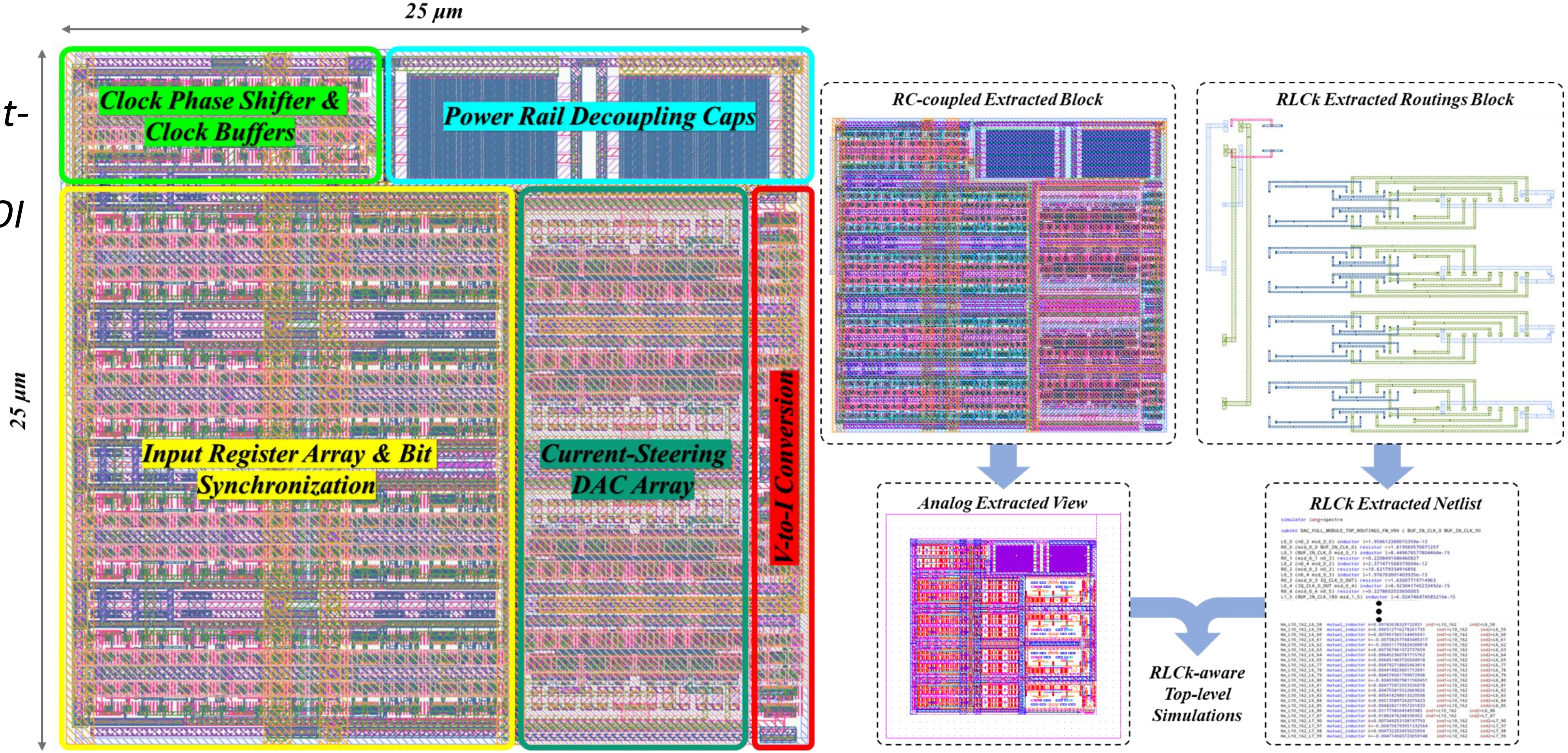




33GHz Differential LNA with 16dB Gain and NF < 4dB in 22nm CMOS FD-SOI

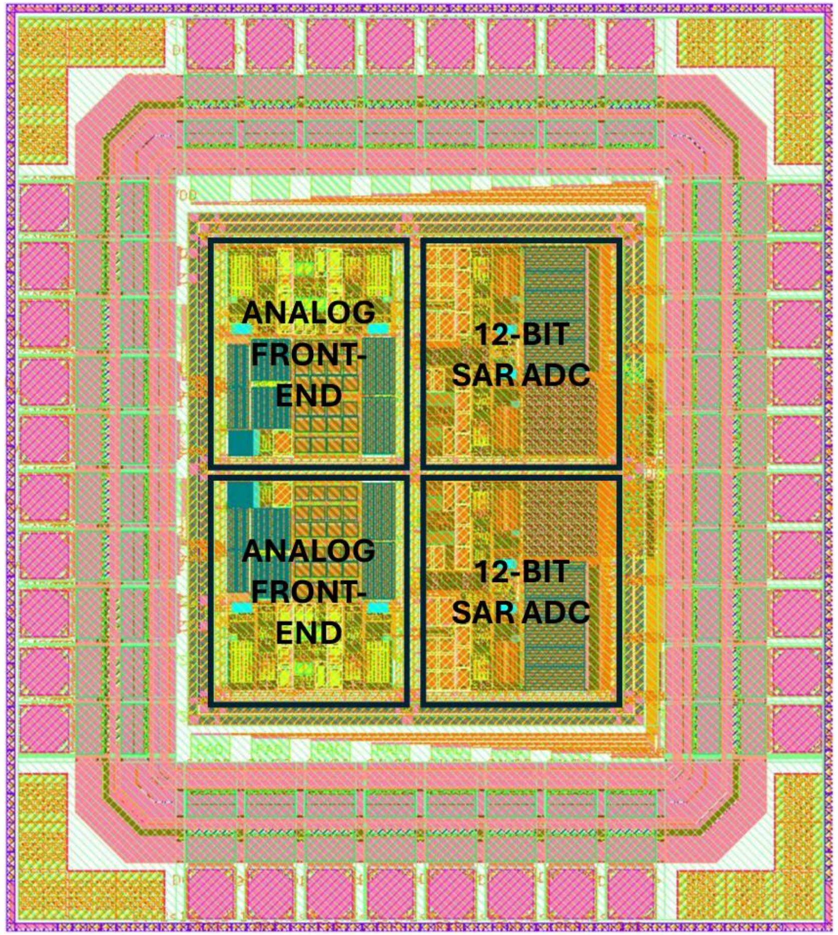
Chip Design Activities – Data Converters

28GS/s Time-Interleaved Current-Steering DAC in 22nm CMOS FD-SOI

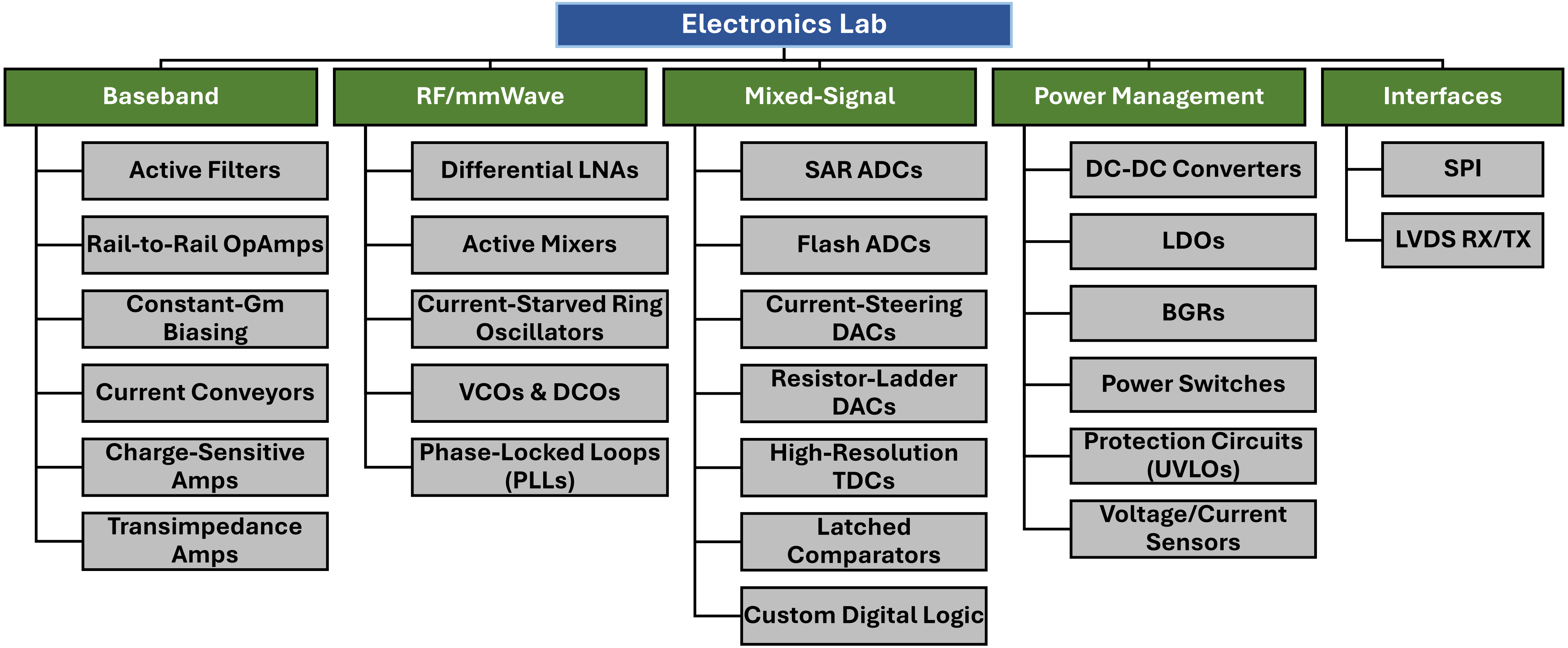


Chip Design Activities – Data Converters

12-Bit 250kS/s SAR Analog-to-Digital Converter in 180nm CMOS



Chip Design Portfolio



Digital Design Suite

Design Step	Cadence	Synopsys
RTL Simulation / Verification	Xcelium / IMC	VCS/ Verdi
Formal Verification / Lint	Jaspergold	VC static / Spyglass
Synthesis	Genus	Design Compiler
Equivalence Check	LEC	Formality
Power Estimation	Joules	Primepower
Place & Route	Innovus	
Static Time Analysis	Tempus	

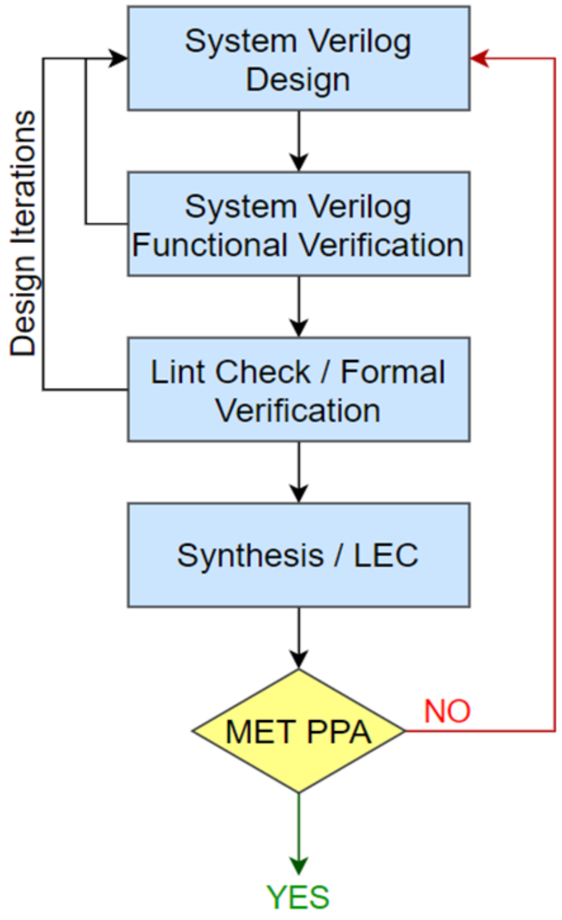
Chip Design Activities – Floating Point IPs

High-performance Floating-Point circuits, based on IEEE-754 Standard

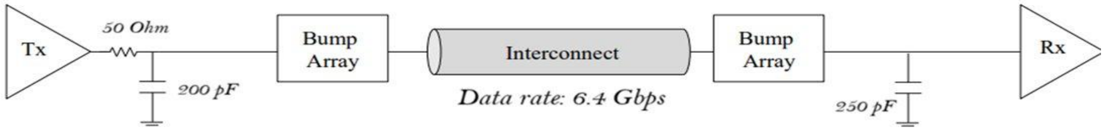
- Fully IEEE compliance
- RISC-V based architecture
- Single precision, half precision and all parameterizable custom precisions from float-8 to float-32
- 400 MHz frequency @40 nm with 3-stage pipelined logic

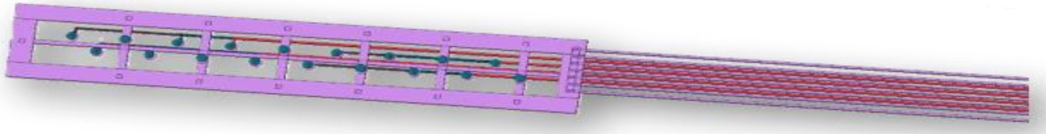
Arithmetic IPs	Conversion IPs
FP multiplier	FP to integer
FP division	Integer to FP
FP adder	FP to FP conversion
FP Multiply and Accumulate (MAC)	FP comparator
FP reciprocal	
FP square root	
FP inverse square root	

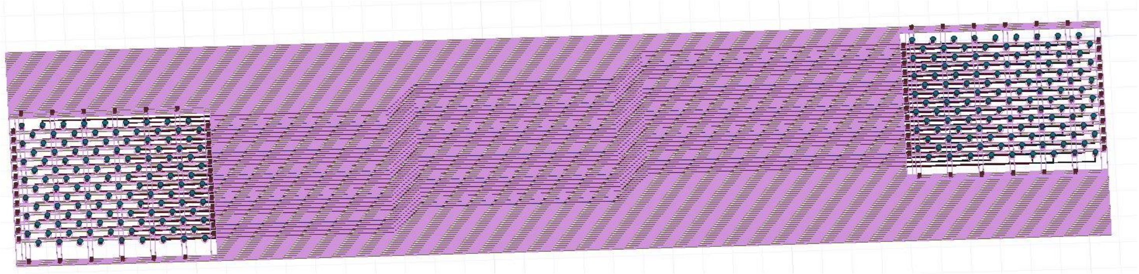
Rounding Modes
IEEE round to nearest even
IEEE round to zero
IEEE round to positive infinity
IEEE round to negative infinity
Round to nearest up
Round away from zero
Round to odd

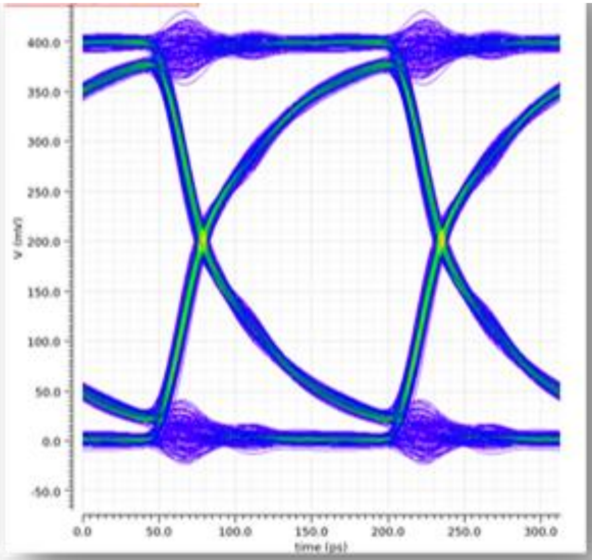


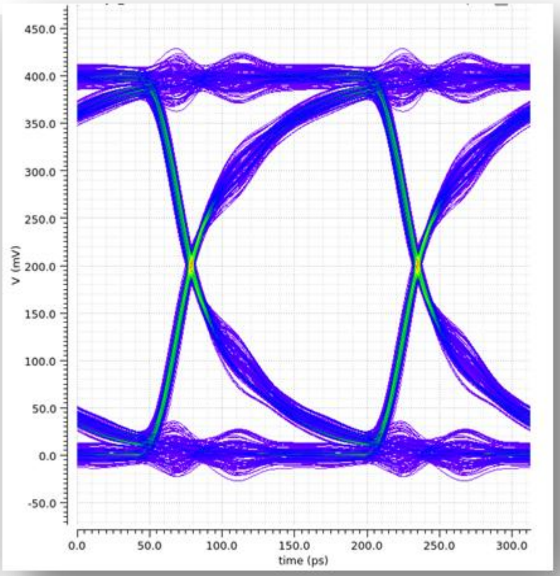
2.5D Systems – Signal Integrity (SI)

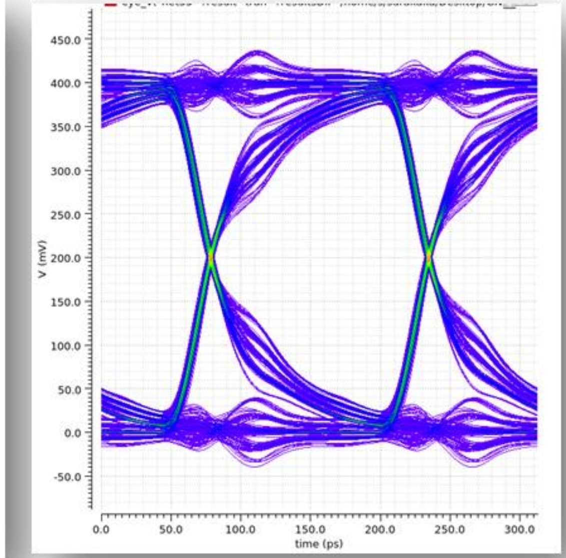








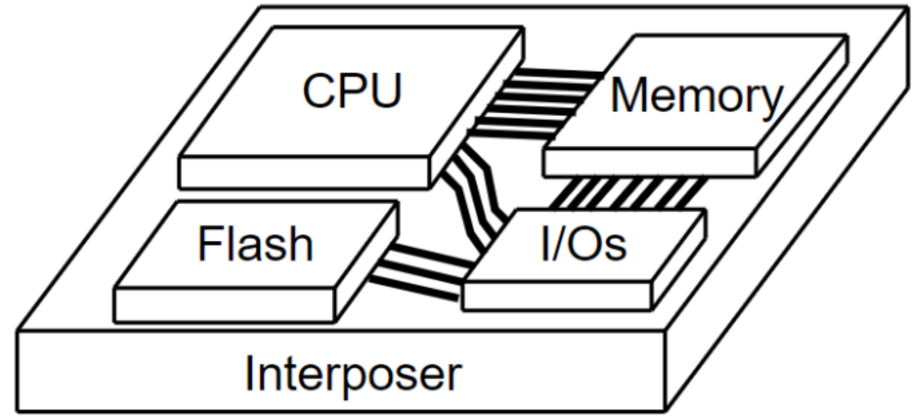


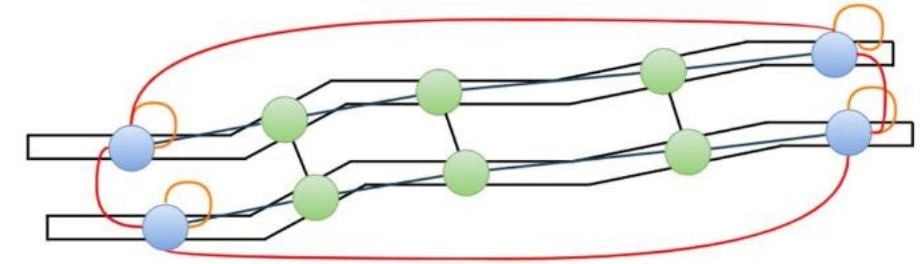


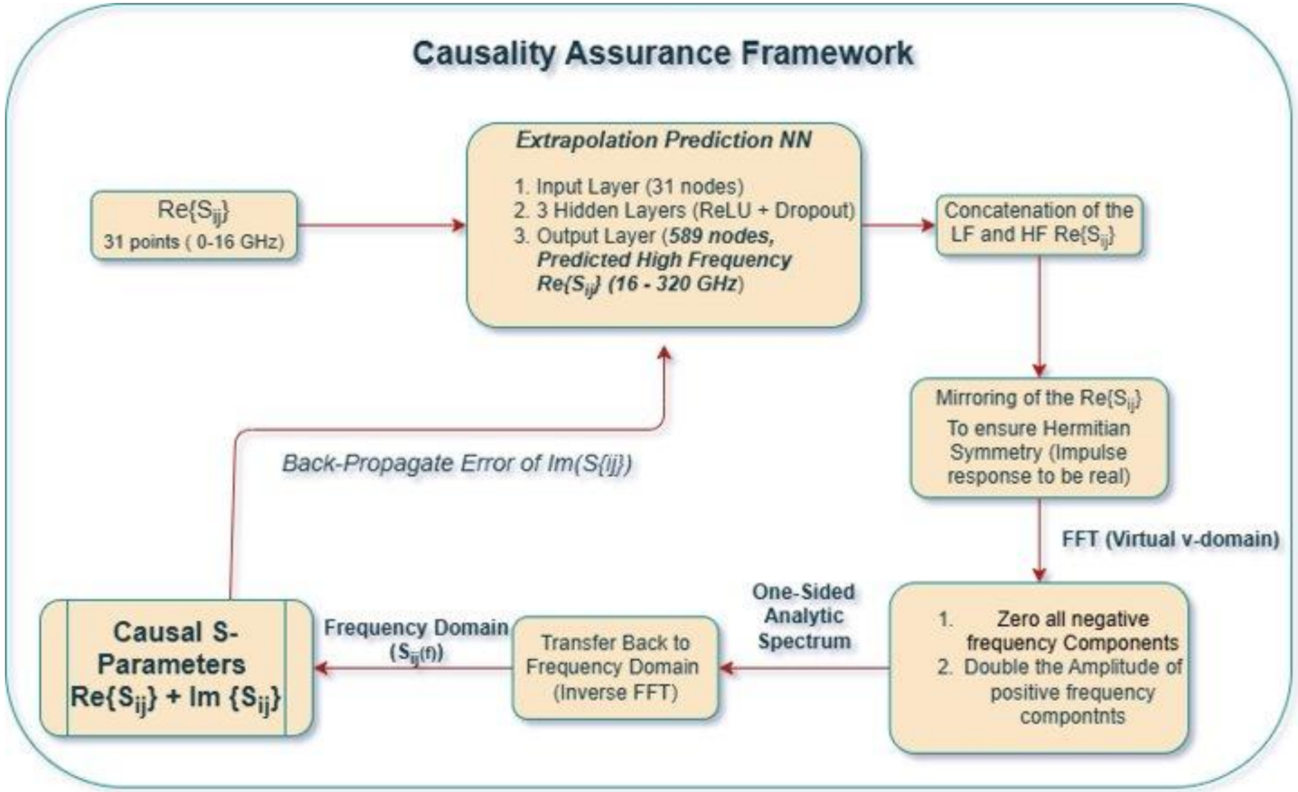
Silicon Interposer design and evaluation automation flows incorporating EM tools and ML techniques

2.5D Systems – Signal Integrity (SI)

Causal and Passive S-parameter estimation using Neural Networks

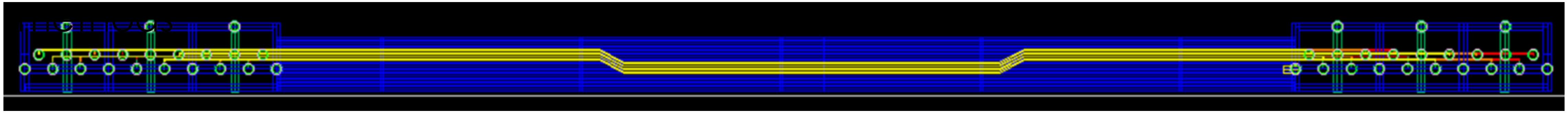




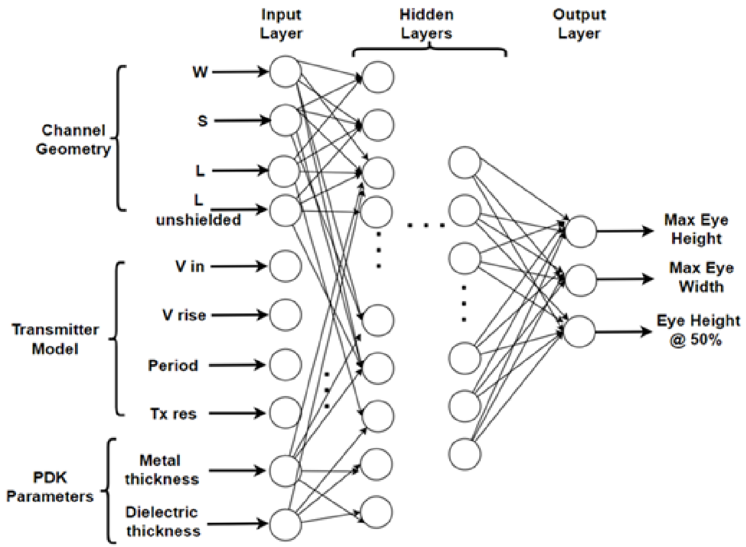


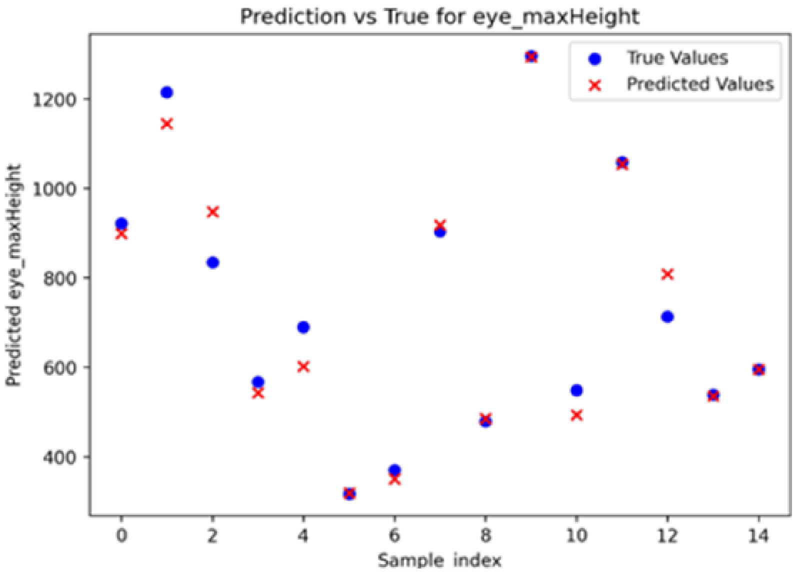
2.5D Systems – Signal Integrity (SI)

Fast and accurate SI analysis on silicon interposers with Machine Learning (ML)



- Estimation of eye-diagram metrics by utilizing a Deep Neural Network (DNN)





- Development of ML techniques and Neural Networks (NNs) to accelerate EM simulations