Electrical simulation and S-parameter measurements of all-silicon CMOS monolithic pixel modules

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Silicon pixel detectors offer high spatial and temporal resolution with a low material budget. Traditional multi-chip modules add material through bump-bonding, flexible PCBs, cooling, and support structures. A new approach explores post-processing monolithic wafers with redistribution layers interconnecting multiple chips, enabling thin and lightweight structures based on low-power monolithic CMOS sensors.

A current concept used in all-silicon modules foresees four future-generation monolithic active pixel sensors (MAPS) in a row, which reduces component count and supports low-material designs suitable for future collider environments. The research focuses on the electrical performance of the signal and data interconnections at high transmission speeds. Current structures target the first use-cases, lower speeds up to 320Mbps, but want to push as much as possible to at least 1Gbps, more if possible. Prototype measurements covering impedance, signal integrity, S-parameters, and electrical simulations of differential trace geometry, dielectric layers, and vias are used to optimize the design for higher data-rate operation.