Universität Siegen
HEP Experimental High Energy Physics
CPPS Center for Particle Physics Siegen

All-Silicon Meeting

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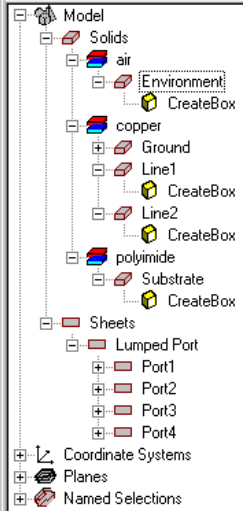
Ansys (HFSS) Simulations of the Surface Differential Line



Ansys
2025 R2

- **Both microstrip excited with 0.5 volts in each and in phase difference of 180deg.**

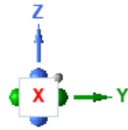
Microstrip

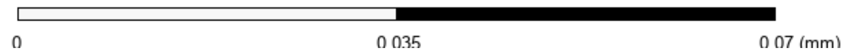
Substrate

Aluminium plane

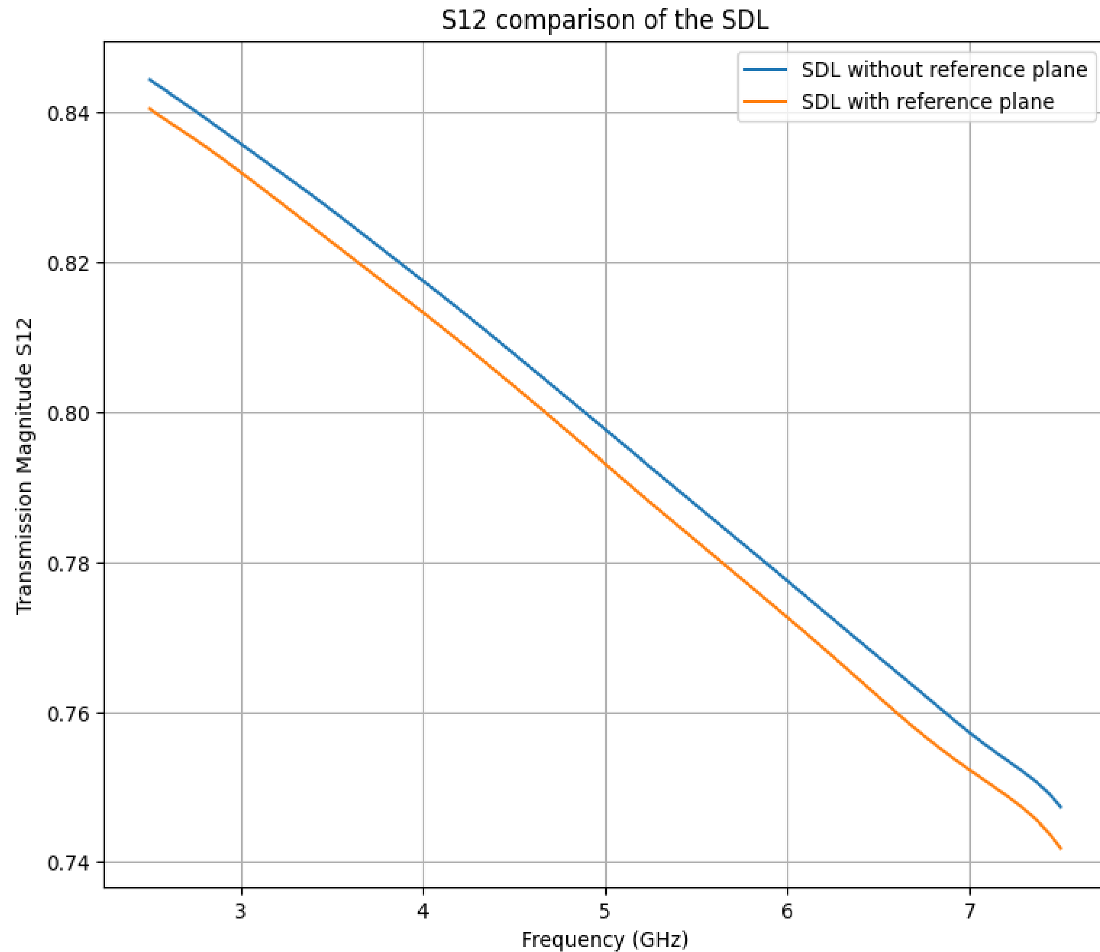
Microstrip Width: 40 µm
Microstrip length: 60 mm
Microstrip Height : 3 µm
Separation: 40 µm

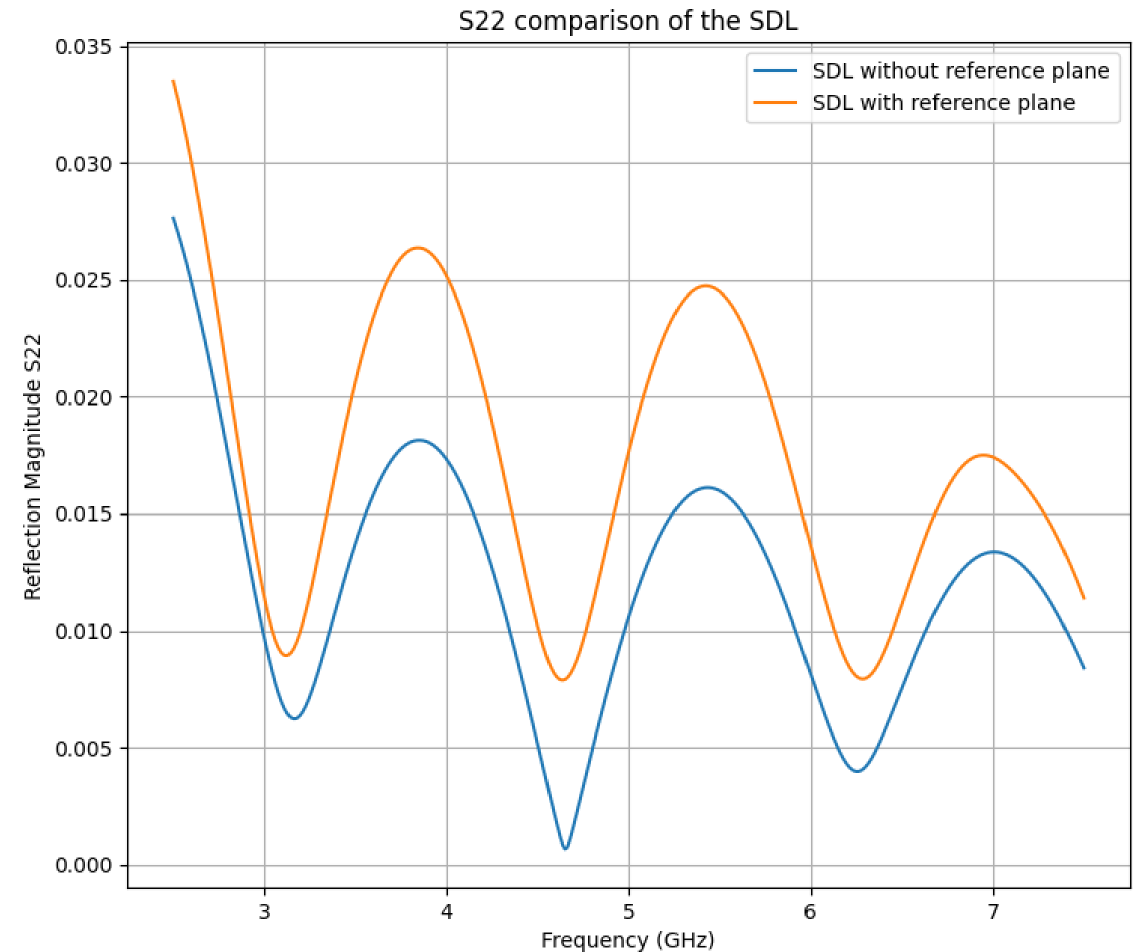
Substrate Height: 24 µm
Differential mode Impedance: 100.07Ω
Common mode Impedance: 55.4Ω
Dielectric Constant: 3.5





Ansys (HFSS) Simulations of the Surface Differential Line





- Copper plane is replaced with an aluminium plane, and the differential lines have no reference plane

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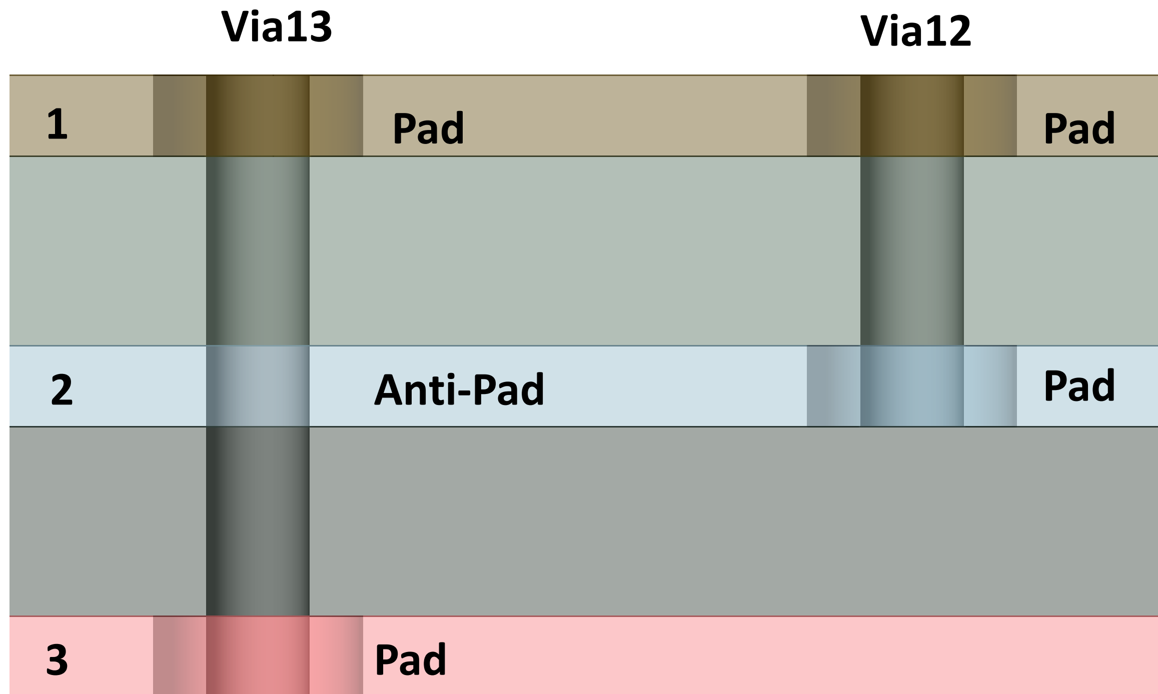
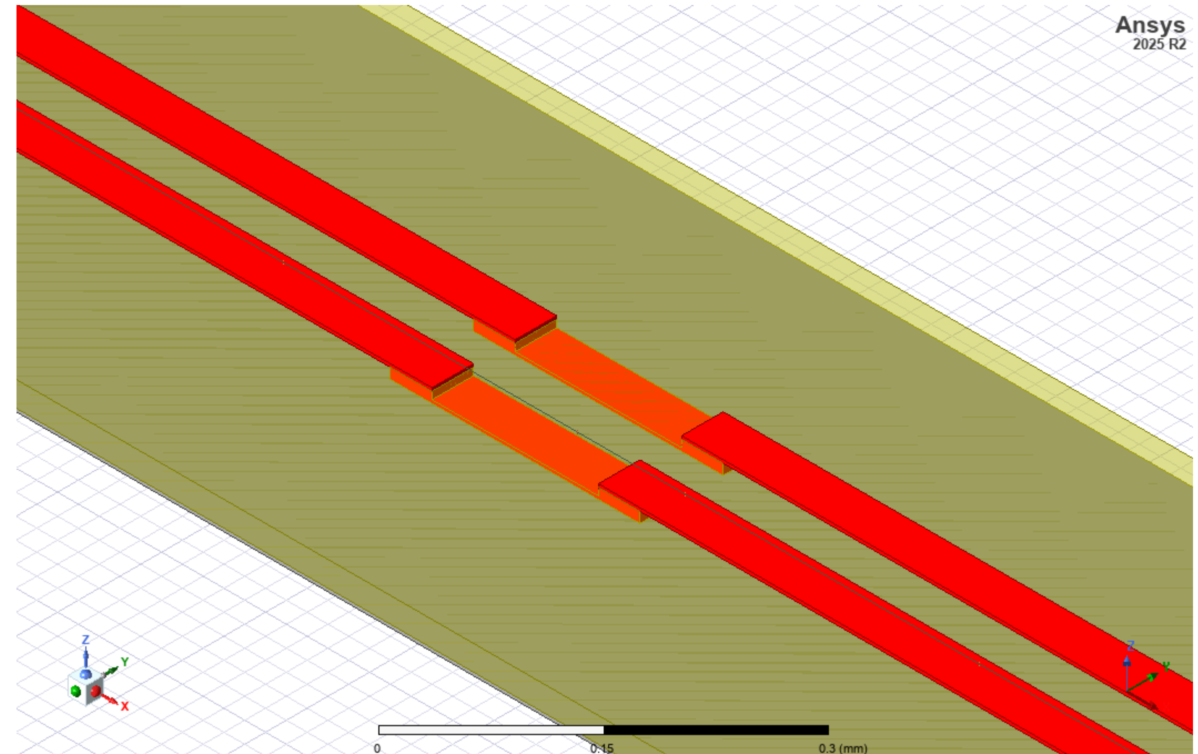
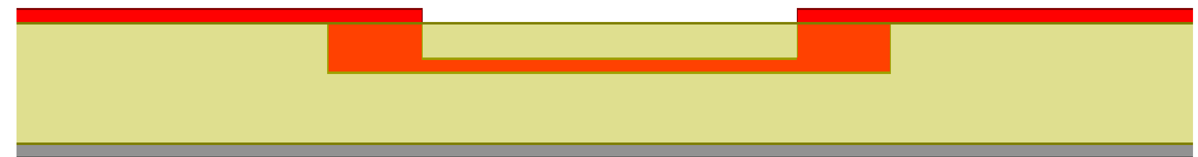
Ansys (HFSS) Simulations of Vias with SDL



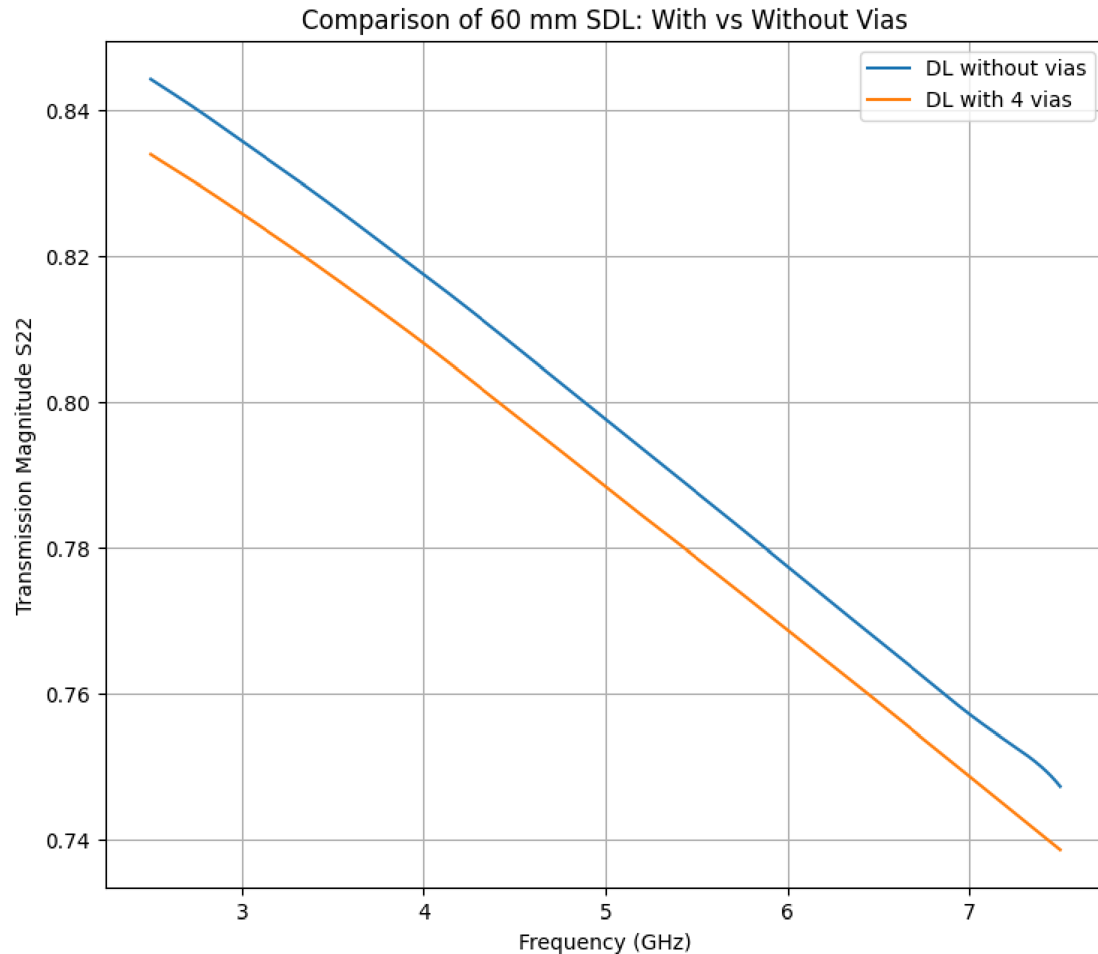


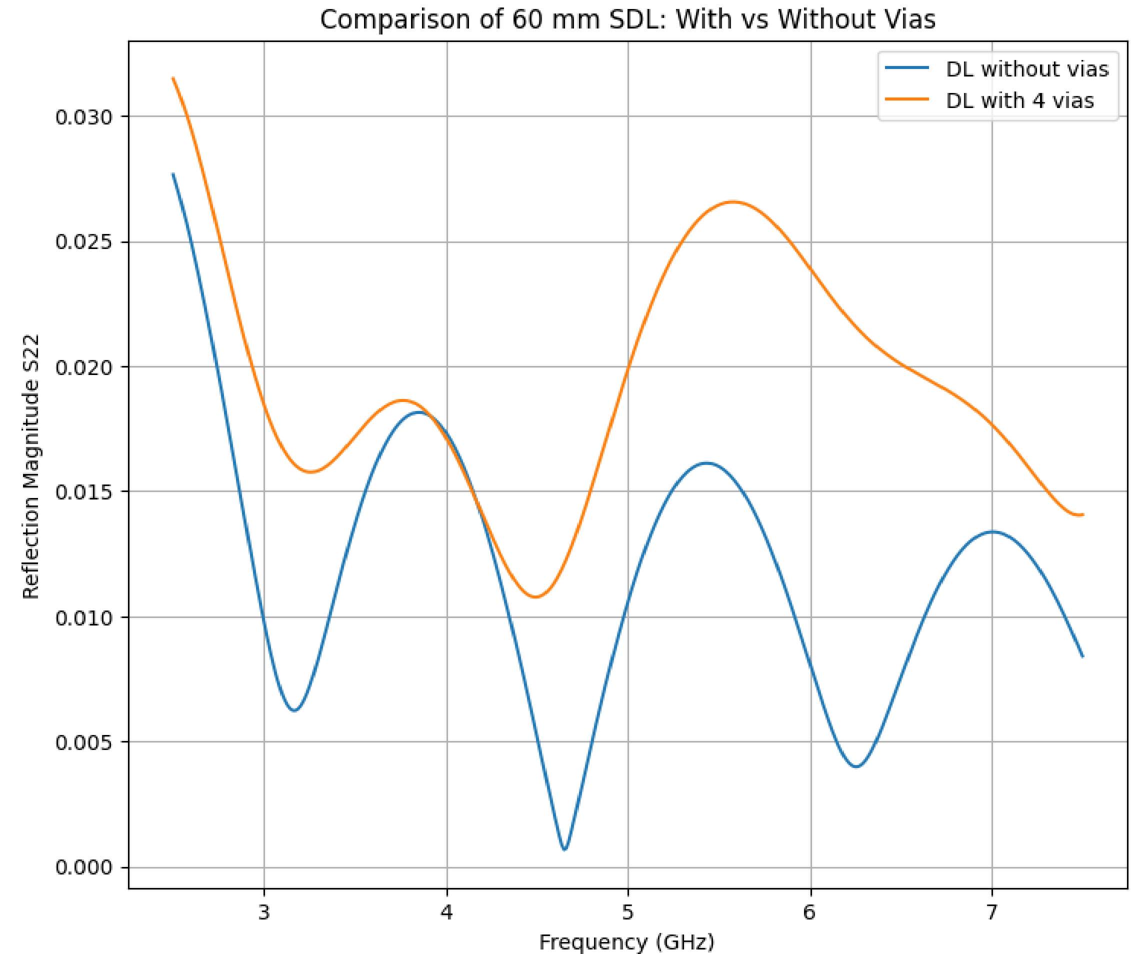


❖ Industry used drilled Vias with Pads (Connectors) and Anti-Pads (Isolators)

❖ Vias used in All-Silicon without drilling can be compared to microstrip changing metal layers

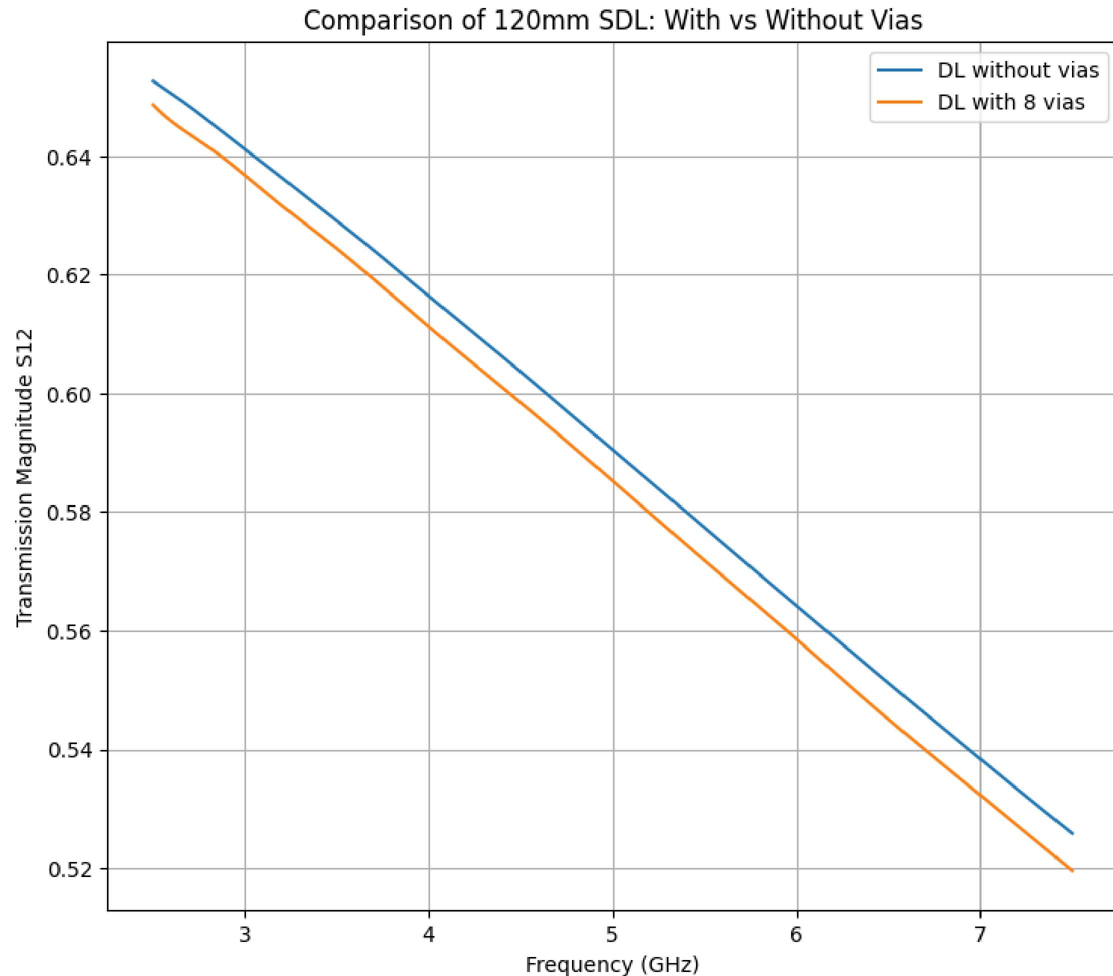
Ansys (HFSS) Simulations of Vias with SDL

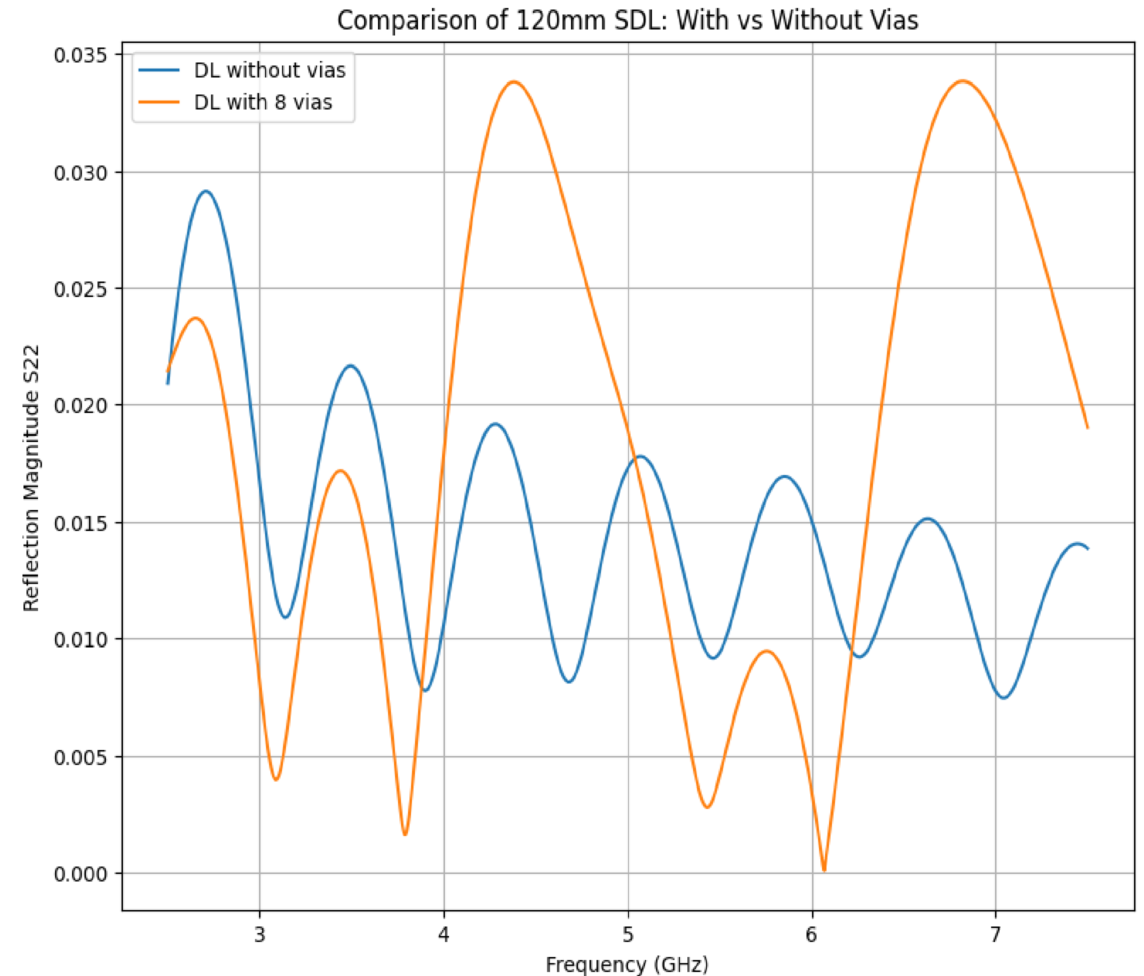




- 60 mm long SDL has two vias in each microstrip; the distance between the two vias is 200 um according to the design of the all-silicon ladder

Ansys (HFSS) Simulations of Vias with SDL

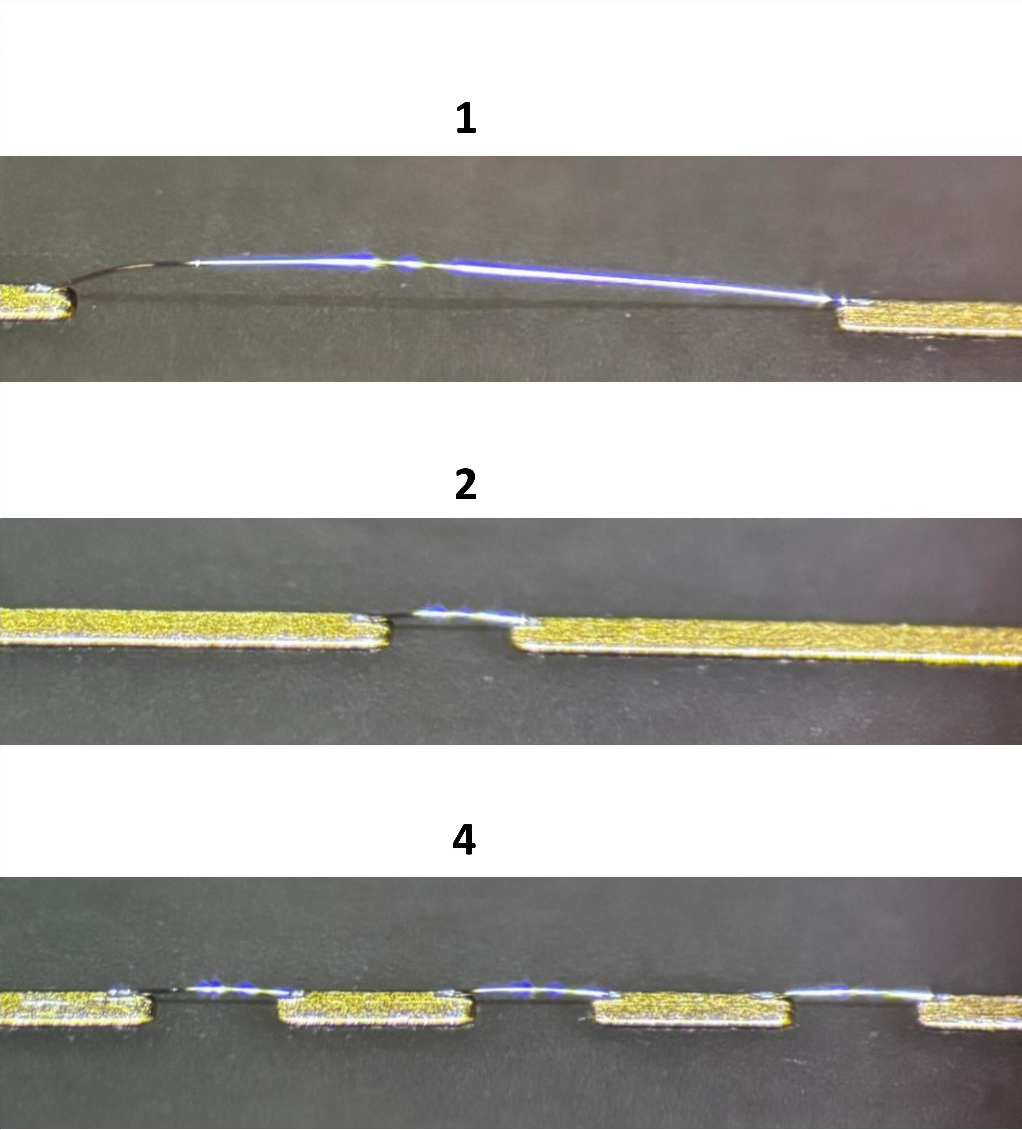




- 120 mm long SDL has two pairs of vias (a total of four) in each microstrip; the distance between the two pairs is 40 mm in this simulation; later, more vias will be added

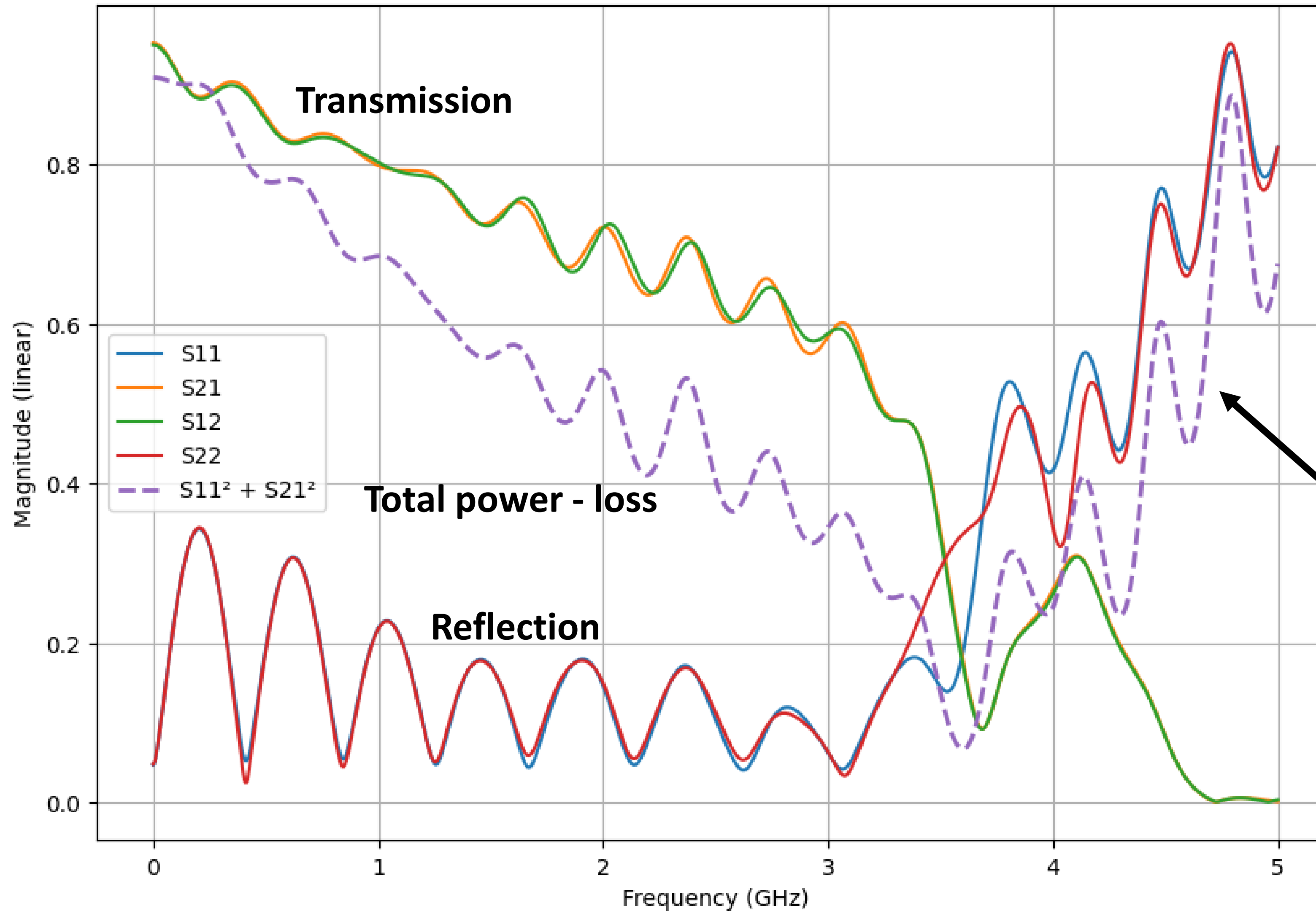
Wire-bonding on Test PCB

1 (4 mm wire-bonds)
2 (0.8 mm wire-bonds)
3 (No wire-bonds)
4 (0.8 mm wire-bonds)



S-parameters measurements for Line-1

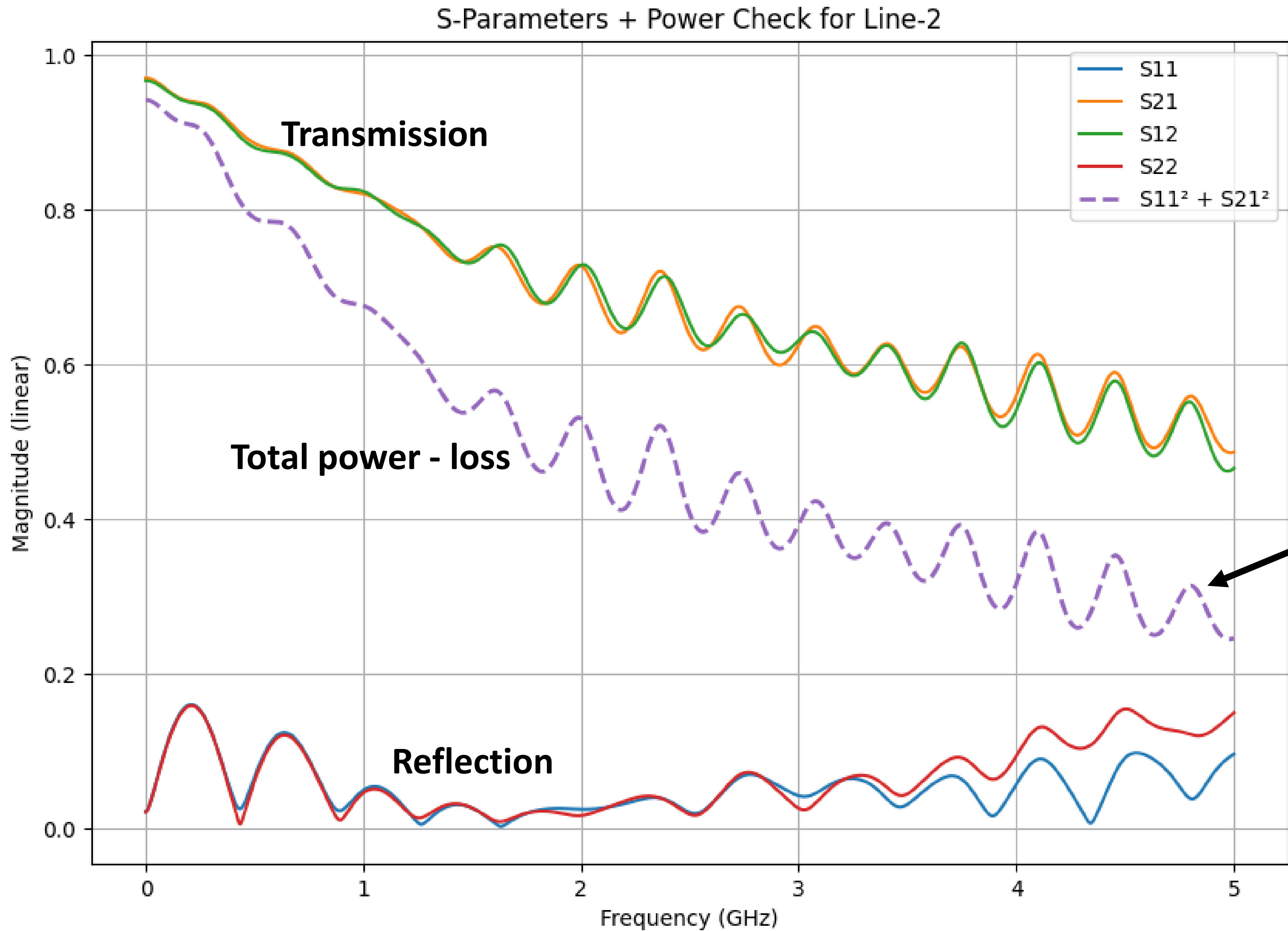
Where did the missing power go?
It is dissipated as:
•**Conductor loss**
•**Dielectric loss**
Radiation loss (especially at discontinuities, bends, wire-bonds)
•**Surface roughness effects**



Input power splits into reflection + transmission + loss

Power conservation check in Line-1 with longer wire-bonds (4 mm)

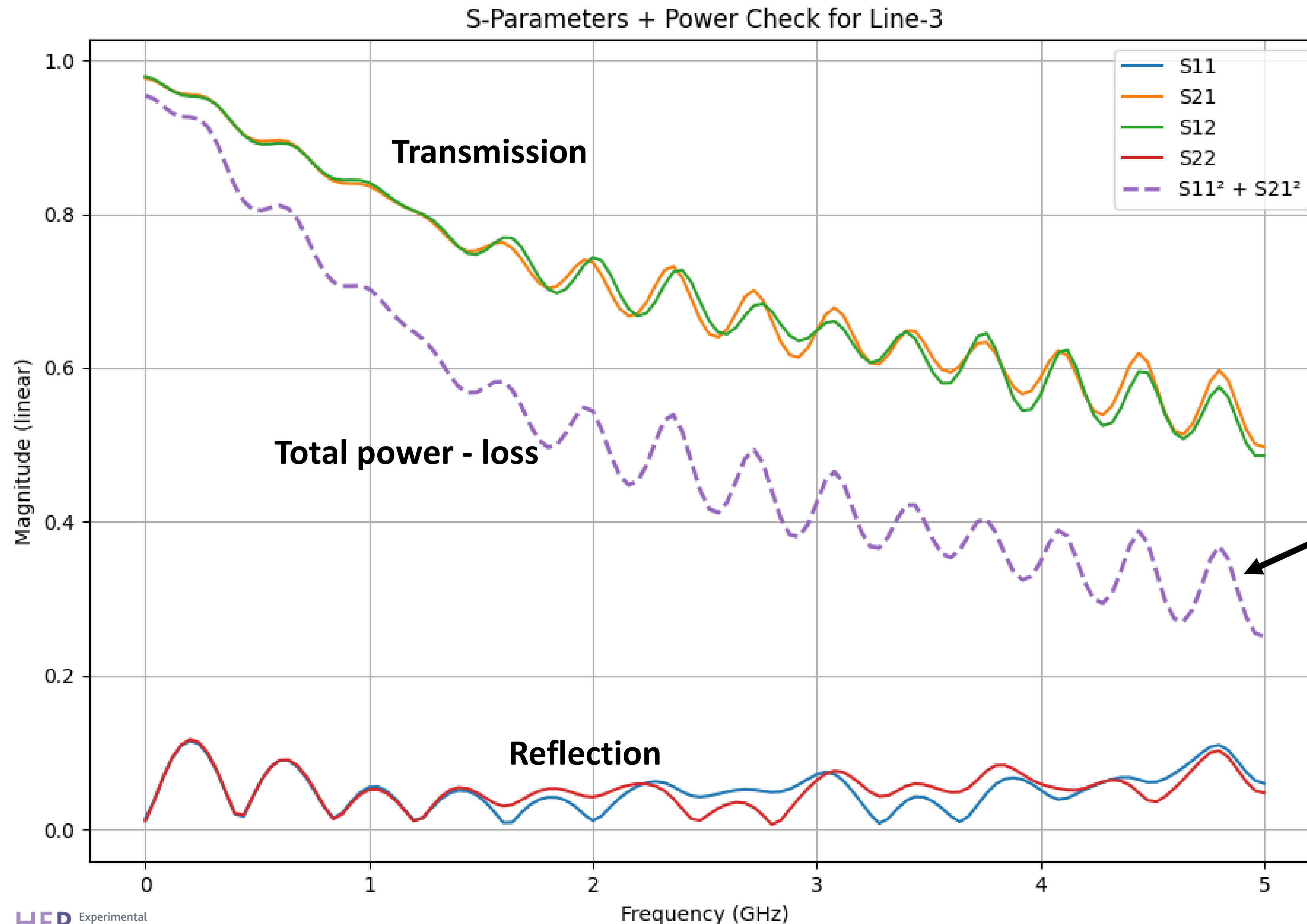
S-parameters measurements for Line-2



Input power splits into reflection + transmission + loss

Power conservation check in Line-2 with short wire-bonds (0.8 mm)

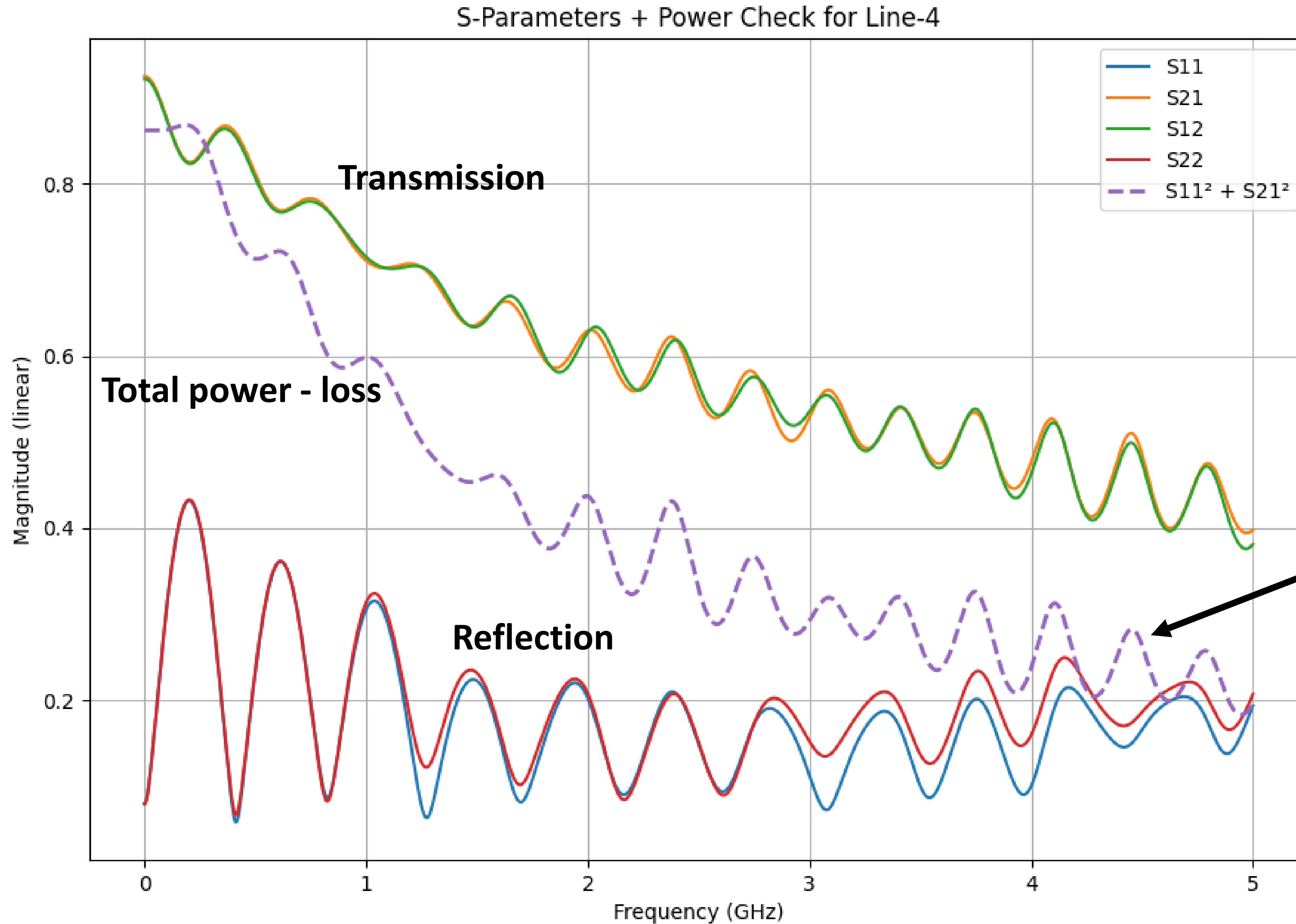
S-parameters measurements for Line-3



Input power splits into reflection + transmission + loss

Power conservation check in Line-3 with no wire-bonds

S-parameters measurements for Line-4



Input power splits into reflection + transmission + loss

Power conservation check in Line-4 with short wire-bonds but more populated wire-bonds (0.8 mm)

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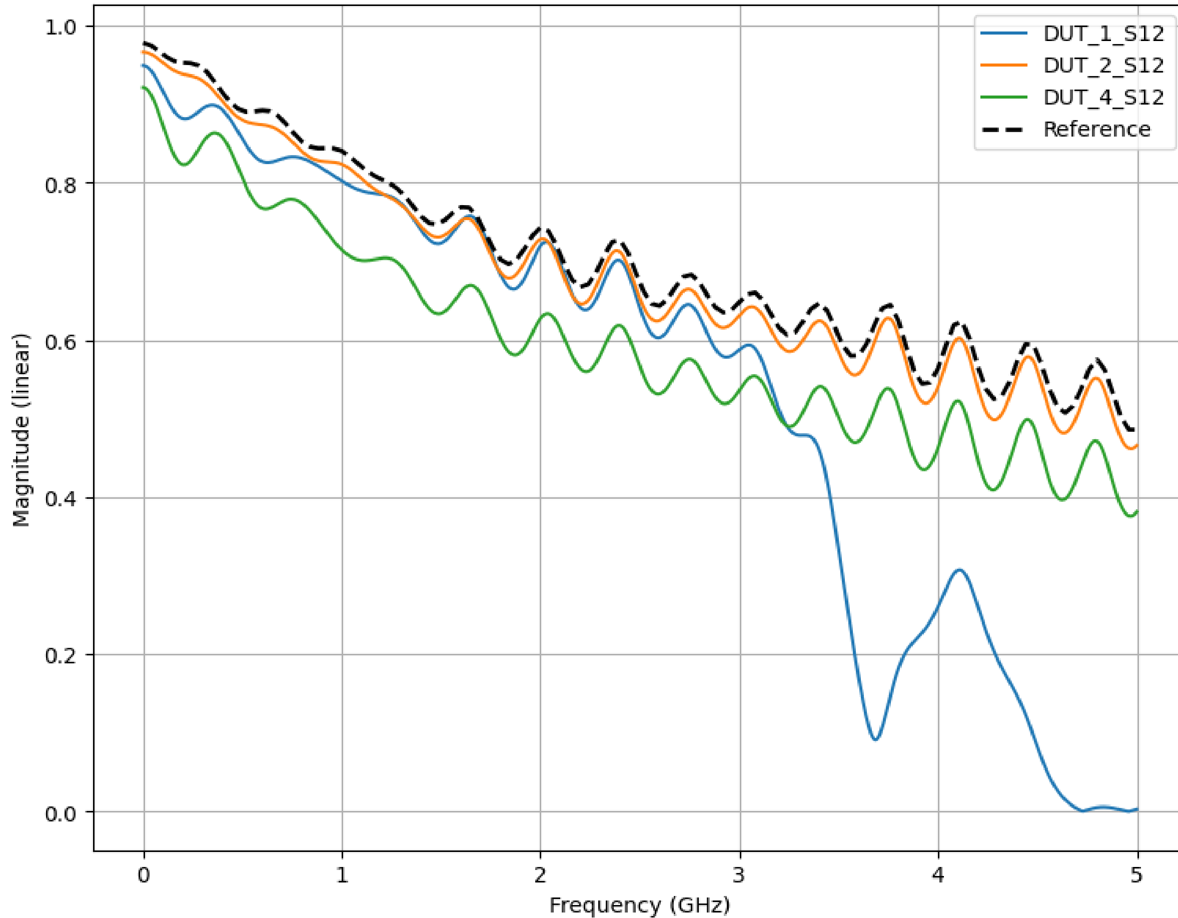
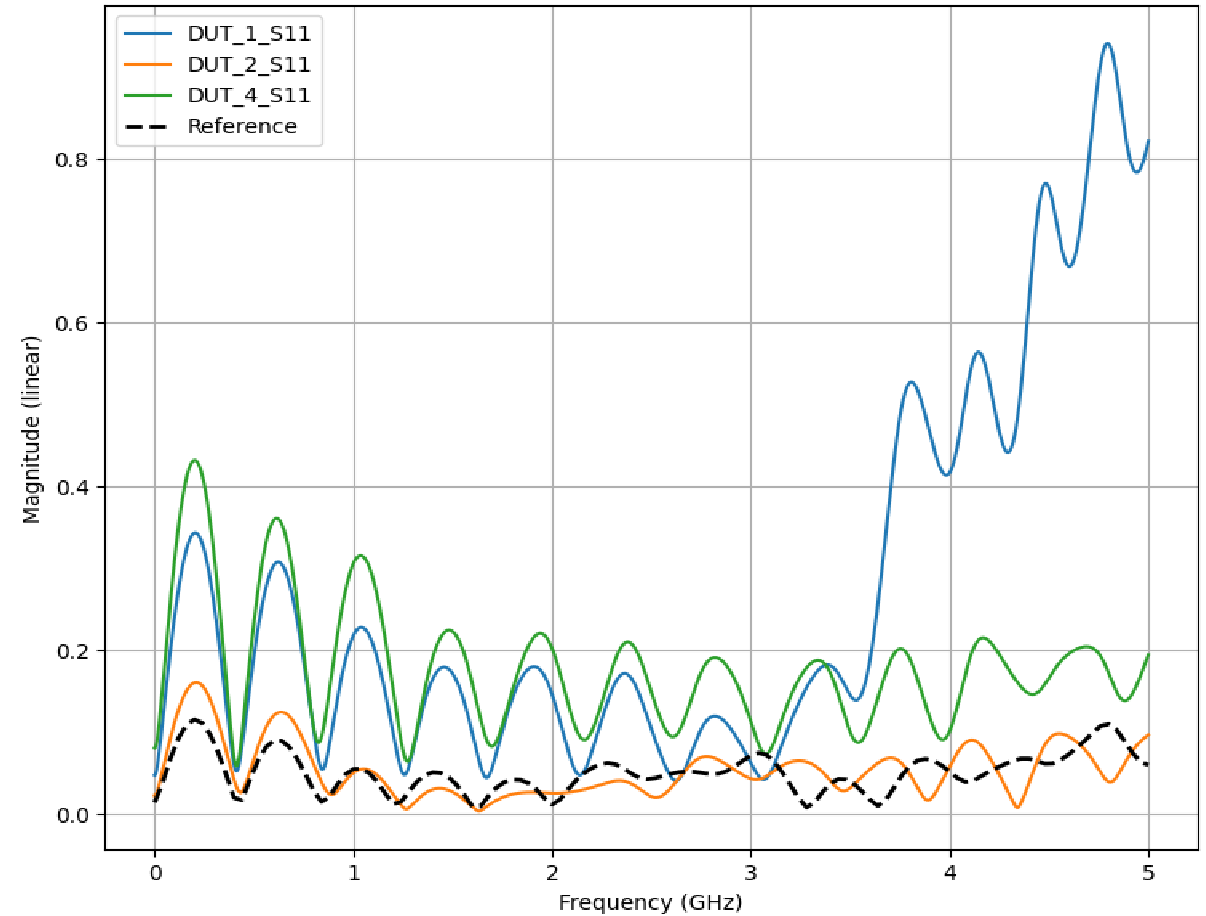
S-parameters comparison all four lines





- Comparison shows that short wire-bonds (0.8 mm) are quite comparable with the reference line, with no wire-bonds, whereas long wire-bonds (4 mm) reflect more data at higher frequency

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Next steps :

- Wire bonding of the differential lines on the wire-bond test PCB
- More simulations of vias, probably with different shapes of vias
- Any suggestions?