

All-Silicon Meeting

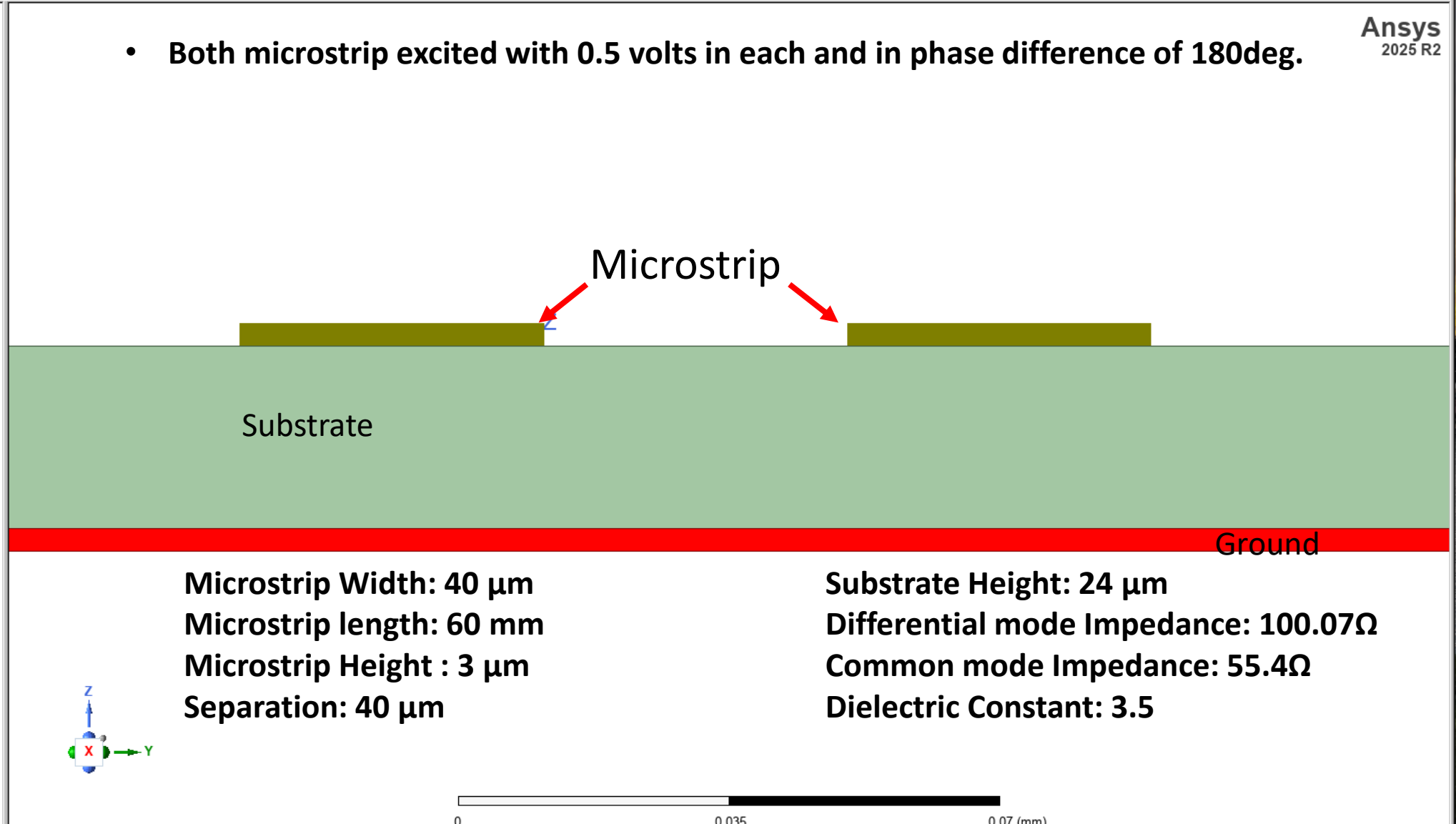
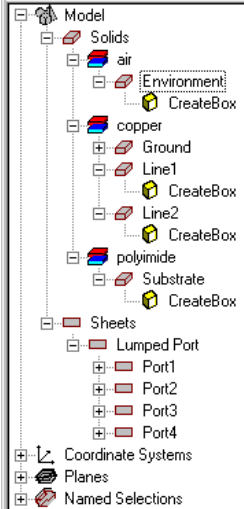
Darshil Vagadiya
With E-lab
02.04.2026

In collaboration with

Ansys (HFSS) Simulations of the Surface Differential Line

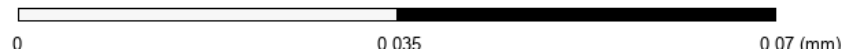
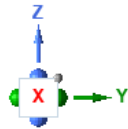
Ansys
2025 R2

- Both microstrip excited with 0.5 volts in each and in phase difference of 180deg.



Microstrip Width: 40 μm
Microstrip length: 60 mm
Microstrip Height : 3 μm
Separation: 40 μm

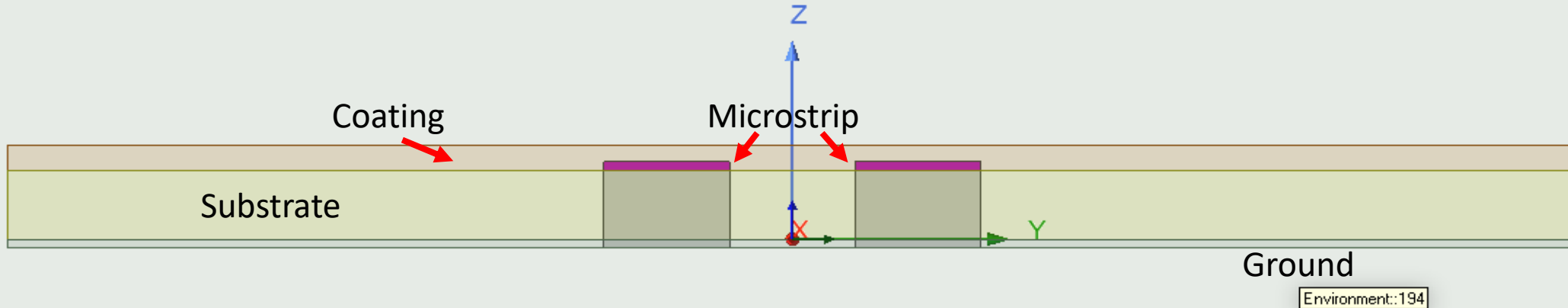
Substrate Height: 24 μm
Differential mode Impedance: 100.07 Ω
Common mode Impedance: 55.4 Ω
Dielectric Constant: 3.5



Ansys (HFSS) Simulations of the Coated Differential Line

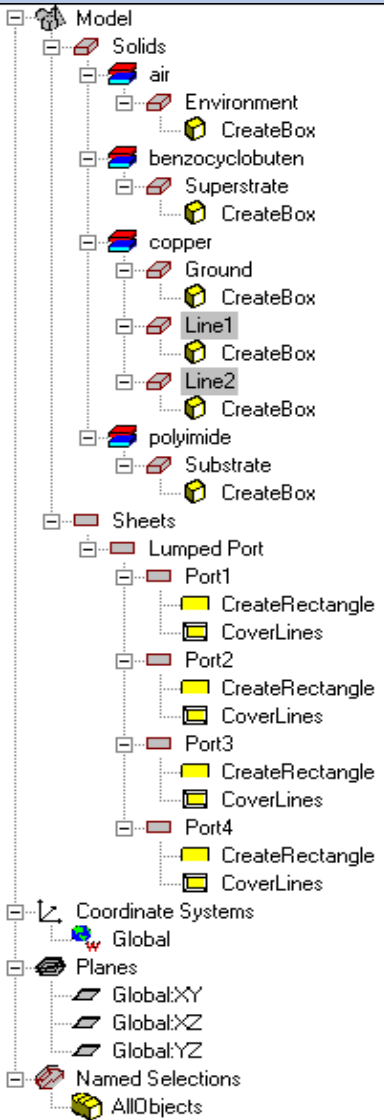
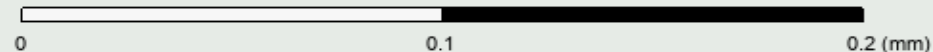
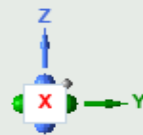
Ansys
2025 R2

- Both microstrip excited with 0.5 volts in each and in phase difference of 180deg.



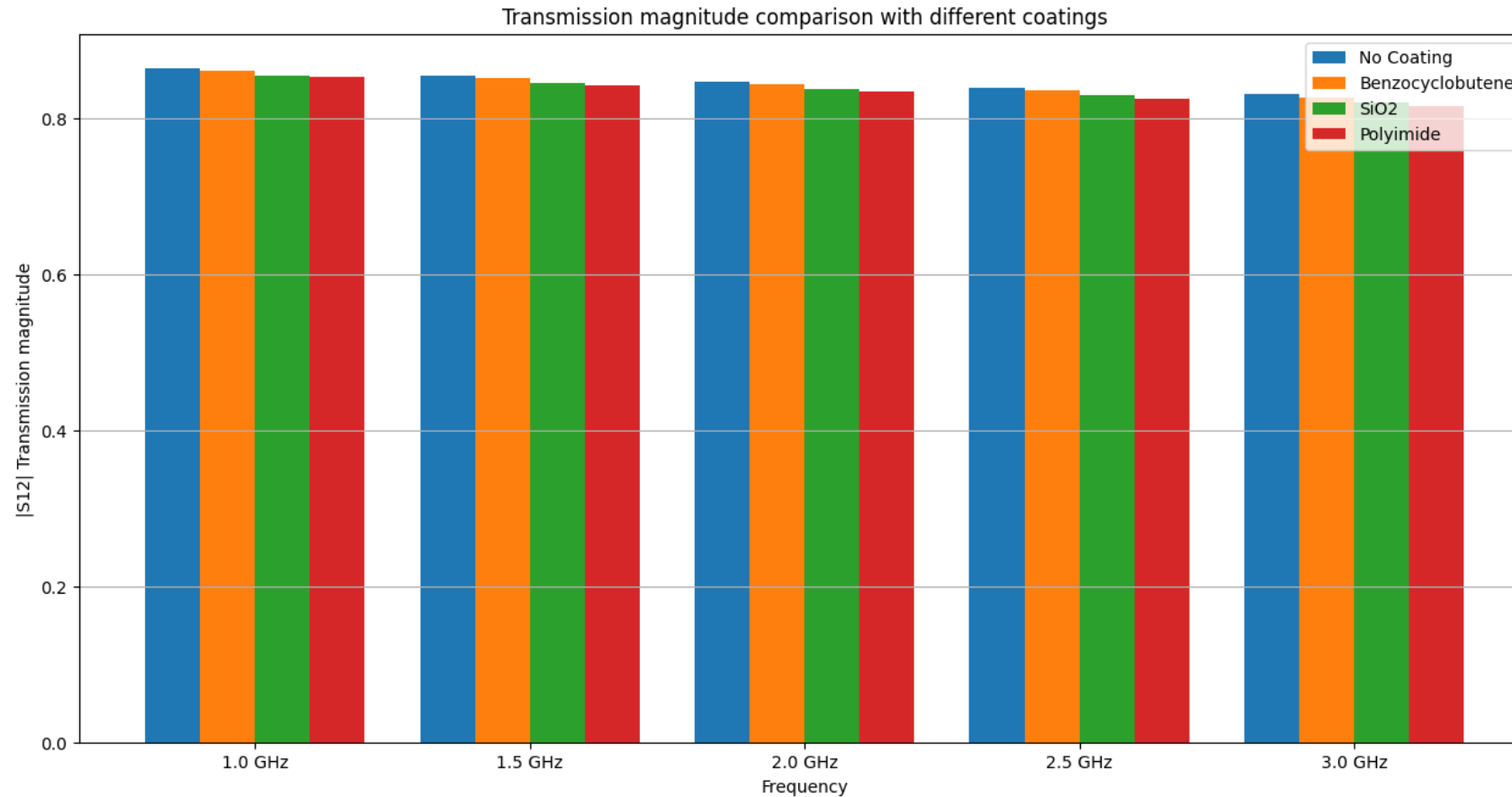
Microstrip Width: 40 μm
Microstrip length: 60 mm
Microstrip Height : 3 μm
Separation: 40 μm
Substrate Height: 24 μm

Coating material: Polyimide
Coating height: 9 μm
Effective coating height: 6 μm
Differential mode Impedance: 95 Ω
Dielectric Constant: 3.5



Results of Ansys Simulations of the Coated SDL

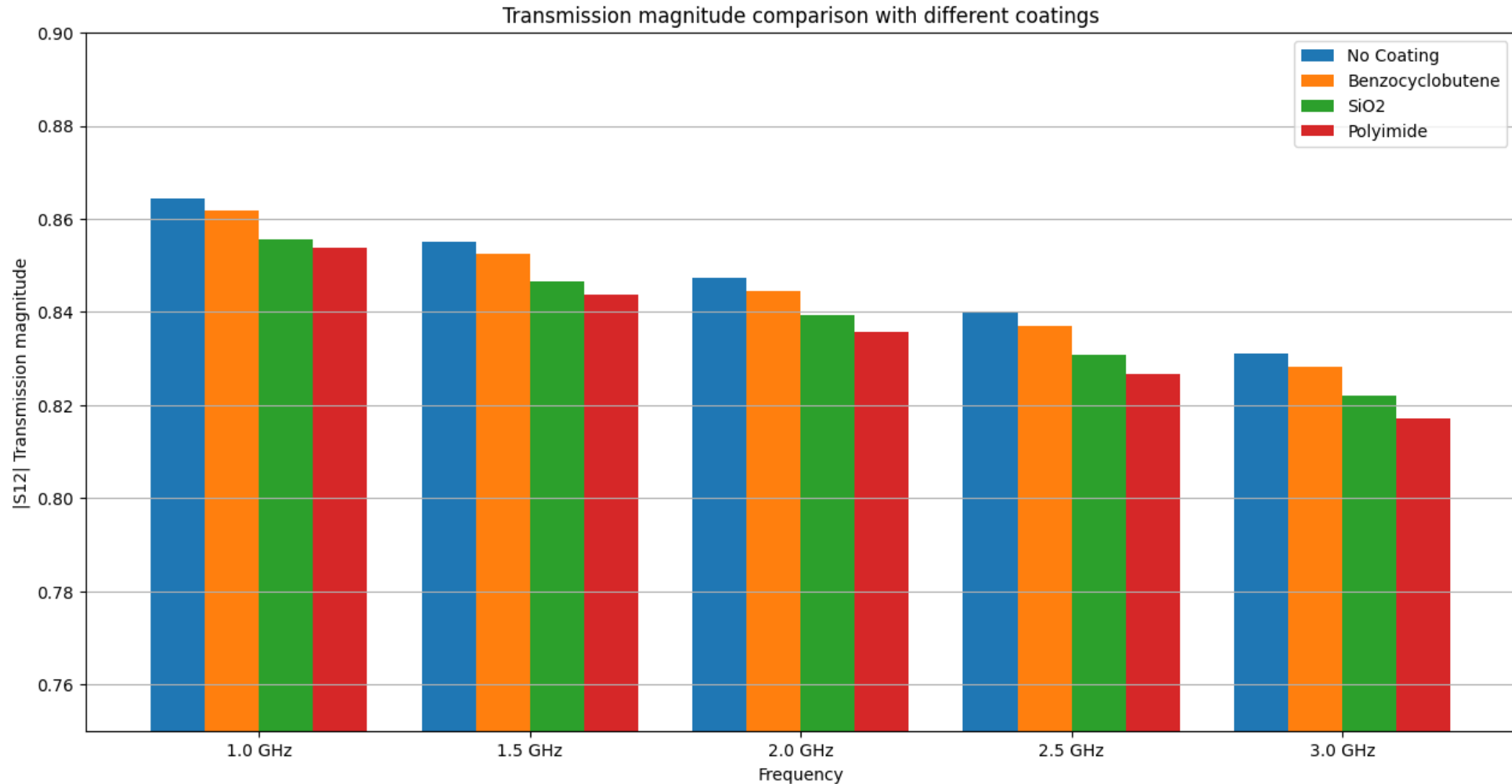
Study of the transmission magnitude as a function of the coating height



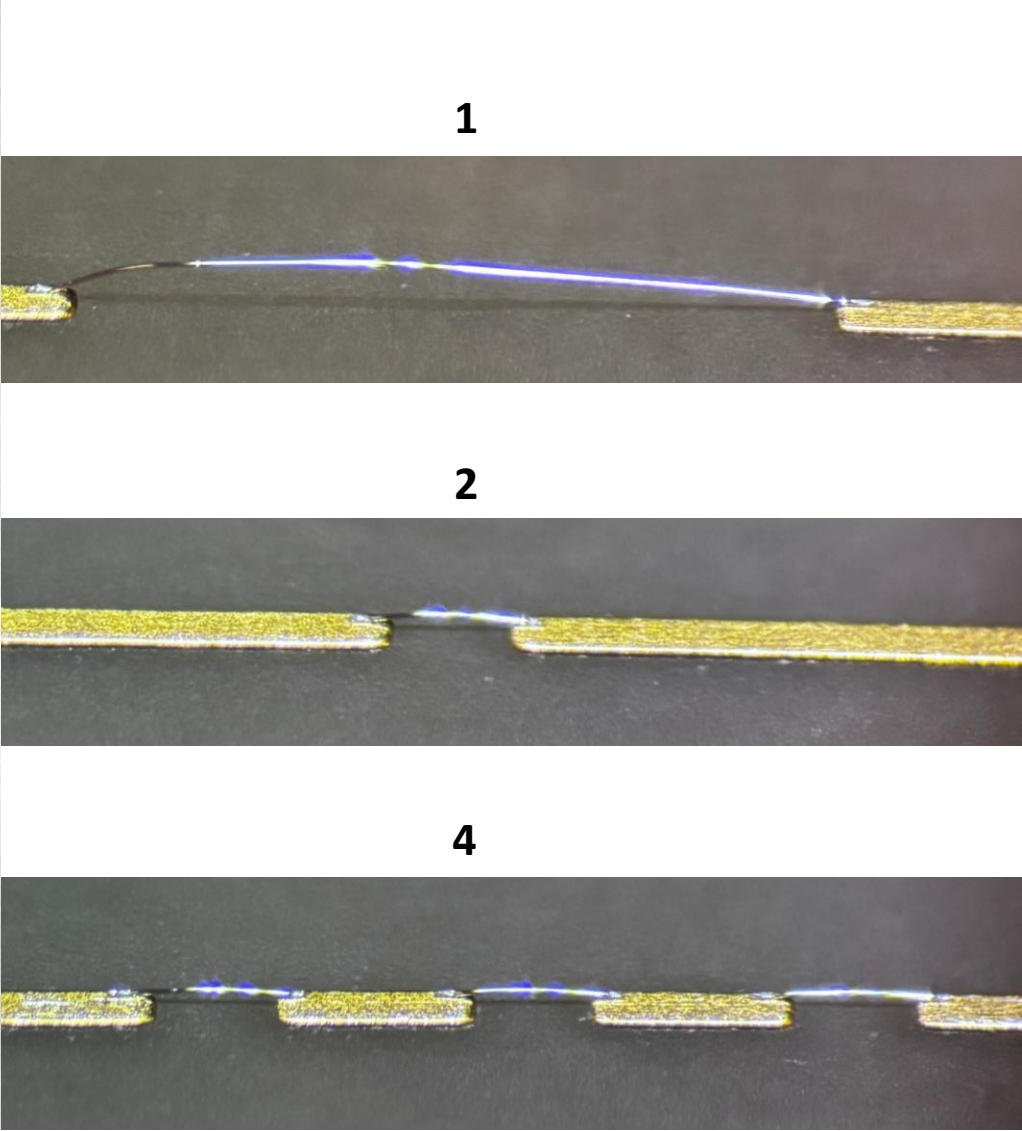
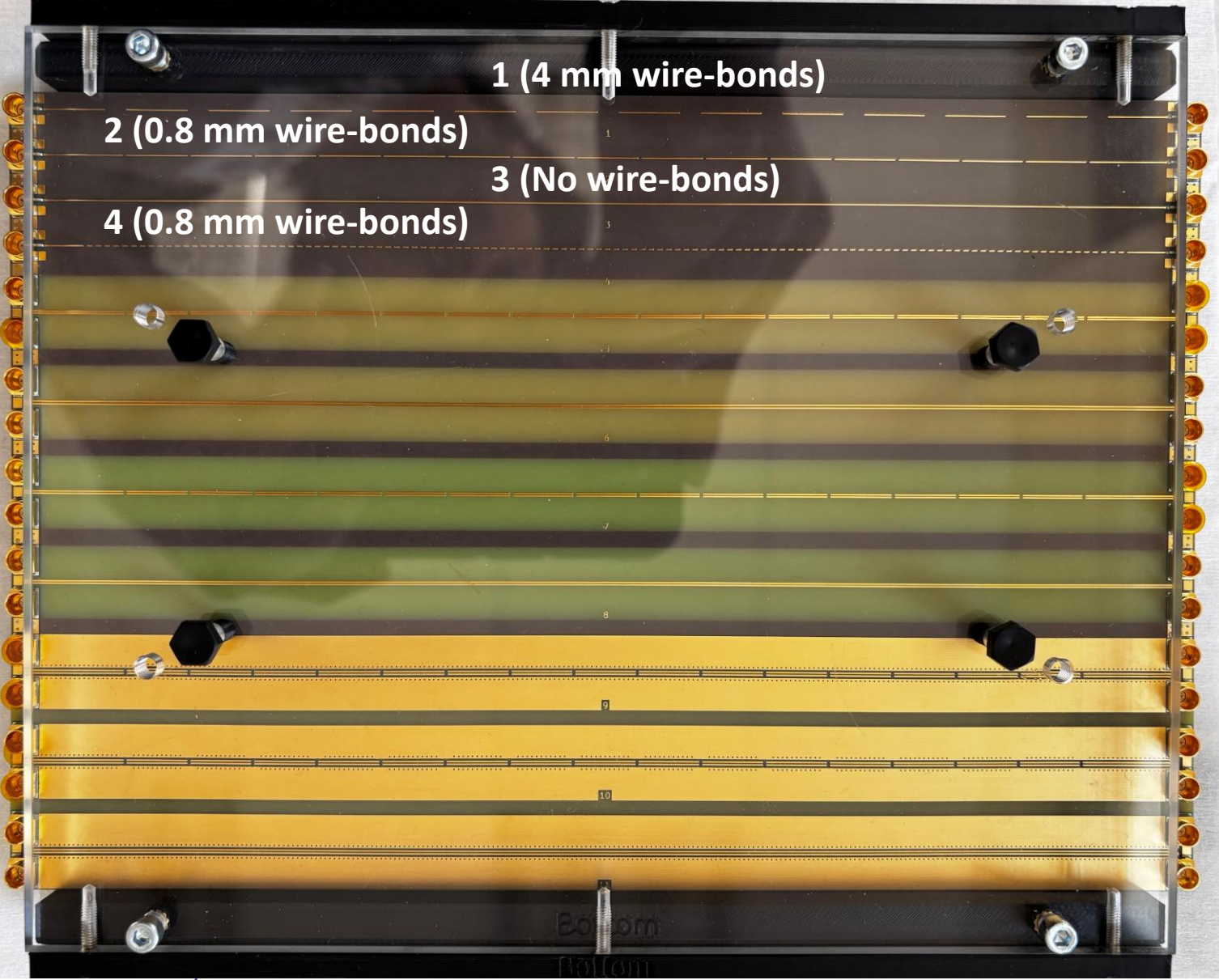
- 3 different coating materials are used.
- In this plot, coating thickness is 7 μm from the substrate height.

Results of Ansys simulations of the coated SDL

Study of the transmission magnitude as a function of the coating height



Wire-bonding on Test PCB



Questions :

- In the IZM structure, what is the reference plane (Ground) for differential lines and Vias?
- Structure of Vias?

Next steps :

- Simulations of vias is in progress; till now, I have not gotten any satisfactory results.
- TDR measurements of wire-bonded lines.