Universität Siegen

HEP Experimental High Energy Physics

CPPS Center for Particle Physics Siegen

All-Silicon Meeting

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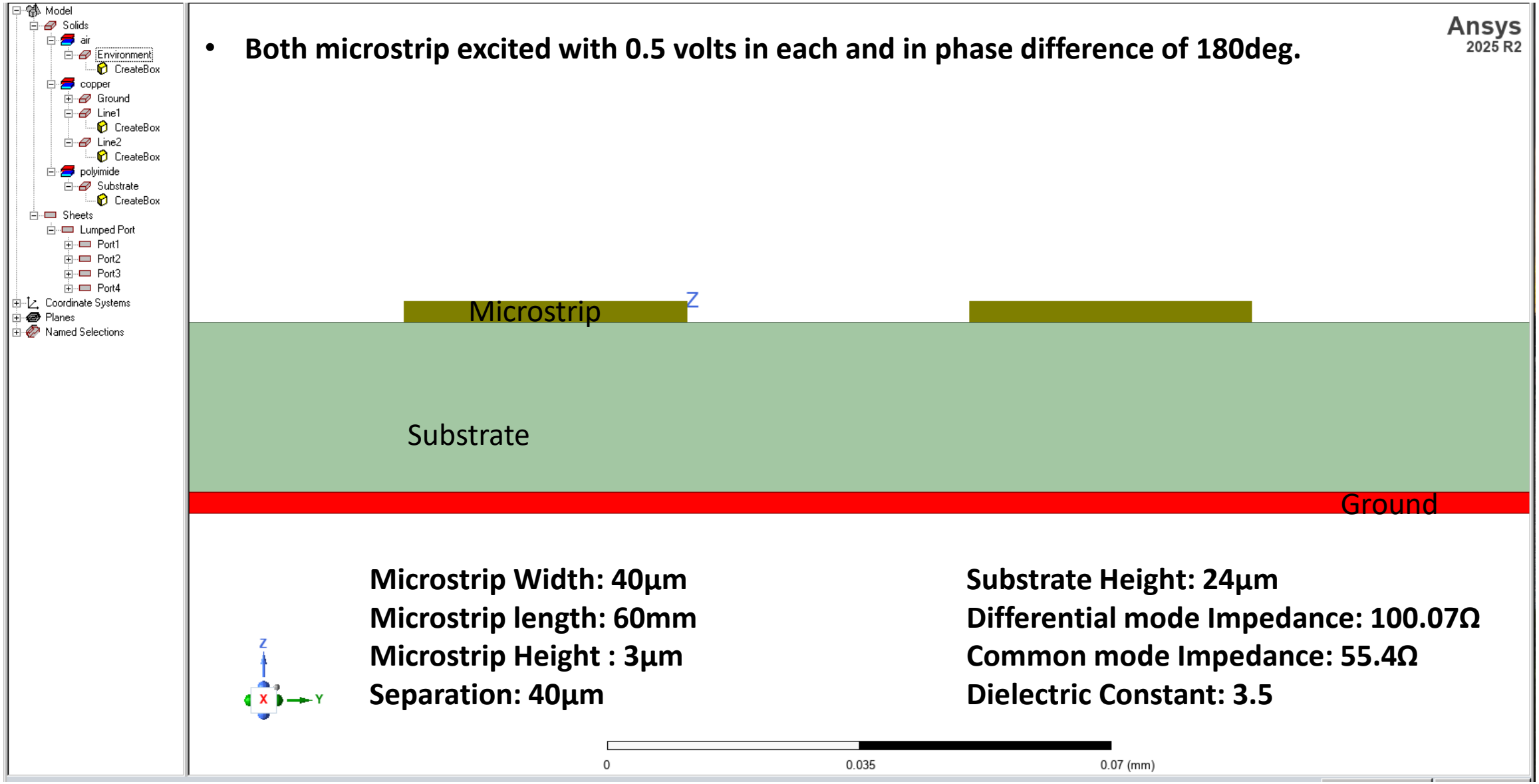
Ansys (HFSS) Simulations of Differential Line

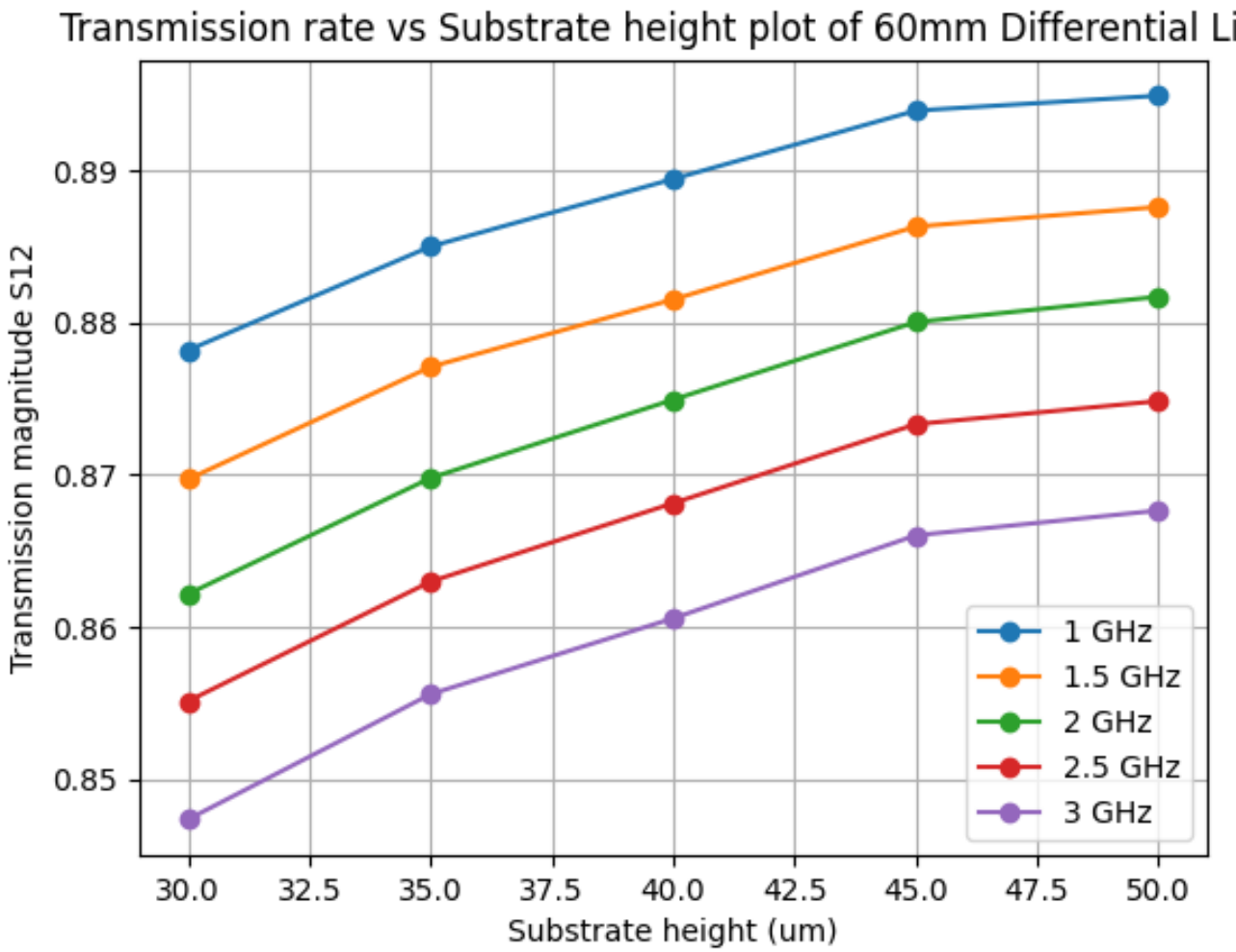


Microstrip Width: 40µm
Microstrip length: 60mm
Microstrip Height : 3µm
Separation: 40µm

Substrate Height: 24µm
Differential mode Impedance: 100.07Ω
Common mode Impedance: 55.4Ω
Dielectric Constant: 3.5

Results of Ansys Simulations of the SDL

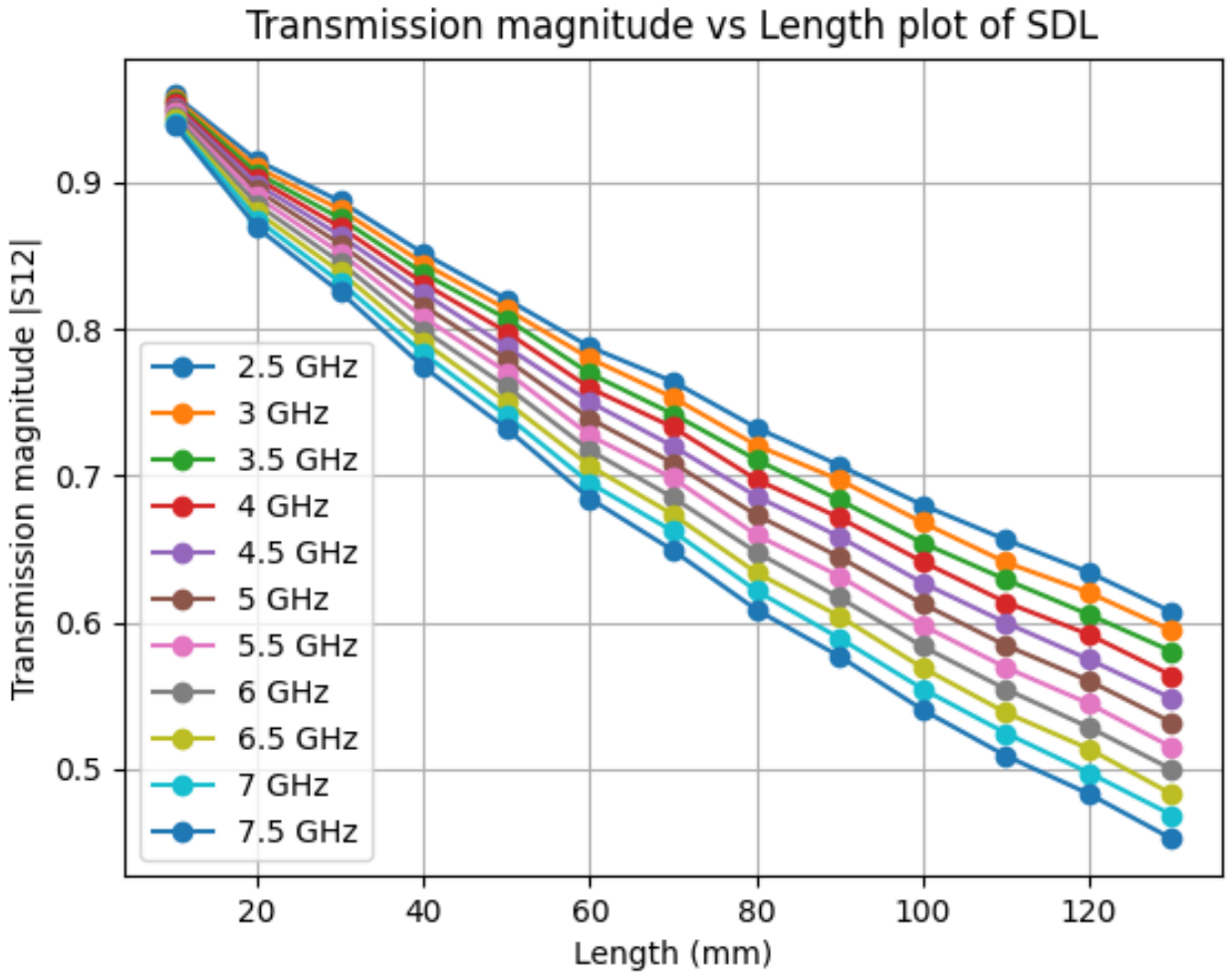
Study of the transmission magnitude as a function of the substrate height



- Frequency range is set to 1GHz to 3GHz.
- Height of substrate varies from 30um to 50um.
- Microstrip length: 60mm
- Microstrip Height : 3µm
- Microstrip width: 40µm
- Each setup is terminated by a corresponding matching resistor.

Results of Ansys simulations of the SDL

Study of the transmission rate as a function of the microstrip length

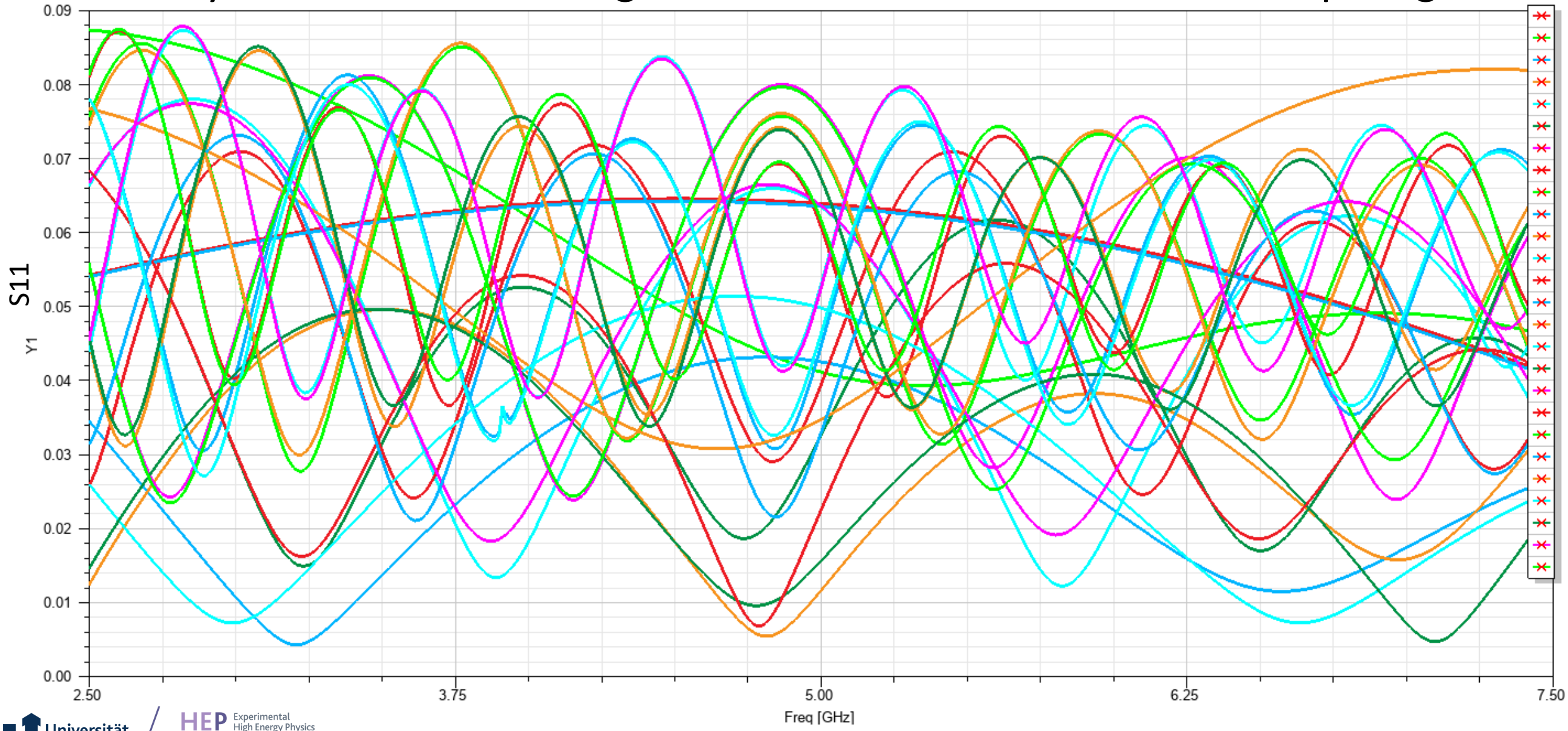


- The length of the microstrip varies from 10mm to 140mm.
- Microstrip width and separation: 20µm
- Microstrip height : 3µm
- Substrate height: 24µm
- Transmission degradation comes from:

$$\alpha = \alpha_c + \alpha_d + \alpha_r$$

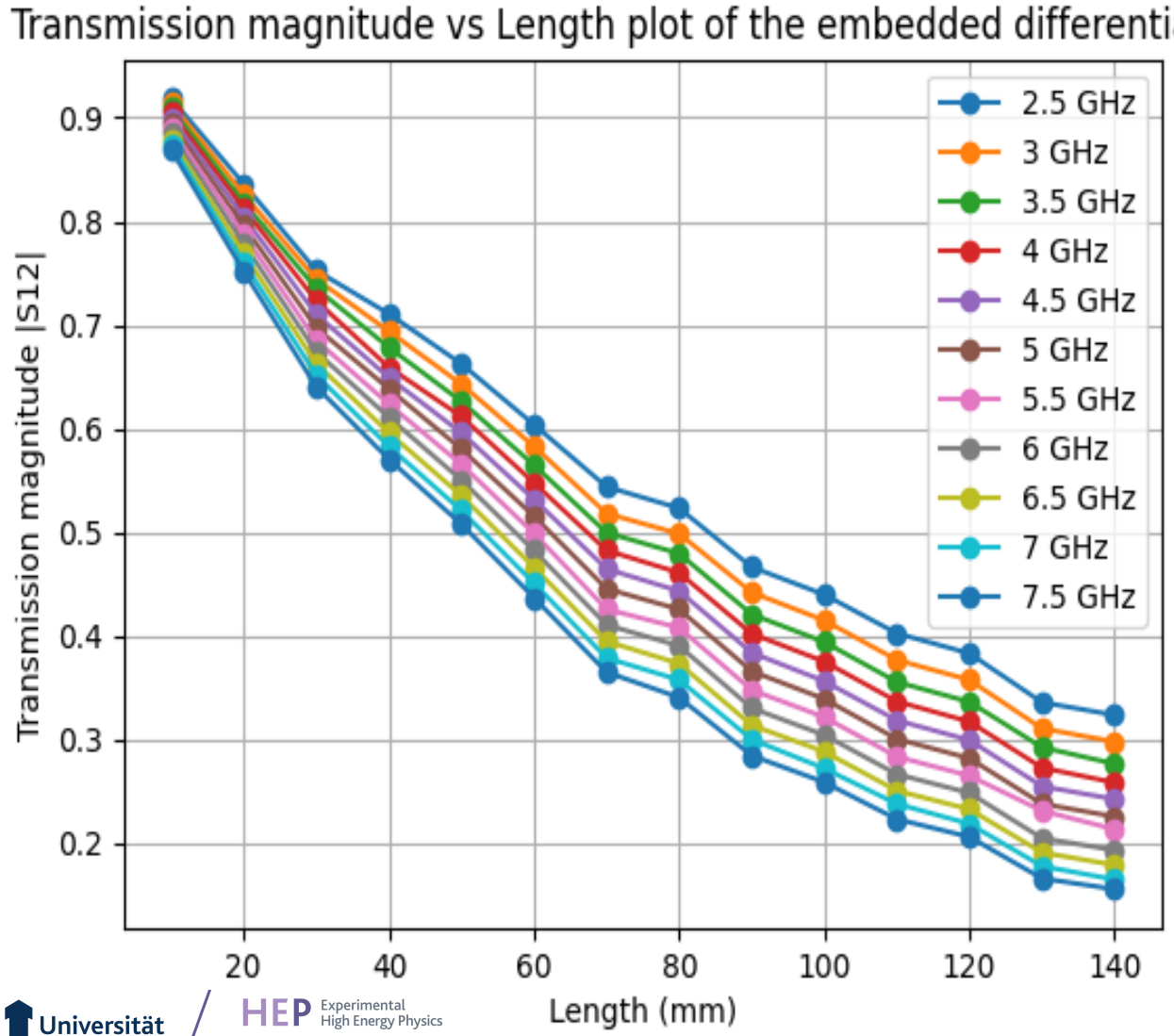
Results of Ansys simulations of the SDL

Study of the reflection magnitude as a function of the microstrip length



Results of Ansys Simulations of the embedded differential Line

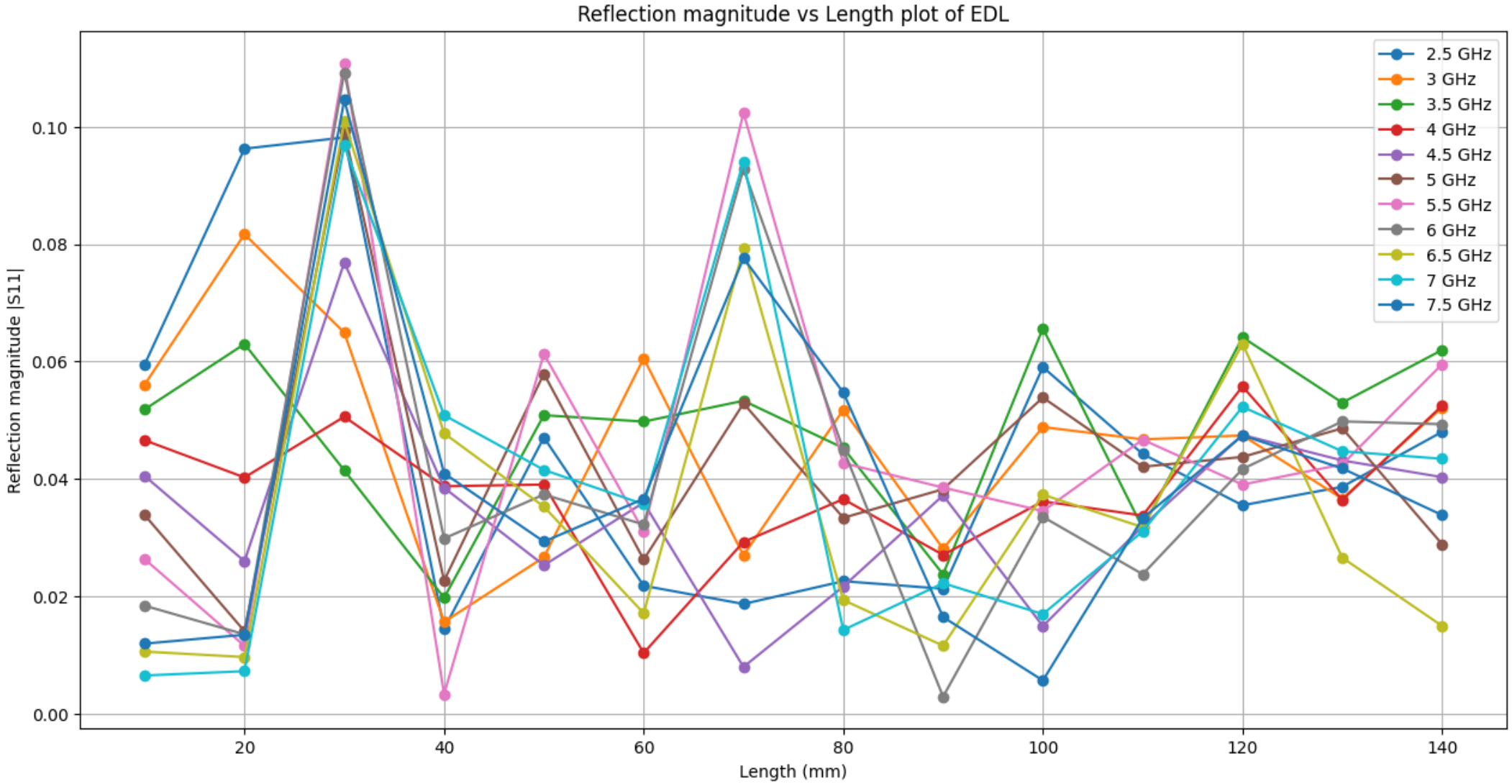
Study of the transmission magnitude as a function of the length of the microstrip



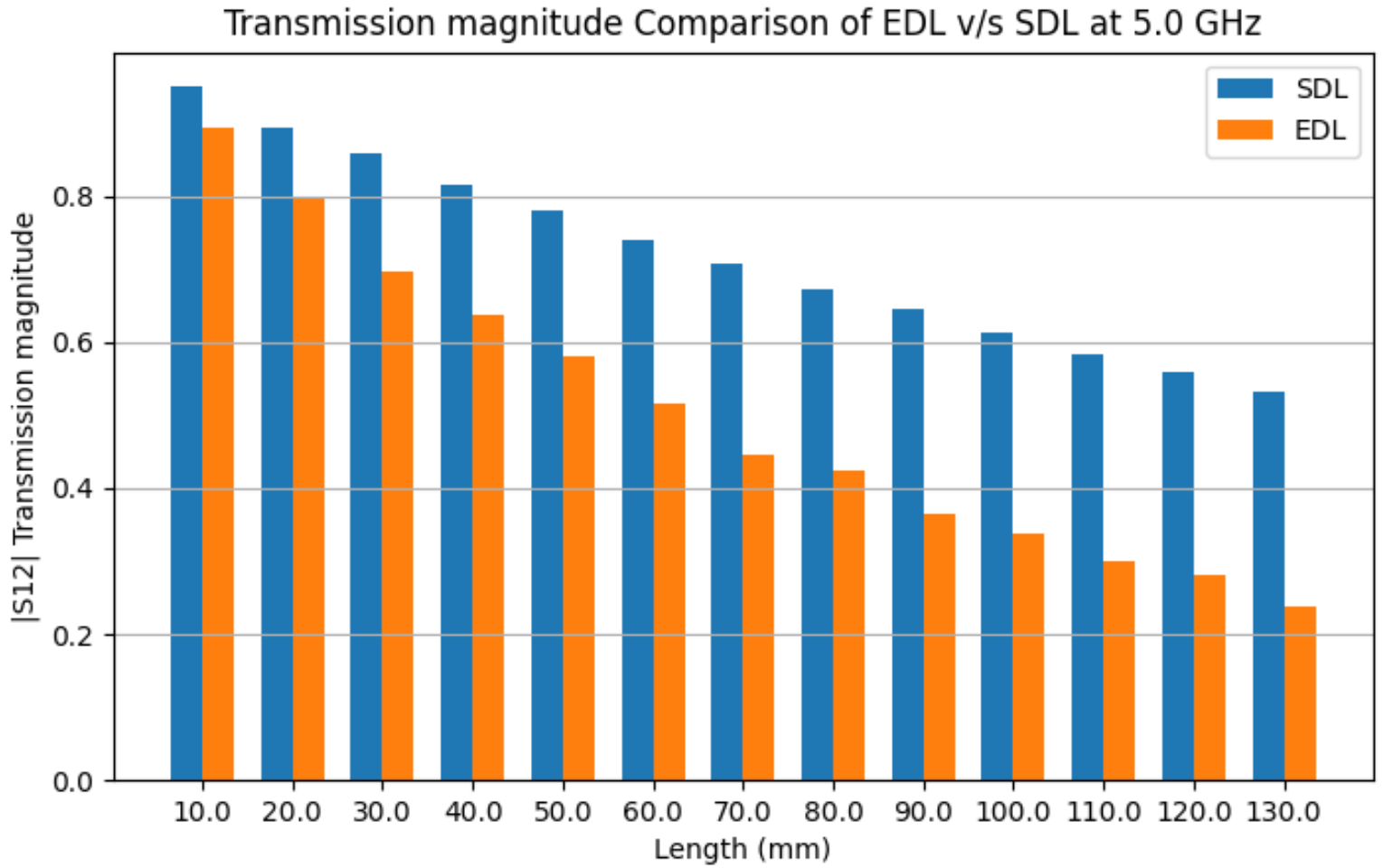
- Frequency range is set to 2.5GHz to 7.5GHz.
- Length of microstrip varies from 10um to 140um.
- Microstrip width: 20mm
- Microstrip height: 3µm
- Substrate height: 23µm

Results of Ansys simulations of the EDL

Study of the reflection magnitude as a function of the microstrip length

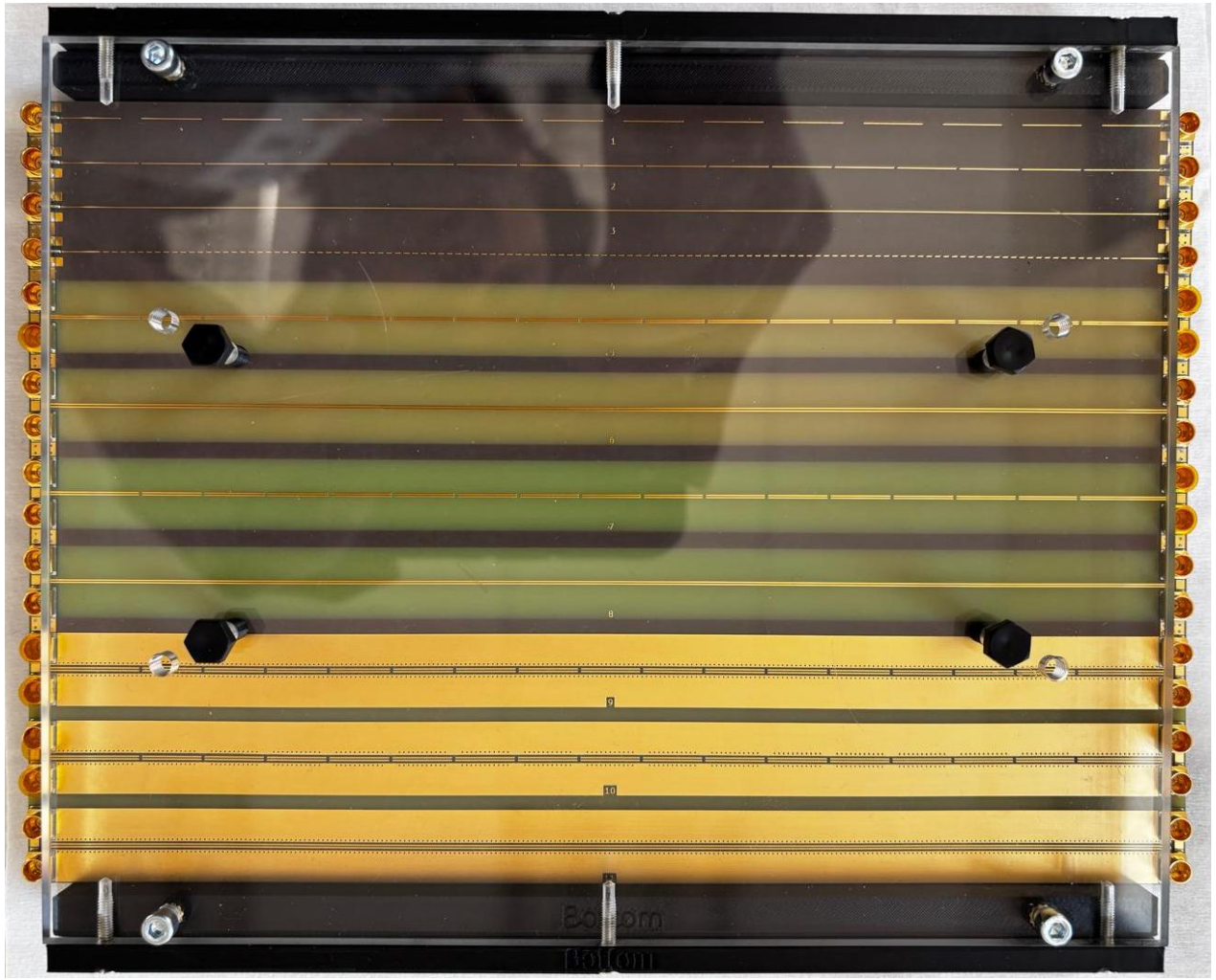


Comparison of the transmission magnitude of EDL and SDL



- Transmission magnitude |S12| of EDL drops faster at larger length.
- EDL can not be used in a chip with long differential lines.

Wire bonding



- The wire bond test pcb is now ready for wire bonding with the protection carrier and lead.

Next steps :

- After DPG:
- Simulation of the asymmetric embedded differential line
- Simulations with other materials as well.
- Wire-bonding and TDR.
- Simulations of vias.

Thank you