Universität Siegen

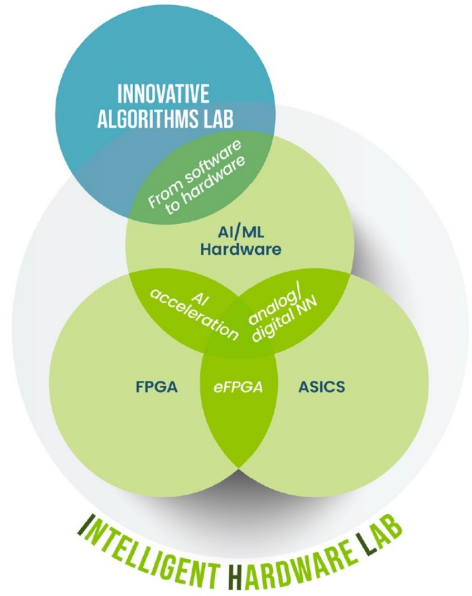
color meets flavor

TA1 – Intelligent Hardware Lab: Status and Outlook

uni-siegen.de

Qader Dorosti · Cluster Assembly

+ FPGA & electronics expertise at all CmF sites



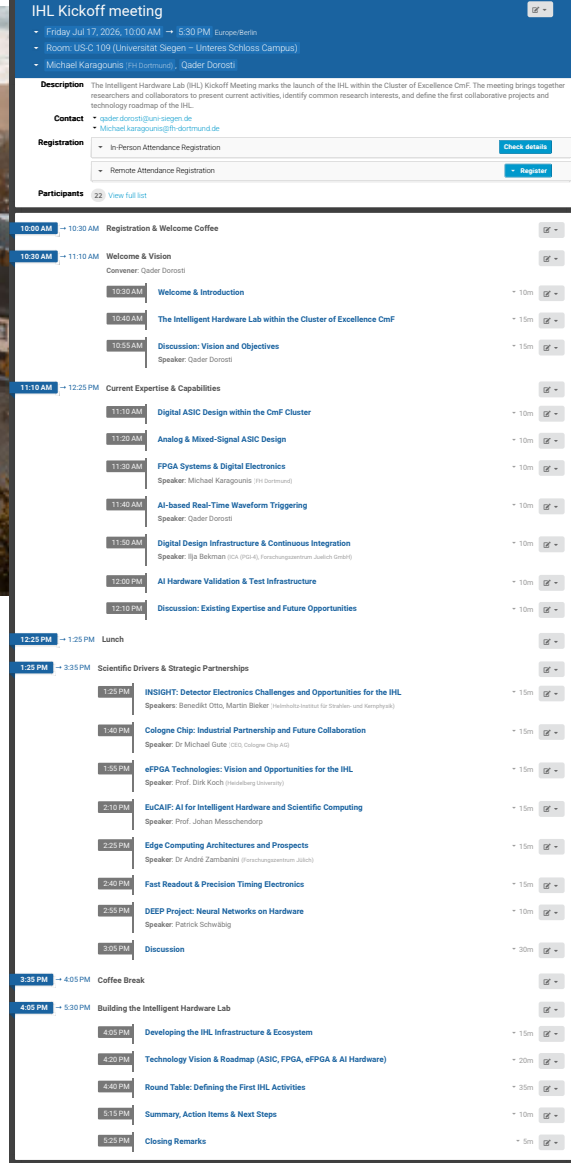
Personnel and Recruitment

- Research Fellows:
  - Tetsuichi Kishishita (Analog ASIC Design), University of Bonn (SiLAB)

- Recruitment in preparation (E-14)
  - AI on FPGA
  - ASIC Verification
  - Analog & Mixed-Signal ASIC Design

- Current status
  - Advertisements prepared
  - Requirement adapted to broaden the applicant pool
  - Administrative process ongoing

IHL Kickoff Meeting



IHL Kickoff meeting

Friday Jul 17, 2026, 10:00 AM → 5:30 PM Europe/Berlin

Room: US-C 109 (Universität Siegen – Unteres Schloss Campus)

Michael Karagounis (FH Dortmund), Qader Dorosti

Description The Intelligent Hardware Lab (IHL) Kickoff Meeting marks the launch of the IHL within the Cluster of Excellence CmF. The meeting brings together researchers and collaborators to present current activities, identify common research interests, and define the first collaborative projects and technology roadmap of the IHL.

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Registration In-Person Attendance Registration — Check details; Remote Attendance Registration — Register

Participants 22 View full list

10:00 AM → 10:30 AM **Registration & Welcome Coffee**

10:30 AM → 11:10 AM **Welcome & Vision**
Convener: Qader Dorosti
- 10:30 AM **Welcome & Introduction** · 10m
- 10:40 AM **The Intelligent Hardware Lab within the Cluster of Excellence CmF** · 15m
- 10:55 AM **Discussion: Vision and Objectives** · 15m
  Speaker: Qader Dorosti

11:10 AM → 12:25 PM **Current Expertise & Capabilities**
- 11:10 AM **Digital ASIC Design within the CmF Cluster** · 10m
- 11:20 AM **Analog & Mixed-Signal ASIC Design** · 10m
- 11:30 AM **FPGA Systems & Digital Electronics** · 10m
  Speaker: Michael Karagounis (FH Dortmund)
- 11:40 AM **AI-based Real-Time Waveform Triggering** · 10m
  Speaker: Qader Dorosti
- 11:50 AM **Digital Design Infrastructure & Continuous Integration** · 10m
  Speaker: Ilja Bekman (ICA (PGI-4), Forschungszentrum Jülich GmbH)
- 12:00 PM **AI Hardware Validation & Test Infrastructure** · 10m
- 12:10 PM **Discussion: Existing Expertise and Future Opportunities** · 10m

12:25 PM → 1:25 PM **Lunch**

1:25 PM → 3:35 PM **Scientific Drivers & Strategic Partnerships**
- 1:25 PM **INSIGHT: Detector Electronics Challenges and Opportunities for the IHL** · 15m
  Speakers: Benedikt Otto, Martin Bieker (Helmholtz-Institut für Strahlen- und Kernphysik)
- 1:40 PM **Cologne Chip: Industrial Partnership and Future Collaboration** · 15m
  Speaker: Dr Michael Gute (CEO, Cologne Chip AG)
- 1:55 PM **eFPGA Technologies: Vision and Opportunities for the IHL** · 15m
  Speaker: Prof. Dirk Koch (Heidelberg University)
- 2:10 PM **EuCAIF: AI for Intelligent Hardware and Scientific Computing** · 15m
  Speaker: Prof. Johan Messchendorp
- 2:25 PM **Edge Computing Architectures and Prospects** · 15m
  Speaker: Dr André Zambanini (Forschungszentrum Jülich)
- 2:40 PM **Fast Readout & Precision Timing Electronics** · 15m
- 2:55 PM **DEEP Project: Neural Networks on Hardware** · 10m
  Speaker: Patrick Schwäbig
- 3:05 PM **Discussion** · 30m

3:35 PM → 4:05 PM **Coffee Break**

4:05 PM → 5:30 PM **Building the Intelligent Hardware Lab**
- 4:05 PM **Developing the IHL Infrastructure & Ecosystem** · 15m
- 4:20 PM **Technology Vision & Roadmap (ASIC, FPGA, eFPGA & AI Hardware)** · 20m
- 4:40 PM **Round Table: Defining the First IHL Activities** · 35m
- 5:15 PM **Summary, Action Items & Next Steps** · 10m
- 5:25 PM **Closing Remarks** · 5m

- Current status
  - 21 registered participants
  - Mostly in-person attendance
- External Speakers
  - Michael Gude (Cologne Chip)
  - Dirk Koch (eFPGA / FABulous)
  - Johan Messchendorp (EuCAIF)
- Objectives
  - Build the IHL community
  - Identify first collaborative activities
  - Define the next steps

Registration still open

https://indico.hiskp.uni-bonn.de/event/1681

Stay connected

Community and Visibility

IHL website

color-meets-flavor.de/research/intelligent-hardware-lab-ihl

- IHL overview
- Partners and structure
- Visible entry point

IHL mailing list

listen.uni-bonn.de/wws/info/cmf-ihl

- Announcements
- Training dates
- Project coordination

Next step: make IHL more visible, reachable, and useful for the first CmF hardware projects.