UNIVERSITÄT BONN

SI LAB
Silizium Labor Bonn

RDL development in FTD Cleanroom

Elektronik Seminar – 19.01.2026

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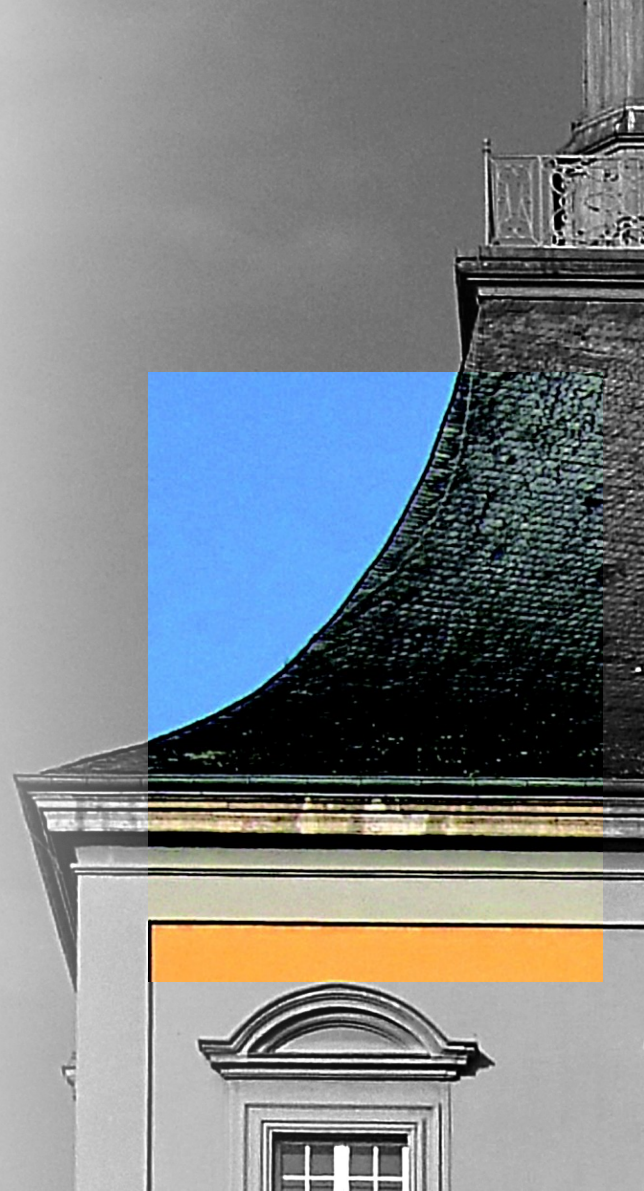
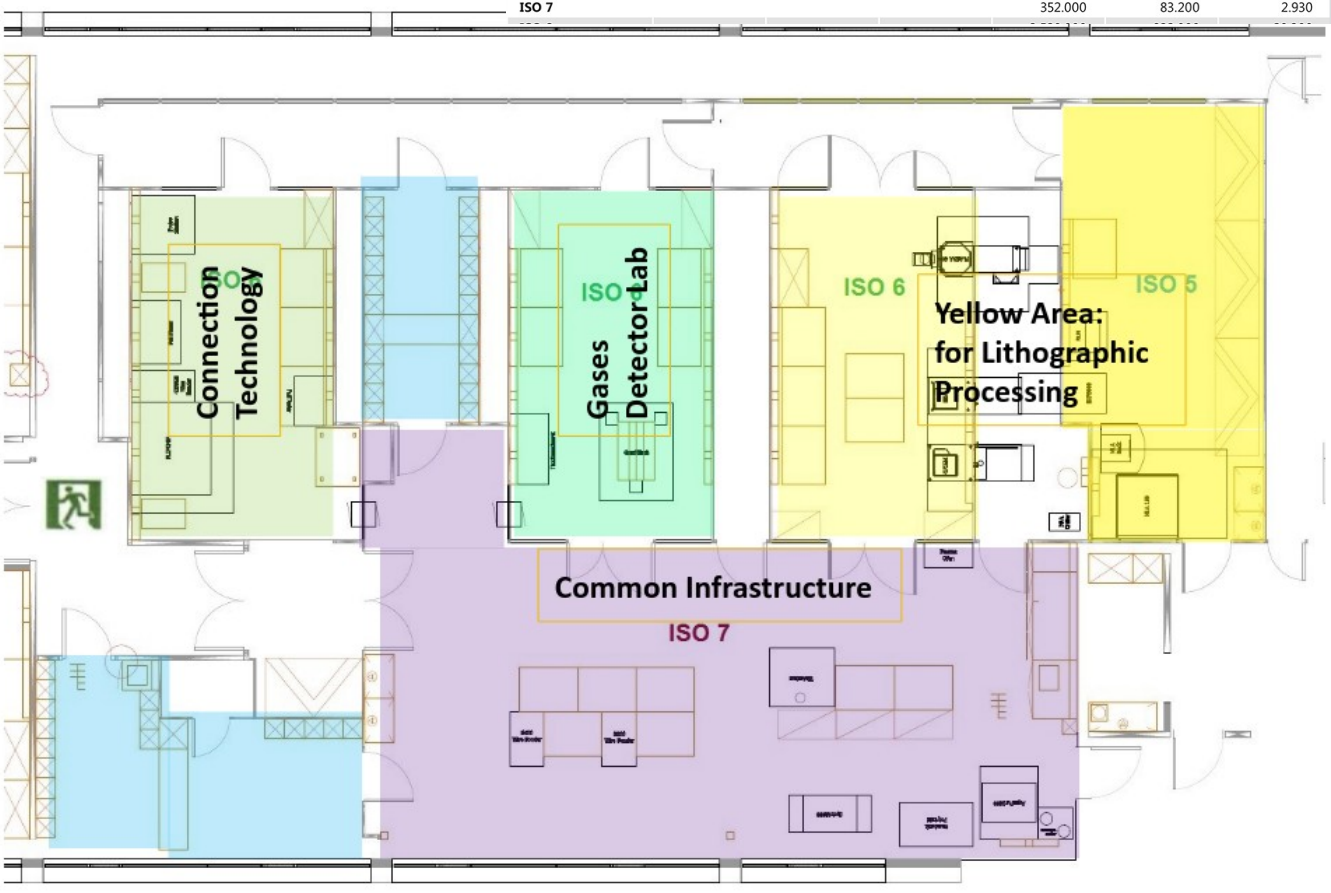


FTD Cleanroom

DIN EN ISO 14644-1	Höchstwert der zulässigen Konzentration (Partikel je m³)					
Klasse	≥ 0,1 µm	≥ 0,2 µm	≥ 0,3 µm	≥ 0,5 µm	≥ 1,0 µm	≥ 5,0 µm
ISO 1	10					
ISO 2	100	24	10			
ISO 3	1.000	237	102	35		
ISO 4	10.000	2.370	1.020	352	83	
ISO 5	100.000	23.700	10.200	3.520	832	
ISO 6	1.000.000	237.000	102.000	35.200	8.320	293
ISO 7				352.000	83.200	2.930

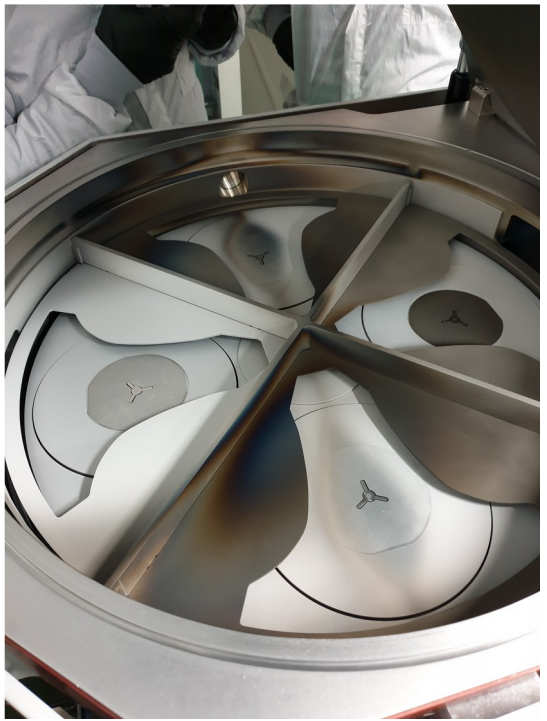
- ca. 350m² Cleanroom area
- Classes ISO 7 to ISO 5
- ISO 7 currently mostly occupied by ATLAS production
- ISO 6 area assigned to Interconnection Technologies and Wafer probing as well as Gaseous Detectors
- Yellow light area (ISO 6 and 5) used for photolithography processing



FTD Cleanroom - Machines

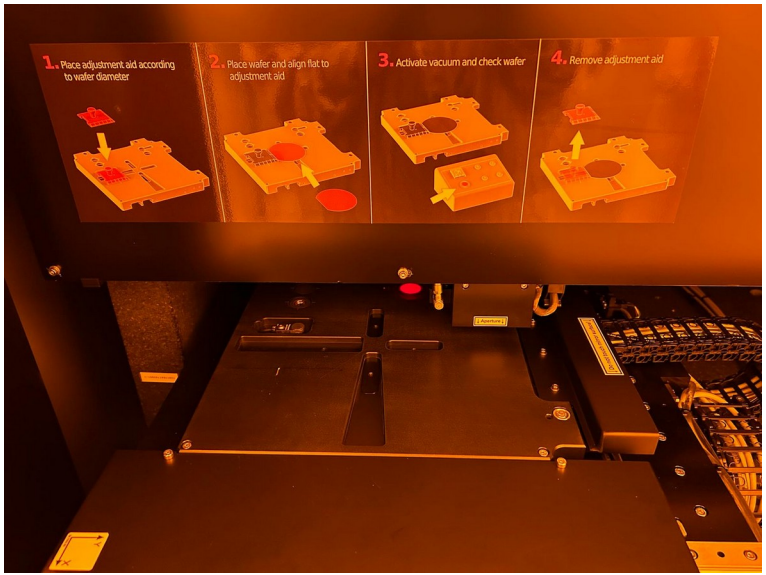
Relevant for today:

- MLA 150 – exposure
- PL 400 – sputtering
- RIE Machine – etching
- 3x Wet benches
  - Lithographic
  - Organic
  - Anorganic
- Microscopes and other measuring equipment.
- (Dicer/Wafer saw)



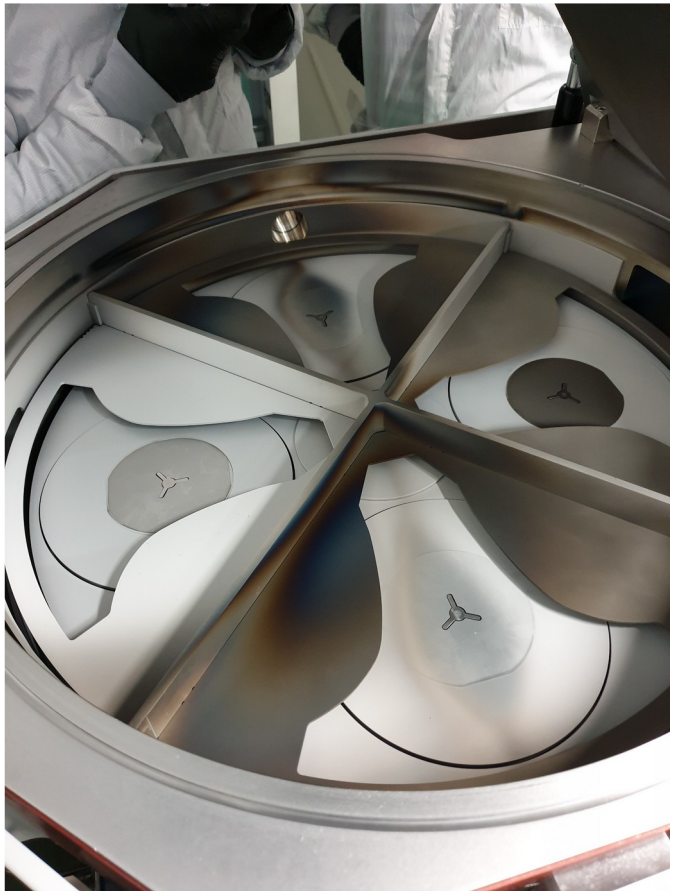
Machines: Heidelberg Instuments MLA 150

- Maskless Aligner Exposure Machine
- 375nm and 405nm laser for exposure
- Minimum feature size of 800nm
- Wafer size up to 150mm (200mm)
- Front- and backside aligment cameras
- Quick design changes possible due to maskless exposure
- Possibility to create masks



Machines: Oxford Instruments PL 400

- Sputtering machine (metalization)
- 4 different materials possibel (only Al installed)
- Up to 4 wafers at once
- Up to 200mm wafers
- Sputtering power between 500W and 5kW
- Process gas Ar (option to include N_2)

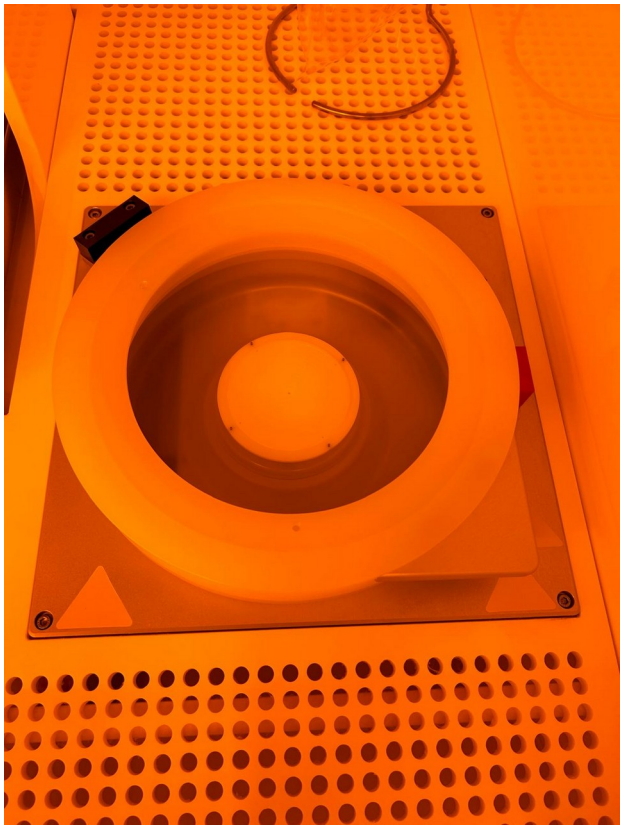


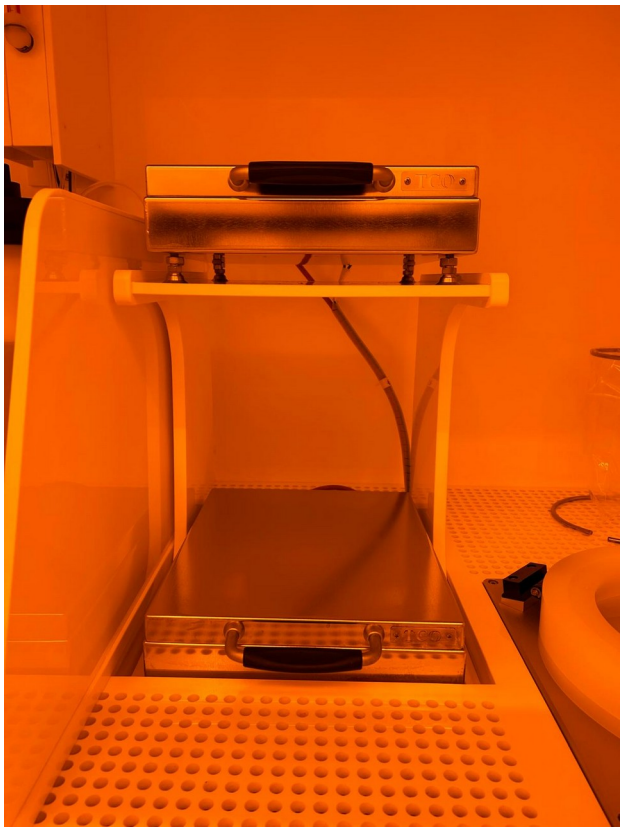
Machines: Wet benches

- 3 wet benches for processing of wafers up to 200mm
- Used for:
  - Application of photoresists
  - Development of photoresists
  - Baking
  - Wet chemical etching
  - Lift off
  - Etc.

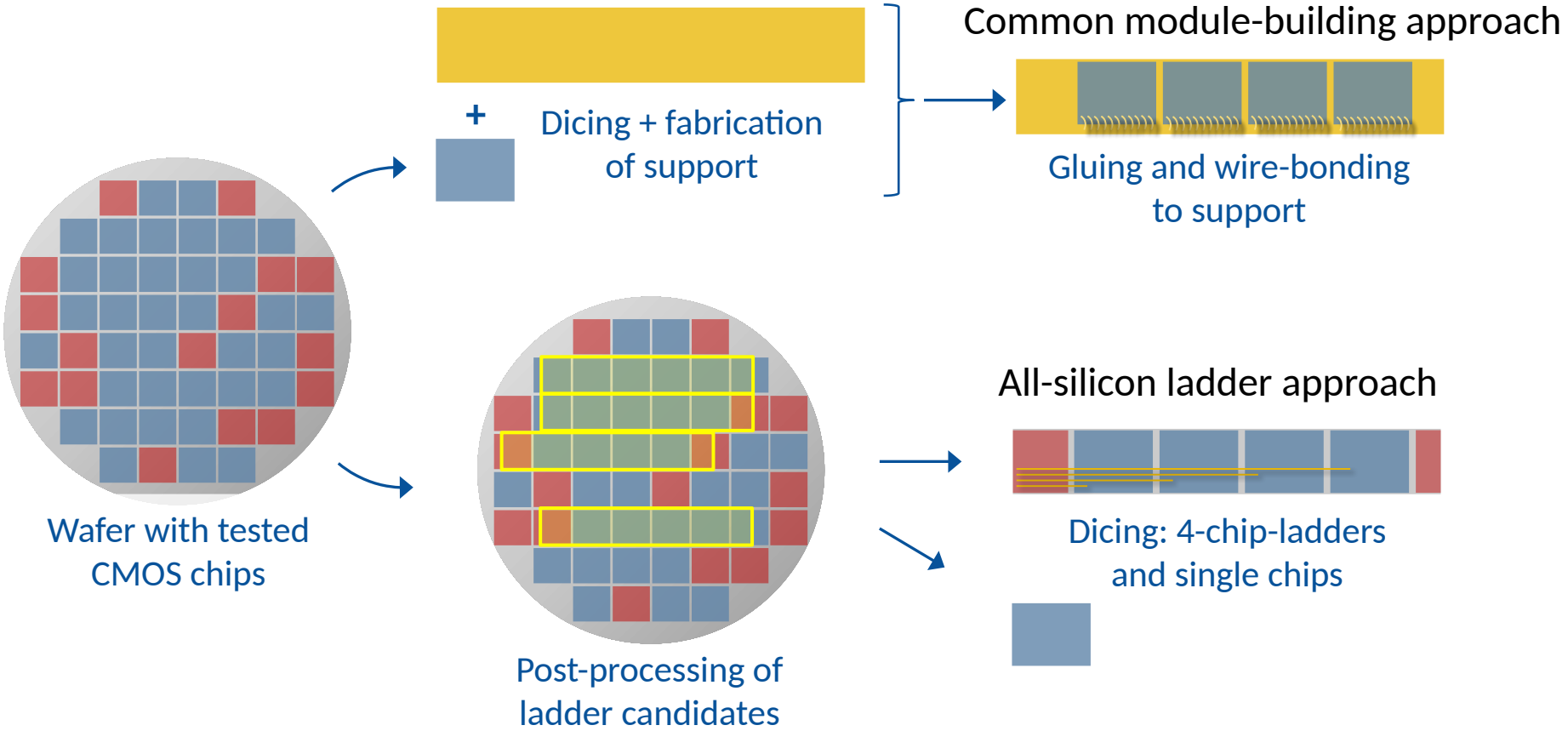
Machines: Wet bench equipment

- Wet benches include
  - Spinners
    - For drying
    - For chemical use
  - Hot plates
    - Automatic ~20°C to 200°C
    - Manuel ~20°C to 550°C (with N_2 oven)
  - DI water
  - (Destilled water)



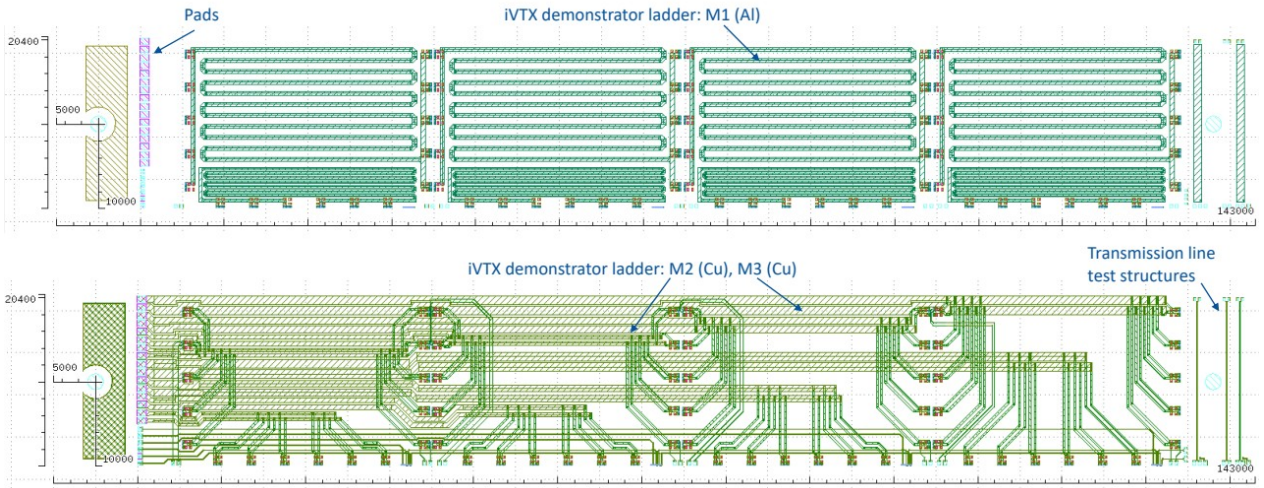


Concept


Common module-building approach
+
Dicing + fabrication of support
Gluing and wire-bonding to support
Wafer with tested CMOS chips
Post-processing of ladder candidates
All-silicon ladder approach
Dicing: 4-chip-ladders and single chips

RDL - Demonstrator

RDL demonstrator with resistive heater to developt working RDL



Metal system:

- Resistive heaters: 1.5 µm Al
- 2 RDL metal layers: 4 µm Cu
- Top metal finish: NiAu for wire-bonding, SMD soldering

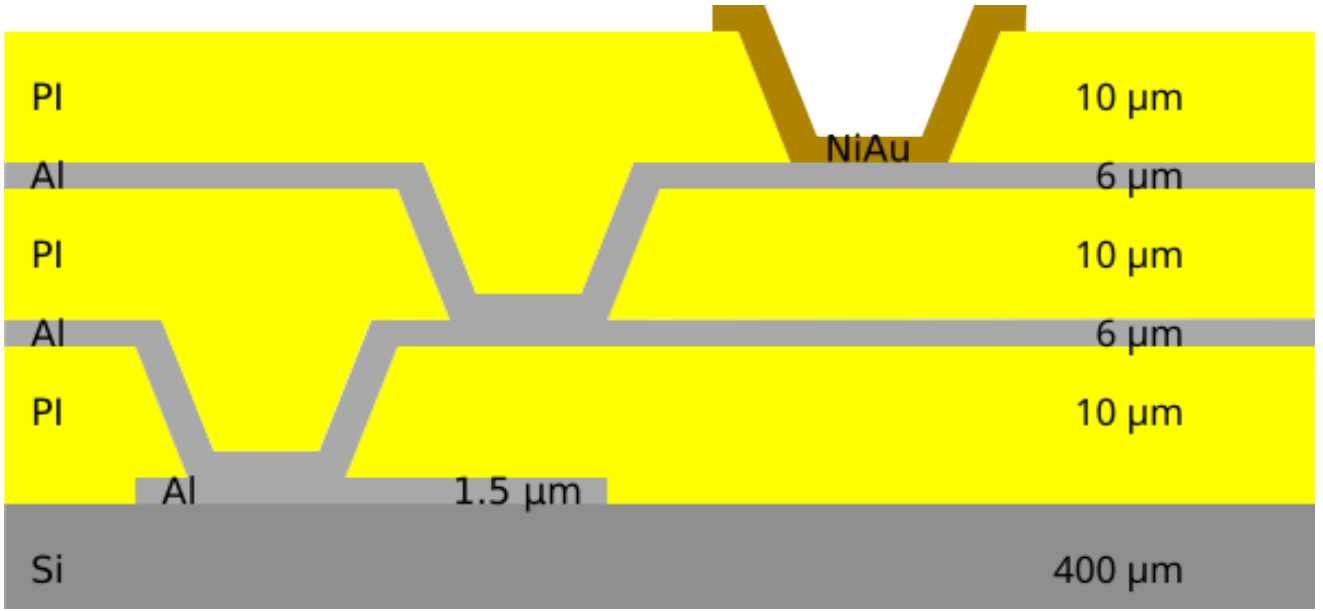
Ladder dimension: 143 x 20.4 mm^2
Dummy heaters (~10 Ω): 30 x 20 mm^2

First prototypes from IZM seem to be working fine but with copper

Currently developing clean room process in FTD cleanroom

Layer Stack-up

- First polymer layer “VIA1”
  - Openings above sensor bond pads
- First RDL metal “M1”
  - Contacts to sensor bond pads
- Second polymer layer “VIA2”
  - Openings to M1
- Second RDL metal “M2”
  - Contacts to M1
- Passivation layer “VIA3”
  - Openings to M2
- (NiAu bond pads “M3”)
  - Contacts to M2



Al Layer process:

	Pure process time
• Clean with Acetone/Isopropanol	~3min
• Bake for min. 10min @ min. 130°C	~15min
• Al sputter	~45min/um
• (Bake for min. 10min @ min. 130°C	~15min)
• Application Photoresist OiR 907-17 @ 1500rpm	~3min
• Softbake 60s @ 100°C	~2min
• Exposure in MLA @ 400-500mJ/cm²	~45min (4”)
• Develop in OPD 4262 for 60s	~1min
• Water rinse for 2min	~5min
• Wet Etch in Al 80	~20min/um
• Water rinse for 2min	~5min
• Acetone clean (remove PR)	~3min
• (Clean spinner and wet bench)	~15min

Polyimide Layer process:

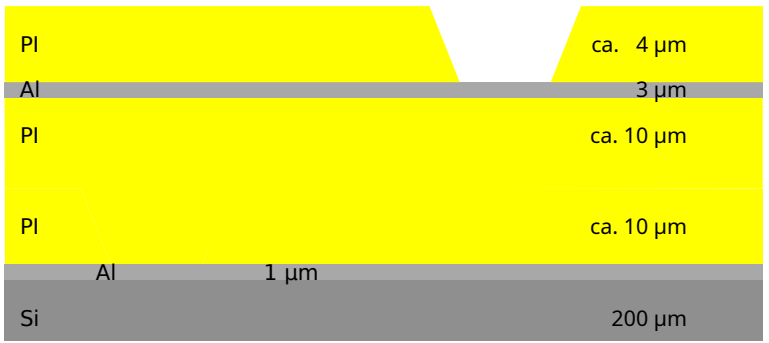
• Clean with Acetone/Isopropanol	~3min
• Bake for min. 10min @ min. 130°C	~15min
• HD 4100 @ 1500rpm (10um)	~3min
• Soft bake 1-4min @ 100°C	~5min
• Exposure @ 450-550mJ/cm^2	~45min (4”)
• Post exposure bake 60s @ 80°C	~2min
• Develop 2x 15s each Cyclopentanone/PGMEA @ 300rpm (dry spin @ min.1500rpm)	~3min
• (Post develop bake 2min @ 150°C then 2min @ 200°C)	~5min
• Hard bake in N_2 30min @ 200°C (10°C/min ramp) then 60min @ 375°C (10°C/min ramp) then cool to room temp	~3h

Pure process time

Stackup for teststurctures

Simplified stackup:

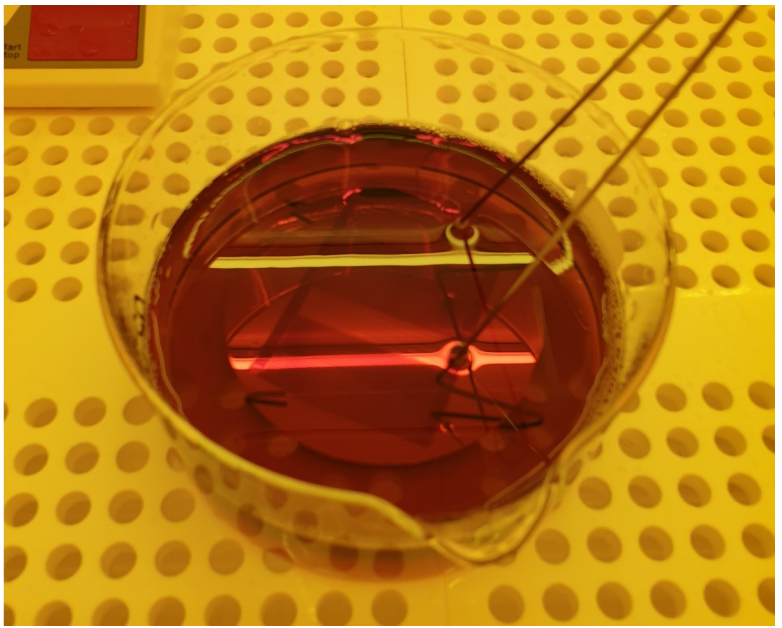
- trace width/seperation simpified for ease of production (40/40 and 30/30)
- 3 wafers working (one broke during production)
  5 structures wire bonded to PCB
- Structure length between 5 and ca. 20 cm
- Al layer thickness currently limited to 3um
- Signal layers only (first via test ongoing)



Production steps

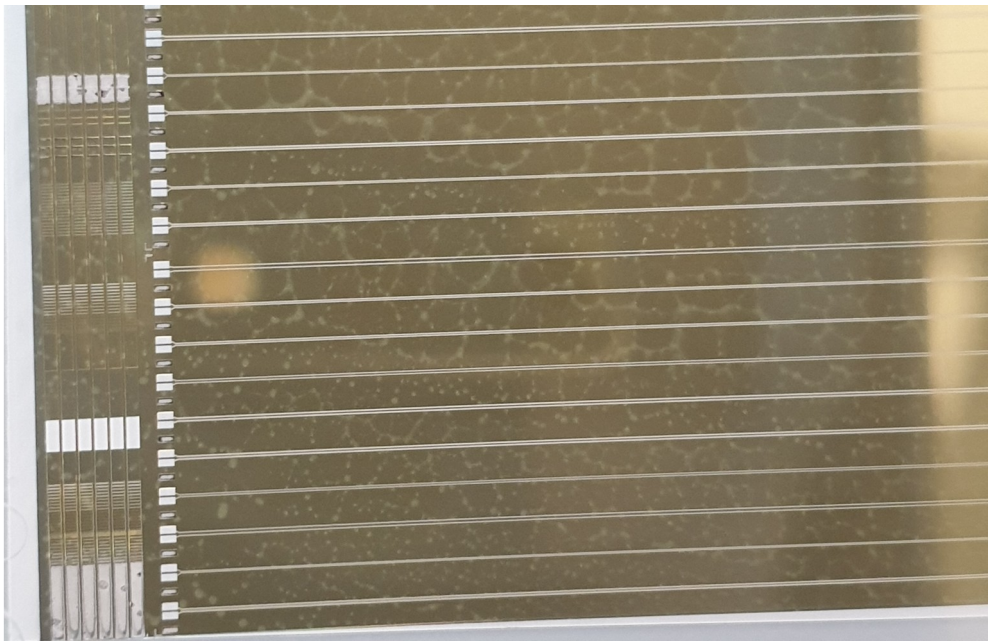
- Sputtering of 1um Al
- Photoresist + etch of Al
- HD 4100 processing (no hard bake)
- HD 4100 processing
- Hard bake
- Sputtering 3 um
- Photoresist + etch
- HD 4100 processing
- Hard bake

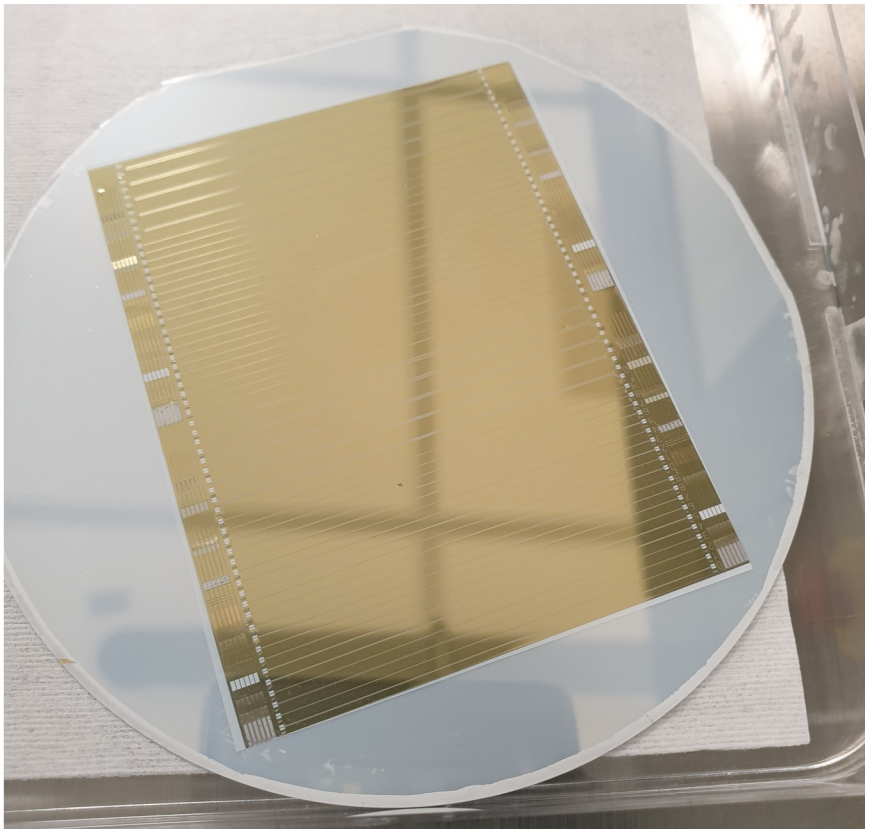
Four 200 um 10 cm wafers were processed of which one broke on the MLA (when removing tape to hold wafer down)



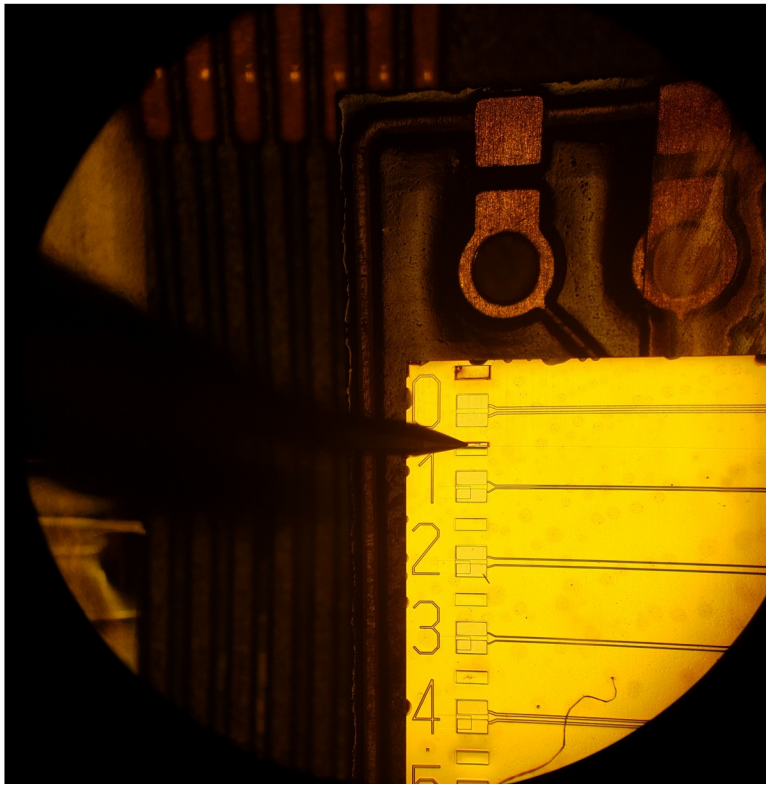
3 wafers produced

- Production finished smoothly
- Several of the structures seem to work!





Needle probing

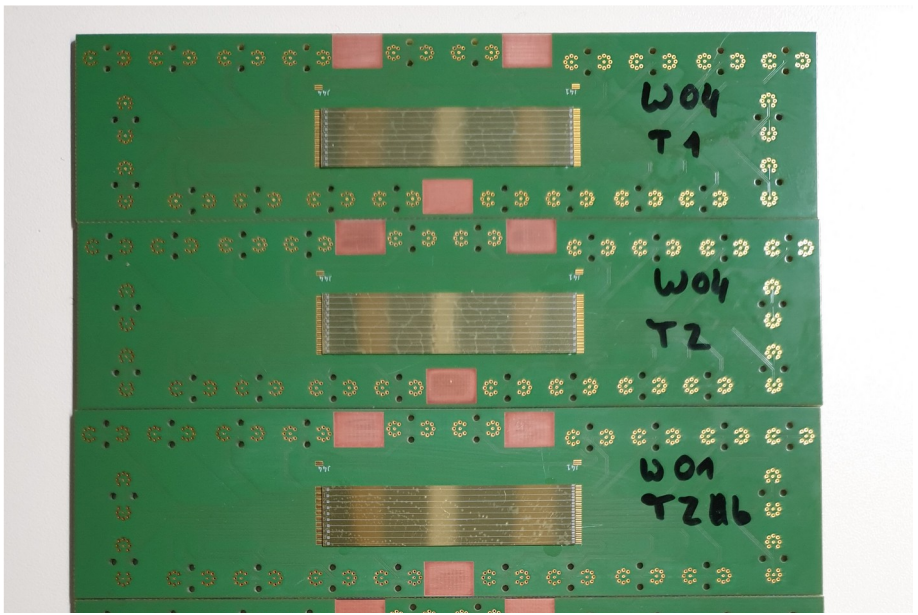


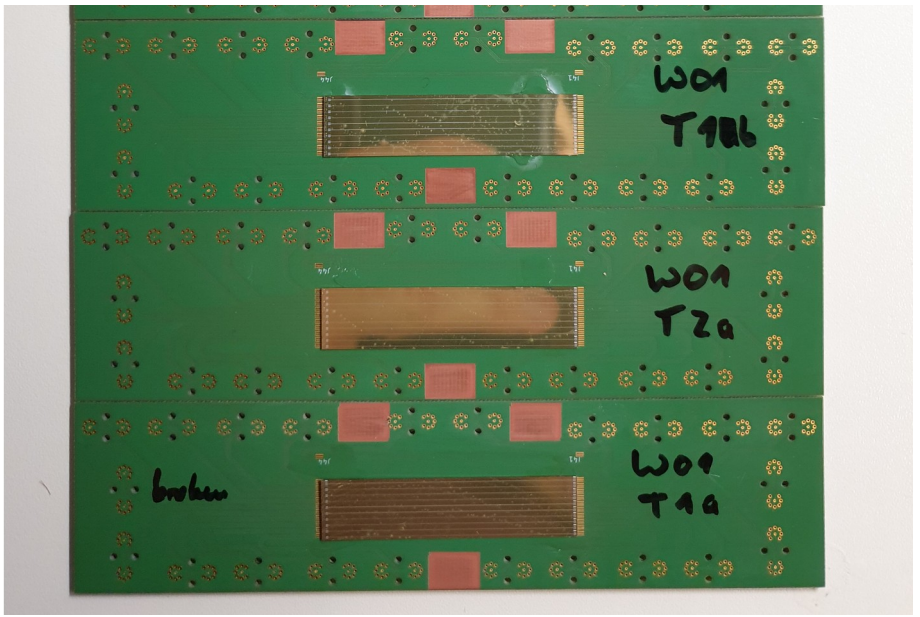
- Verified contact and continuety of traces with needle prober
- Found good contact to GND on most modules
- Found that not all GND pads are usable
  - On one wafer, left GND pads not open, right pads usable, so connection only from one side (misaligned exposure stopped early, aligned, restarted)
  - On one wafer we were able to scratch GND pads open on right side before wire bonding to achieve contact to GND pads (one layer misaligned)
  - On one wafer pads were etched away, no solution yet but not important for measurements shown today

Test structures glued to PCBs

Structures were glued to PCB

- Problematic: bending of modules due to poyimide shrinking during hard bake

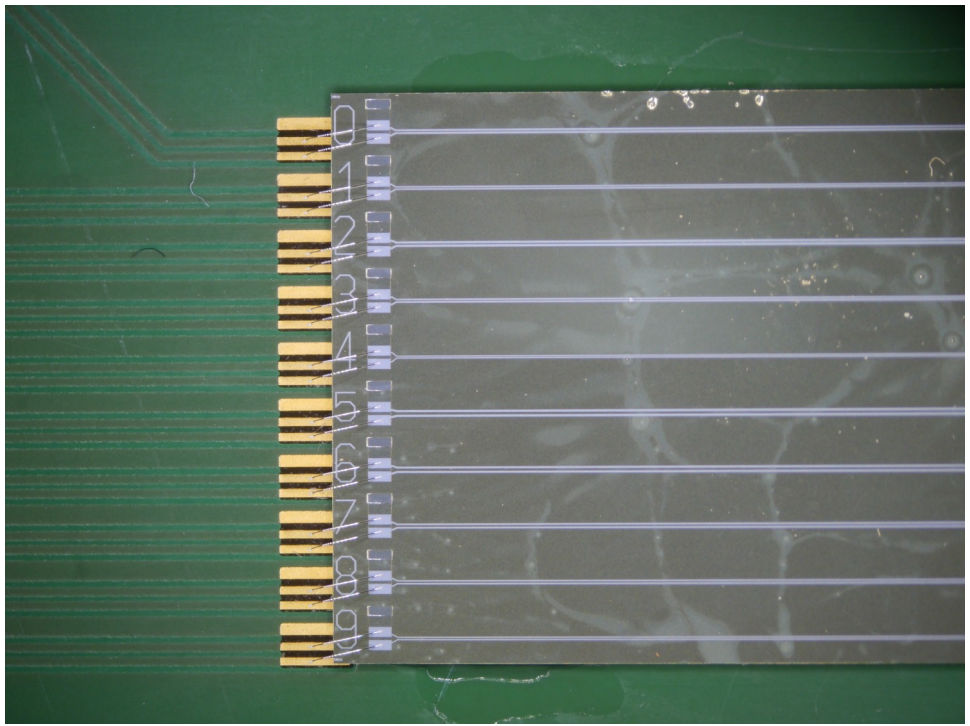


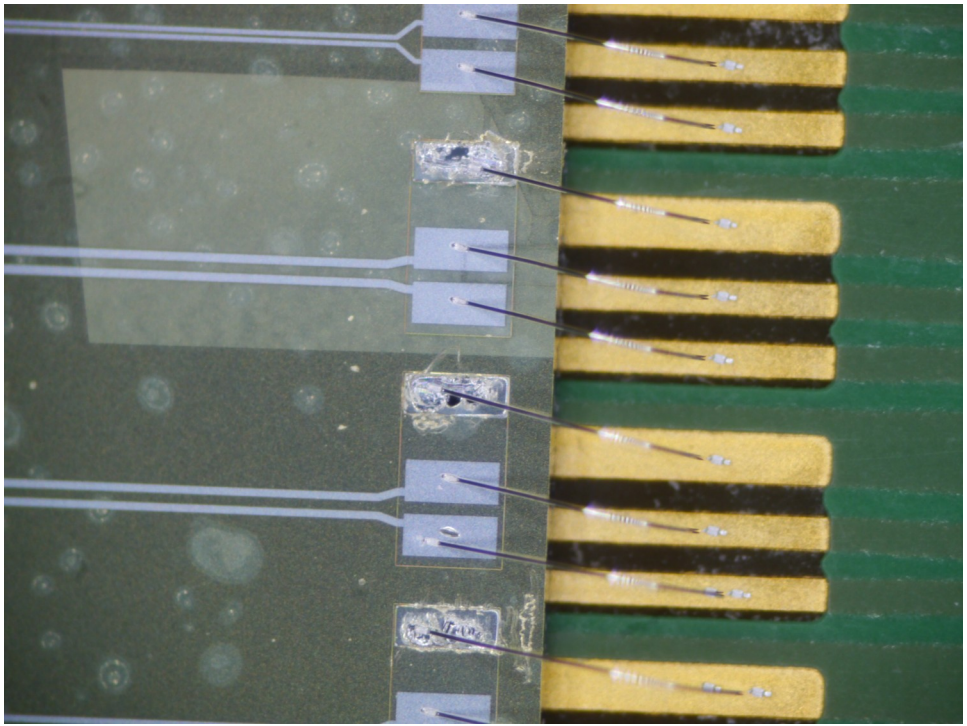


One module broke during gluing

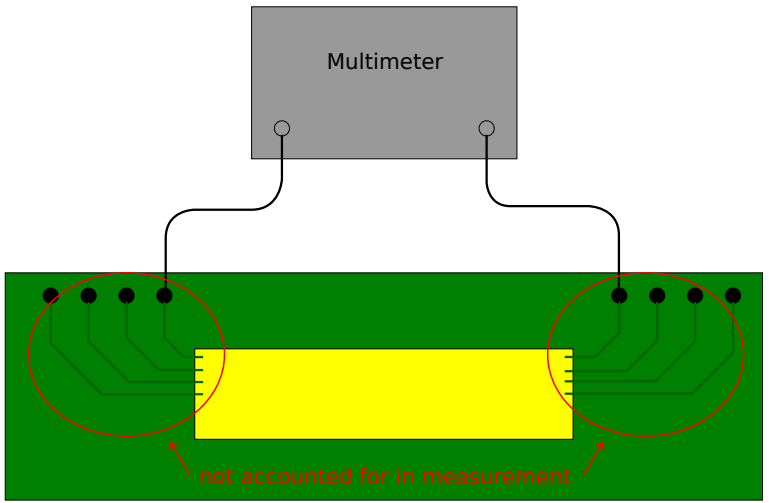
Test structures bonded to PCB

After needle measurements test structures were bonded to PCBs





Preliminary resistance measurements



- Measured resitances with Multimeter
- Not for all corrected for resistances of PCB or wirebonds but corrected for resistance of cables
- Expected values calculated from trace dimensions

W01b T1 TS1

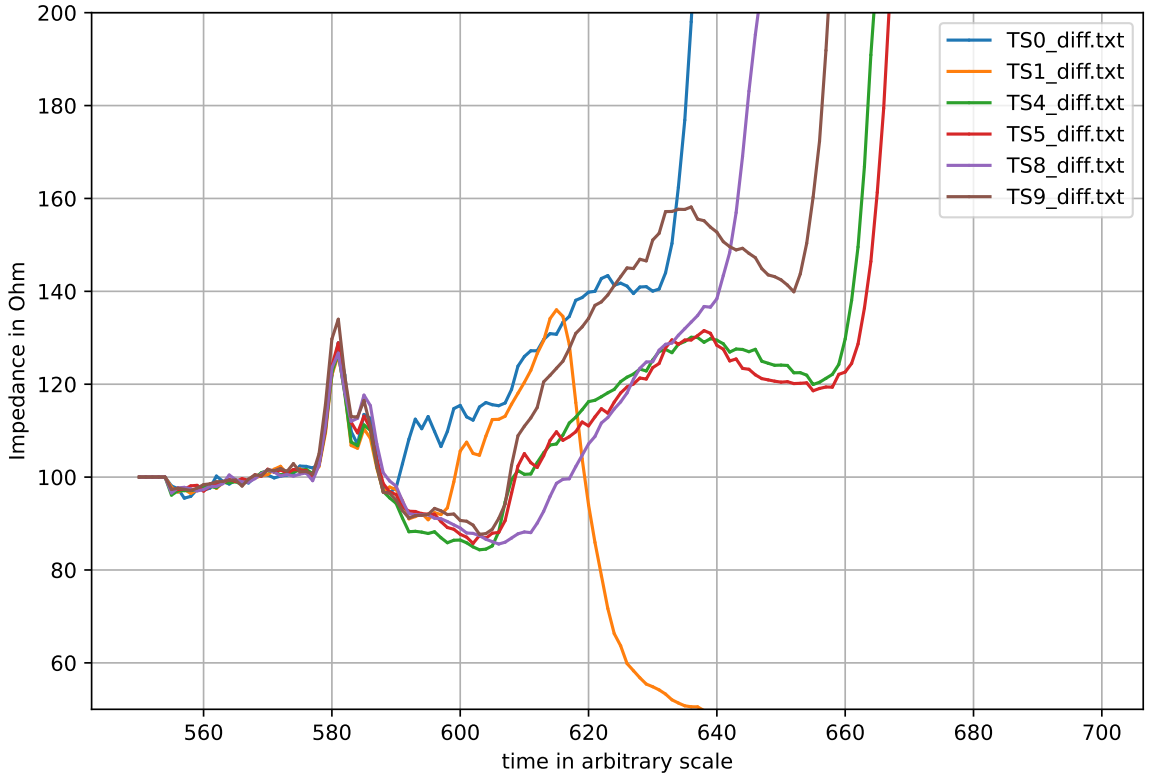
TS0 - 45um			
a)	15.7* Ohm	|	expect:
b)	15.7* Ohm	|	10.5
a-b)	open		
TS1 - 30um			
a)	30.98 Ohm	|	
b)	31.32 Ohm	|	16.4
b-a)	20.21 Ohm	|	
a-b)	40.81 Ohm	|	
TS4 - 50um			
a)	14.00 Ohm	|	9.4
b)	14.22 Ohm	|	
a-b)	open		

TS5 -50um			
a)	13.5* Ohm	|	expect:
b)	13.6* Ohm	|	9.4
a-b)	open		
TS8 - 40um			
a)	20.45 Ohm	|	11.9
b)	-- Ohm	|	
a-b)	open		
TS9 - 40um			
a)	21.30 Ohm	|	11.9
b)	22.18 Ohm	|	
a-b)	open		

*4 point

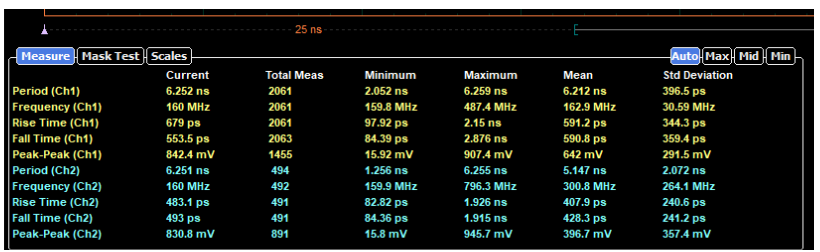
Preliminary impedance measurements

- TDR shows differnetial trace impedance between 100 and 140 Ohms
- 5cm structure is resolvable and impedance is in expected (and acceptable) range
- Strong resistive component visible
- One differential pair shows short (TS1, yellow plot)

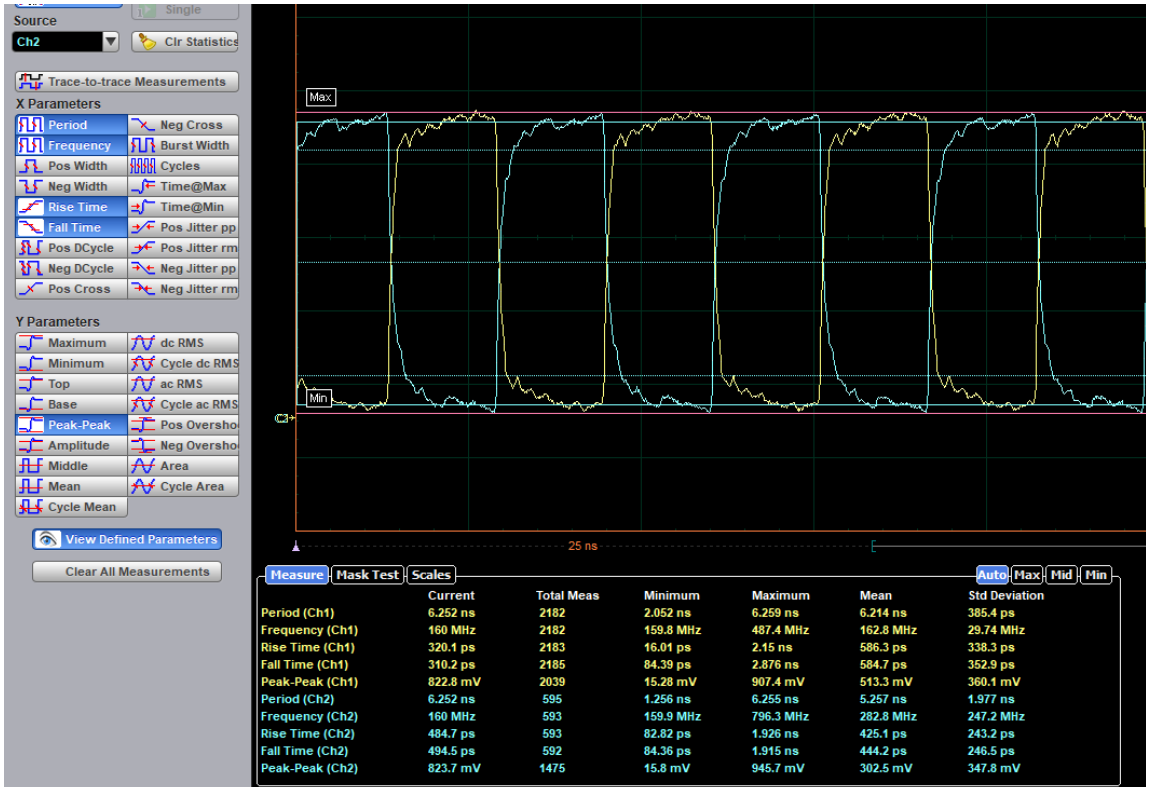


Preliminary measurements

- Rise and fall times were measured with signal generator and square signal
- Rise/Fall time in range of 300 ps to 600 ps



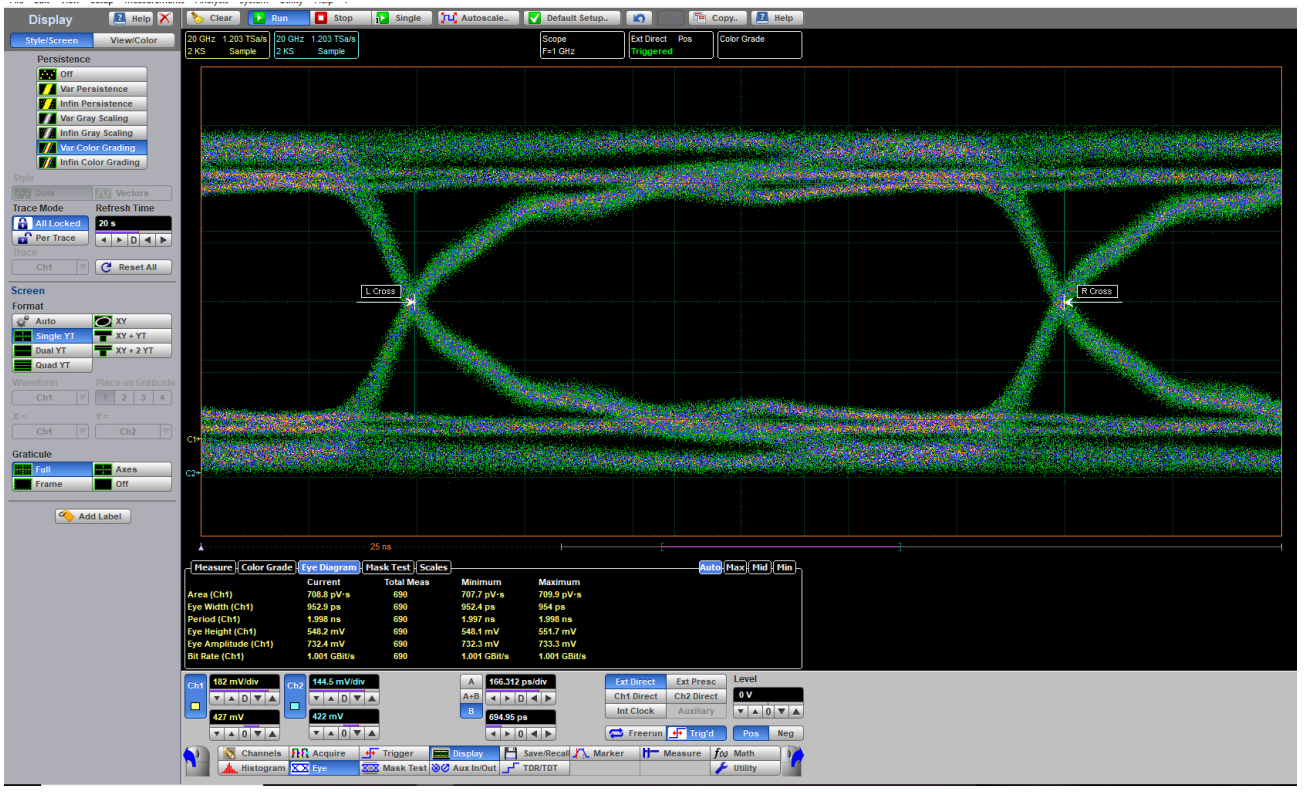
	Current	Total Meas	Minimum	Maximum	Mean	Std Deviation
Period (Ch1)	6.252 ns	2061	2.052 ns	6.259 ns	6.212 ns	396.5 ps
Frequency (Ch1)	160 MHz	2061	159.8 MHz	487.4 MHz	162.9 MHz	30.59 MHz
Rise Time (Ch1)	679 ps	2061	97.92 ps	2.15 ns	591.2 ps	344.3 ps
Fall Time (Ch1)	553.5 ps	2063	84.39 ps	2.876 ns	590.8 ps	359.4 ps
Peak-Peak (Ch1)	842.4 mV	1455	15.92 mV	907.4 mV	642 mV	291.5 mV
Period (Ch2)	6.251 ns	494	1.256 ns	6.255 ns	5.147 ns	2.072 ns
Frequency (Ch2)	160 MHz	492	159.9 MHz	796.3 MHz	300.8 MHz	264.1 MHz
Rise Time (Ch2)	483.1 ps	491	82.82 ps	1.926 ns	407.9 ps	240.6 ps
Fall Time (Ch2)	493 ps	491	84.36 ps	1.915 ns	428.3 ps	241.2 ps
Peak-Peak (Ch2)	830.8 mV	891	15.8 mV	945.7 mV	396.7 mV	357.4 mV



	Current	Total Meas	Minimum	Maximum	Mean	Std Deviation
Period (Ch1)	6.252 ns	2182	2.052 ns	6.259 ns	6.214 ns	385.4 ps
Frequency (Ch1)	160 MHz	2182	159.8 MHz	487.4 MHz	162.8 MHz	29.74 MHz
Rise Time (Ch1)	320.1 ps	2183	16.01 ps	2.15 ns	586.3 ps	338.3 ps
Fall Time (Ch1)	310.2 ps	2185	84.39 ps	2.876 ns	584.7 ps	352.9 ps
Peak-Peak (Ch1)	822.8 mV	2039	15.28 mV	907.4 mV	513.3 mV	360.1 mV
Period (Ch2)	6.252 ns	595	1.256 ns	6.255 ns	5.257 ns	1.977 ns
Frequency (Ch2)	160 MHz	593	159.9 MHz	796.3 MHz	282.8 MHz	247.2 MHz
Rise Time (Ch2)	484.7 ps	593	82.82 ps	1.926 ns	425.1 ps	243.2 ps
Fall Time (Ch2)	494.5 ps	592	84.36 ps	1.915 ns	444.2 ps	246.5 ps
Peak-Peak (Ch2)	823.7 mV	1475	15.8 mV	945.7 mV	302.5 mV	347.8 mV

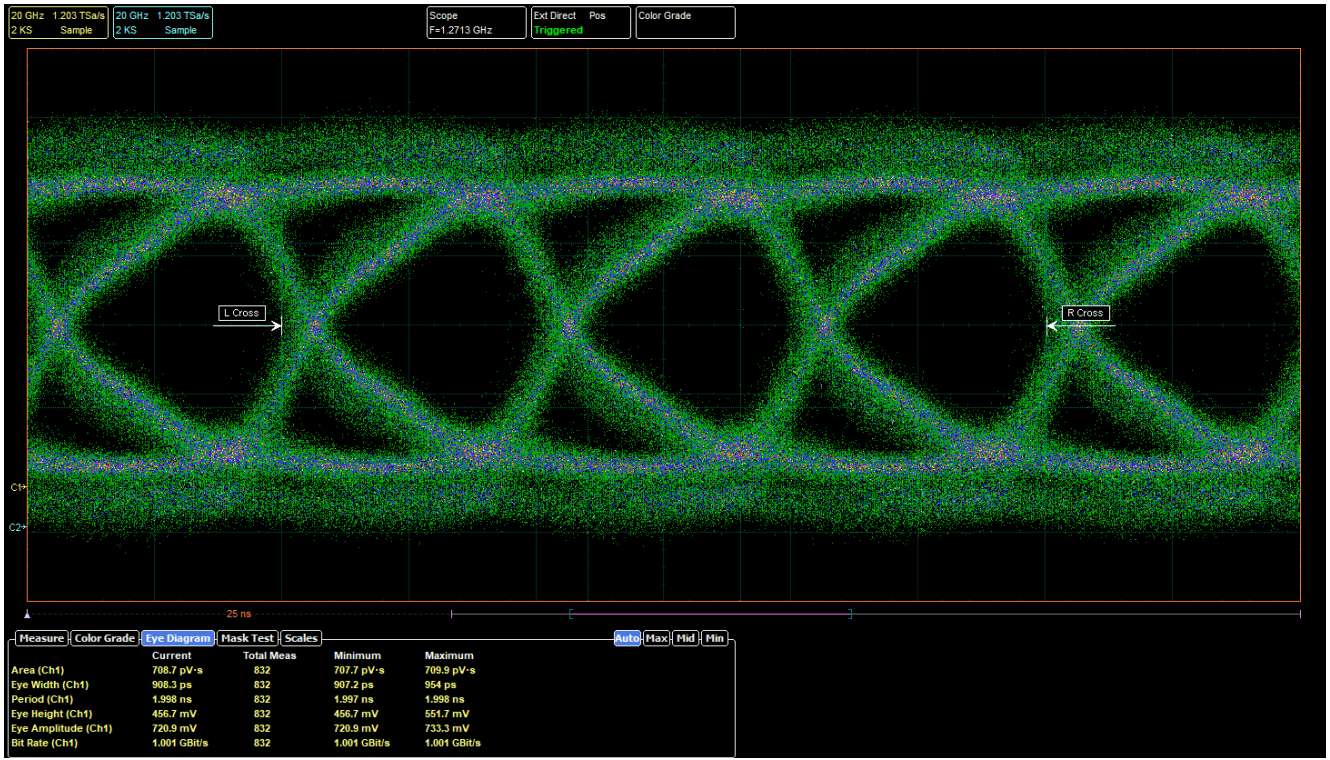
Preliminary eyediagrams

- On one test trace eye diagrams were recorded
  - With 1GHz
- Eye is wide open
  - But expected considering the trace length is only 5 cm



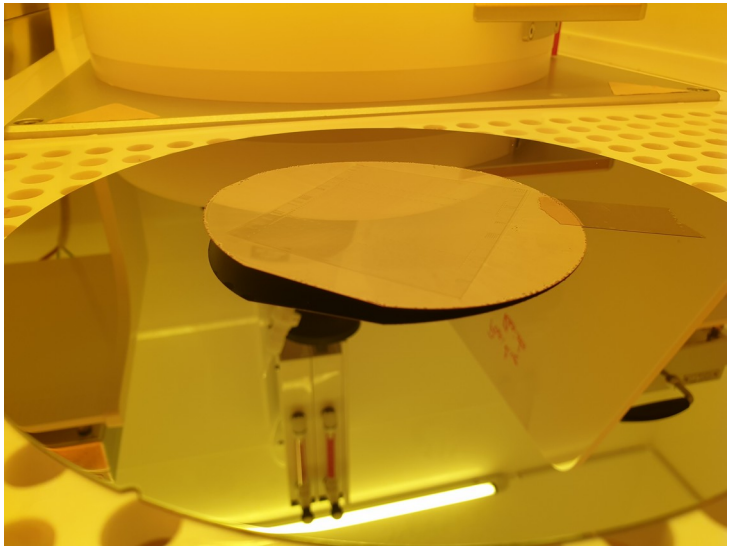
Preliminary eyediagrams

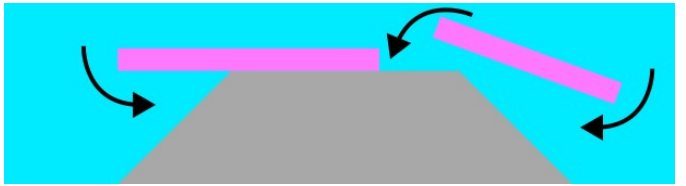
- On one test trace eye diagrams were recorded
  - With 3GHz
- Eye is still very much open.
- Need simulation to compare and need longer structure to verify results for full length RDL



Issues (some selected current and past)

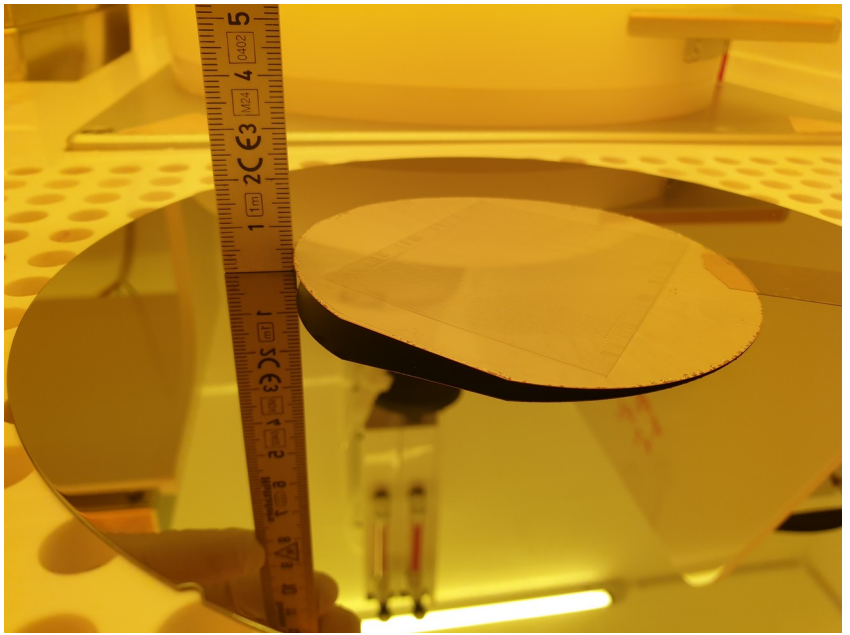
- Bending of wafer
  - Due to polyimide shrinking
- Wafersize of 200mm on MLA
- Vias (delamination)
  - Bad adhesion of HD4100 after hard bake
- Etching of thick AL layers
  - Thick Al layers etch very non uniformly and traces are often bad





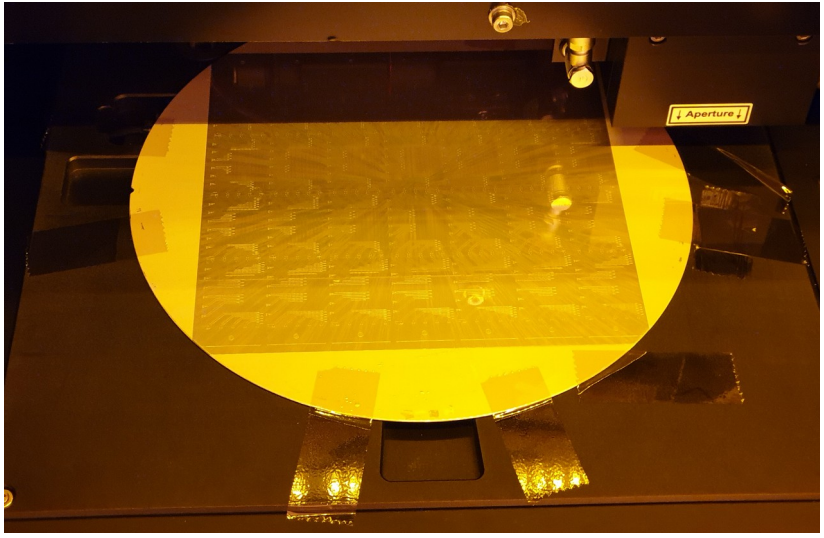
Bending issues

- Bending of modules has been observed on all structures so far
  - Thinner modules bend more due to polyimide tension after hard bake
- Leads to problems with exposure on MLA
- Ideas so far:
  - Use different photoresist (BCB)
  - Process wafer from backside first to introduce bending in opposite direction before processing, resulting in less tension after hard bake



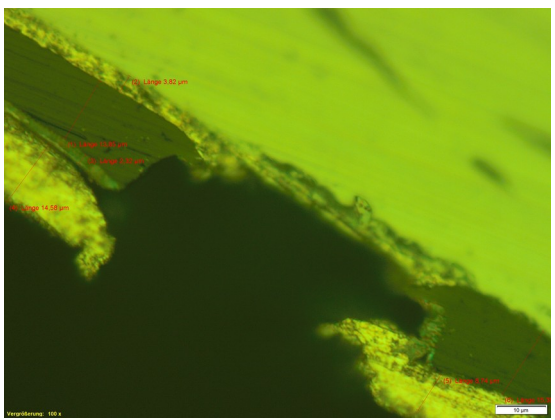
Wafer size on MLA issues

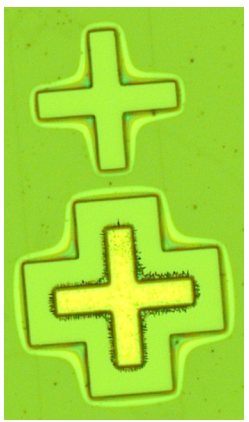
- It is currently (not) possible to process 200mm wafers on the MLA
- MLA is designed for max. 150mm wafers
  - Vacuum chuck (really poor design even for 100mm) incapable of holding 200mm wafers down
    - Workaround: Tape
  - Metal sensor for adjustment aid alarm placed under substrate of 200mm leading to warning and software to stop operation if wafer is metalized
    - Workaround: disable sensor (really risky!)
- Heidelberg is unable to fix the issues even though, they sell the machine officially to support 200mm

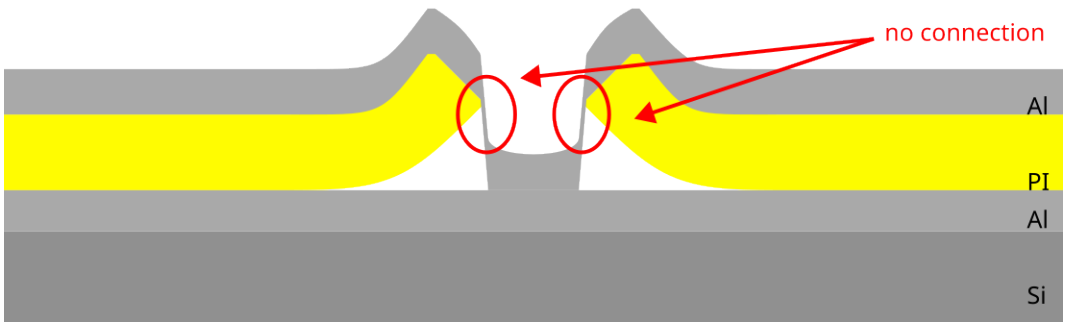


Delamination issues of HD 4100

- Cured HD 4100 lifts of at via openings
- Issue seems to be water residuals form rinsing/humidity
  - Humidity in cleanroom extremely unstable: between 30% rel. Hum. in winter and 55% rel. Hum. in summer
- Solution: baking the wafer before further processing at min. 130°C seems to work quite well

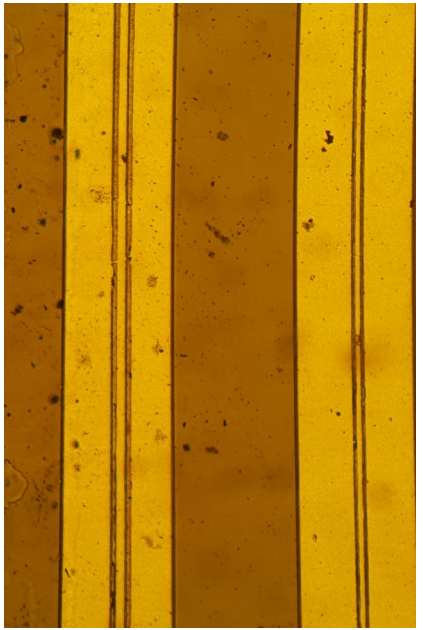


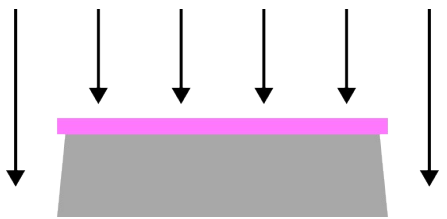


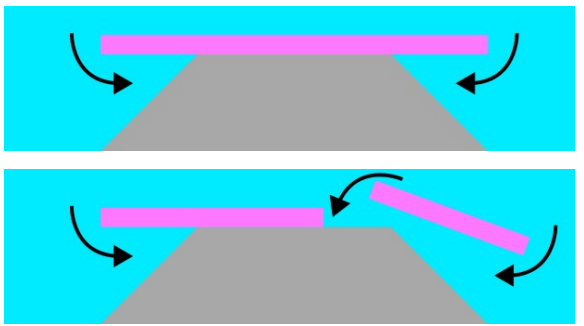


Issues with thick Al layers:

- Thick Al layers tend to etch very poorly
  - Most likely the photoresist breaks away leaving more metal exposed to etchant
  - Traces are broken and unusable
- No solution, yet, but ideas:
  - Etch in 2 or 3 steps (less overhang)
  - Liftoff with thick photoresist
  - Reactice ion etching
  - Embeddd trace in HD 4100







Conclusion

- RDL production in cleanroom is on a path to success
- Still a lot of experience needs to be gained for optimal results and less broken wafers
- Open issues need to be overcome
- All machines need to be installed (Oxford machines installation ongoing)
- Environmental control (humidity and temperature) need to be upgraded as soon as possible (Problem: ATLAS Production cannot be halted)

Backup – Disco DAD 3660

- Dicing saw in ISO 7 as final step of production
- Mechanical saw for silicon and glas
- Precise cutting with 200um thin blade
- Automatic cutting after training
- Clean cuts usable for crosssectioning

Backup – Oxford RIE PlasmaPro 80

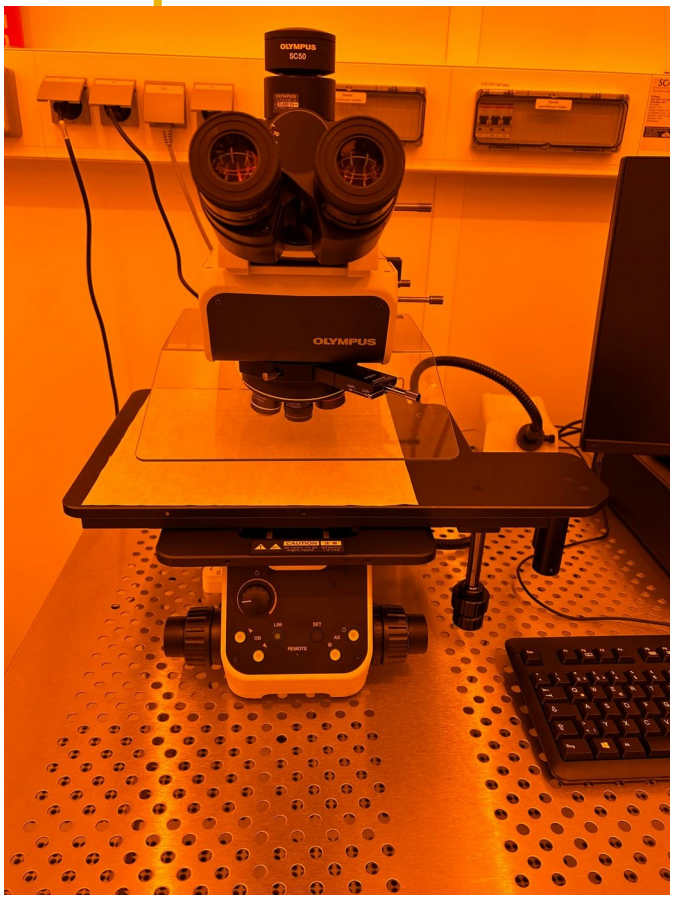
- Reachtive Ion Etching Machine
- Capable of up to 200mm
- Etching with different gas combinations
- Currently: service installation by Dräger
- Commissioning in the future

Backup – Oxford PECVD PlasmaPro 80

- Plasma enhanced chemical vapor deposition machine
- Capable of up to 200mm
- Currently: service installation by Dräger
- Commissioning in the future

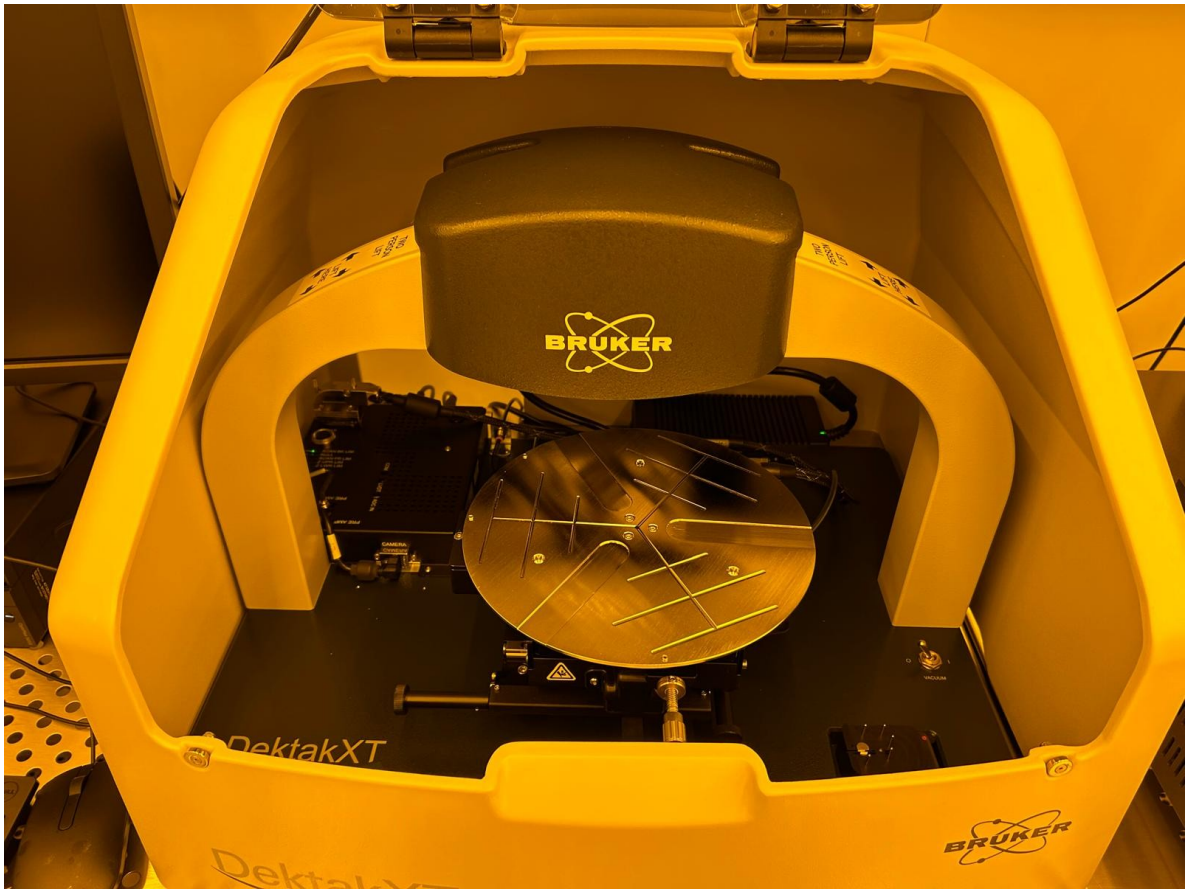
Backup – Olympus Microscope

- 5x up to 100x (2um structures nicely resolvable)
- Connection to PC with measurement software
- Photo capability



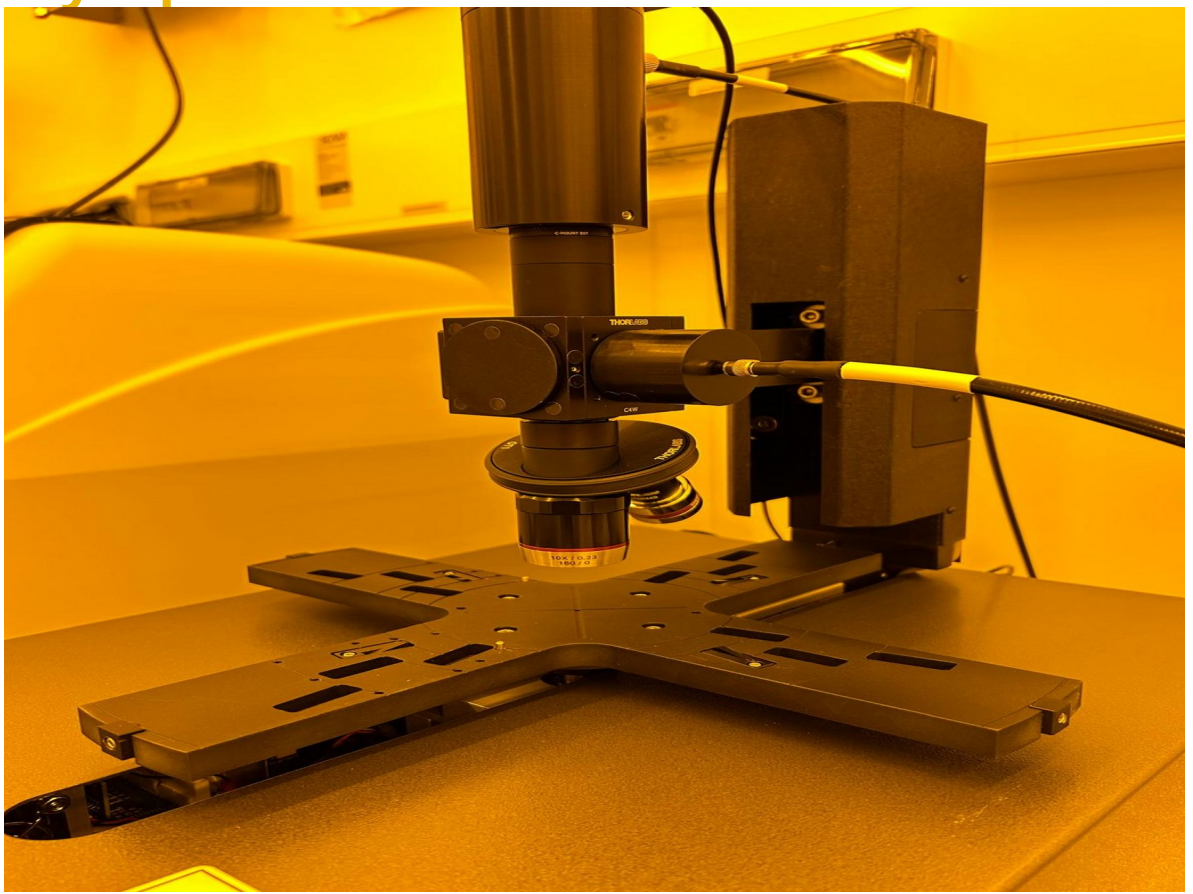
Backup – Bruker DektakXT

- Stylus profiler
- Surface inspection with nm precision
- Wafers up to (200mm)
  - Edges of wafers cannot be probed in any direction because table movement is restricted
  - Only 100mm wafers are fully probeable
  - Upgrade should be considered



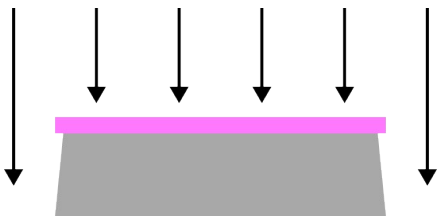
Backup – Olympus interferometer

- Laser interferometer for photoresist thickness measurements
- Automatic measrement procedures
- Need recipes for different resists



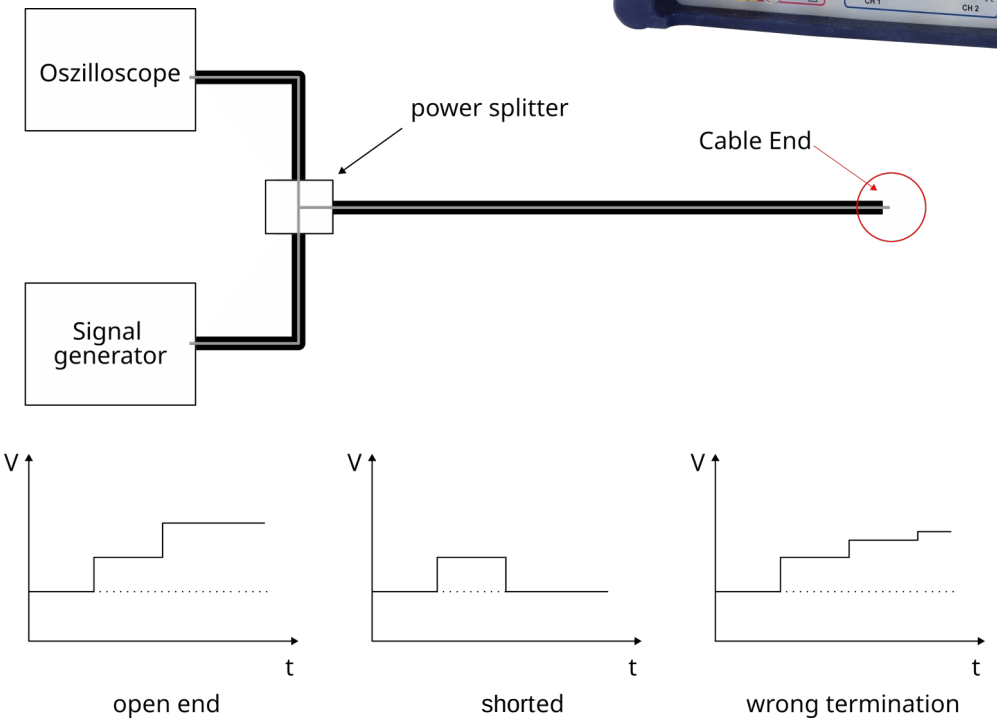
Backup – production of thick Al layers

- Several options to be tested:
  - Multi layer Al: make 2 x 3um Al layers on top of each other and etch separately
    - Possible issues with trace geometry, oxide layer
  - Lift off: structure very thick photoresist first, sputter on top, remove resist, take Al on top, leave trace
    - Possible issues with resist selection, exposure, solvent
  - Dry etching: use dry etching machine for etching
    - Possible issues with etch speed, Al thickness
- Need to try everything and evaluate best option



TDR - Time domain reflectometry

- Send electrical pulse and measure reflection
- Important is sharp edge at the beginning
- Method used to measure
  - Cable length
  - Defects
  - Shorts
  - Changes of impedance
  - Etc.



Backup – Layer thickness measurements