Fachhochschule Dortmund
University of Applied Sciences and Arts

FPGA & Electronics

Intelligent Reconfigurable Detector Electronics

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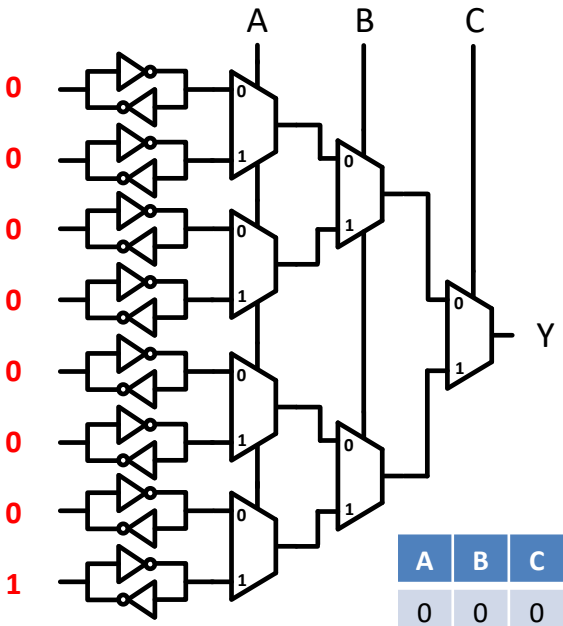
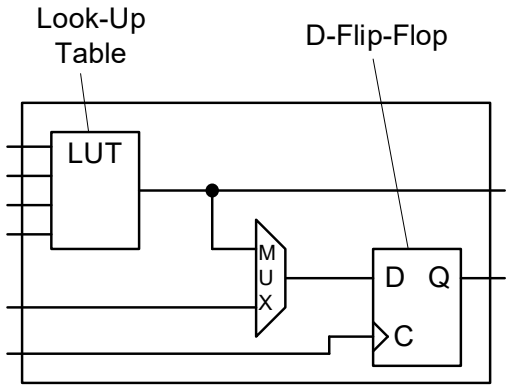
Qader Dorosti, Andre Zambanini, Michael Karagounis

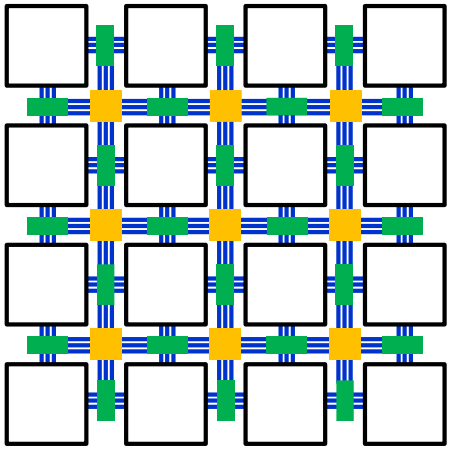
CmF TA1 Kickoff Meeting, Bonn

Field Programmable Gate Array (FPGA)

- An FPGA is a type of digital logic device that can be reconfigured after production







A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

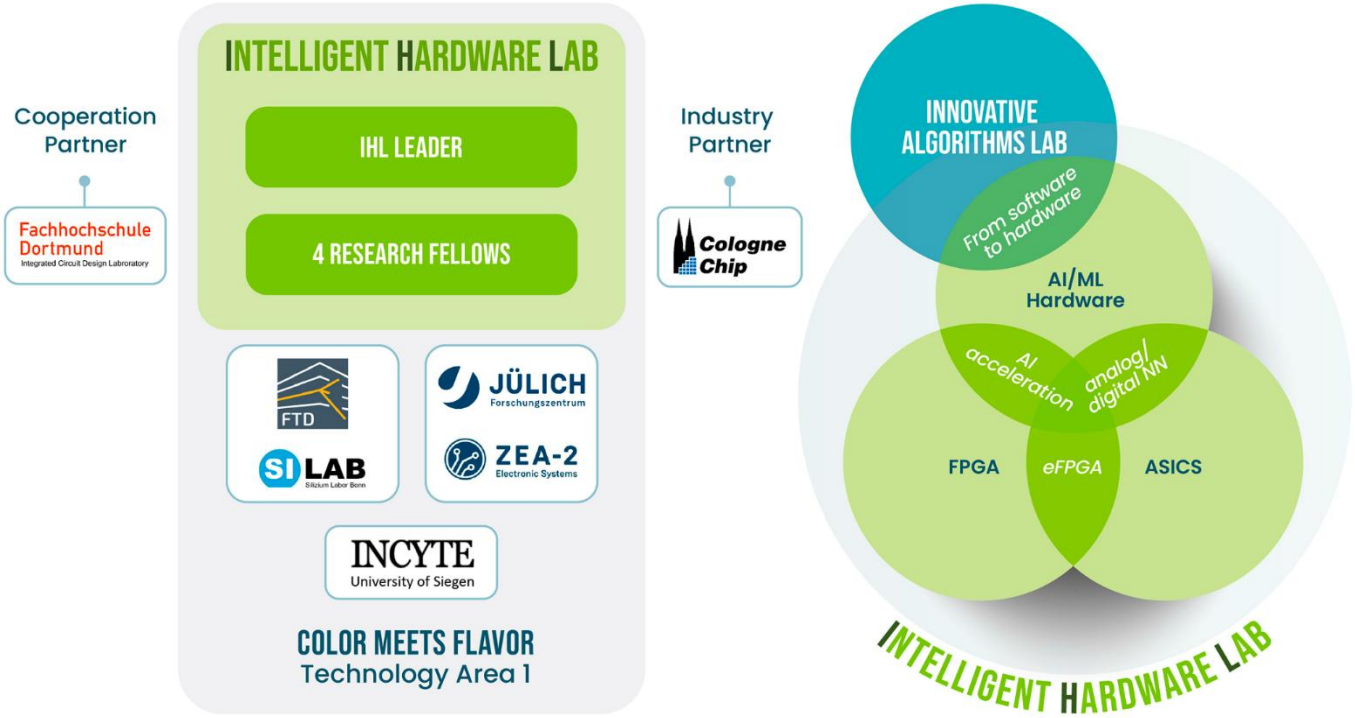
FPGA versus **e**(mbedded)FPGA

- classic FPGA
  - **discrete IC embedded in an electronic system (PCB)**
  - SoC (ARM) CPU + FPGA Fabric
- commercial Vendors
  - AMD/Xilinx
  - Intel/Altera
  - Lattice
  - Cologne Chip AG

- application in detector electronics
  - data acquisition
  - trigger
  - ???

- embedded FPGA
  - **FPGA IP block embedded in an SoC (ASIC)**
- open-source flows
  - openFPGA
  - Faboulous
- commercial vendors
  - QuickLogic
  - Achronix
- application in detector electronics
  - enhance reusability of detector ASICs
  - acceleration of algorithms
  - ???

FPGA as a cross-sectional technology in IHL



- hardware/software co-design for advanced AI/ML algorithms
- built up expertise in AI/ML algorithms.
- built up expertise in efficient accelerator hardware architectures
- automatic optimized mapping and deployment of algorithms to hardware
- design of radiation-hardened hardware (eFPGAs)
- advanced packaging techniques

Ongoing Activities: Online Compression for SiPM Data

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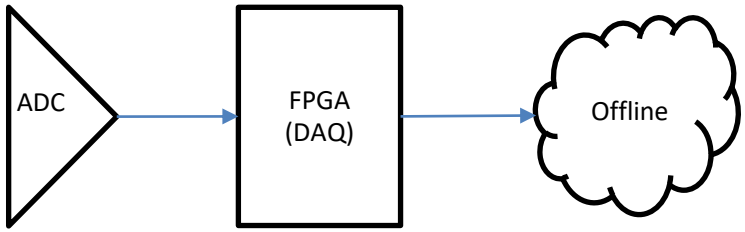
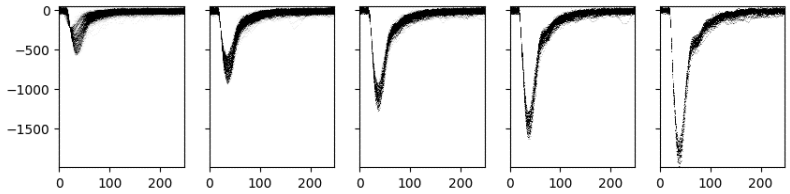
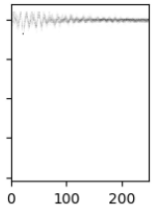
Integrated Computing Architectures ICA



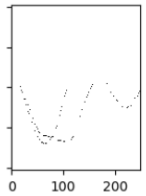
the good



the bad



the ugly



- ADC readout flexible but waveforms have significant data volume
- Idea: Classify ADC data
  - Good: parameterizable → compress
  - Bad: electronics noise → count
  - Ugly: double hits, others → send

→ reduce data volume

- Compare NN approaches:
  - Binary NN + Genetic Algorithm
    128(int7) – 32 – 32 – 2
  - hls4ml 2DCNN
    128 – 4 – 6 – 8 – 2

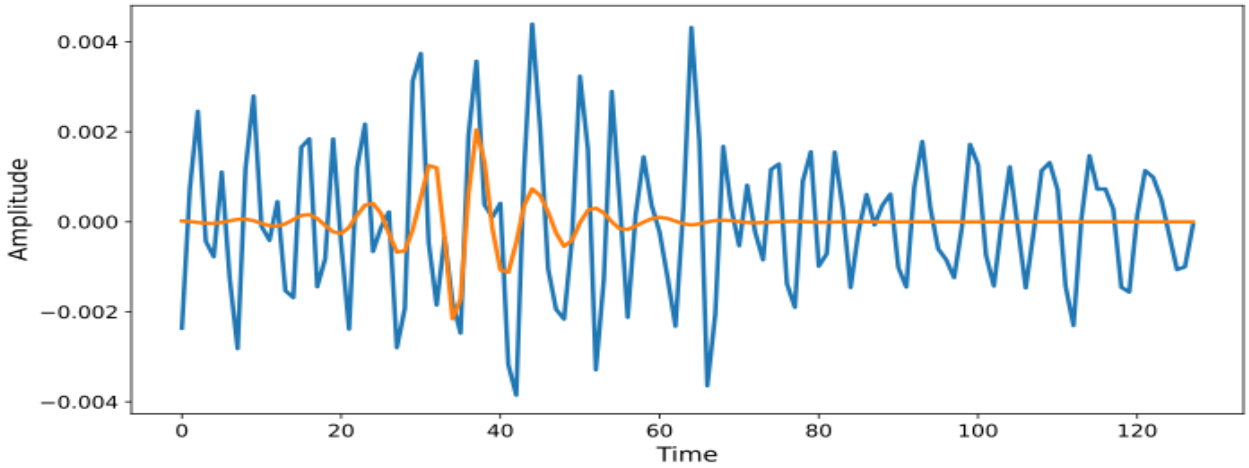
BNN+GA	hls4ml 2DCNN
74 % accuracy	95 % accuracy
16640 weights * 2bit	2696 weights * 8bit
58k LUT + 1.5k FF no DSP, BRAM	186k LUT + 112k FF 556 DSP, 120 BRAM
10 ns latency	3 µs latency
105 min * 90 cpu train.	2 min * 16 cpu training

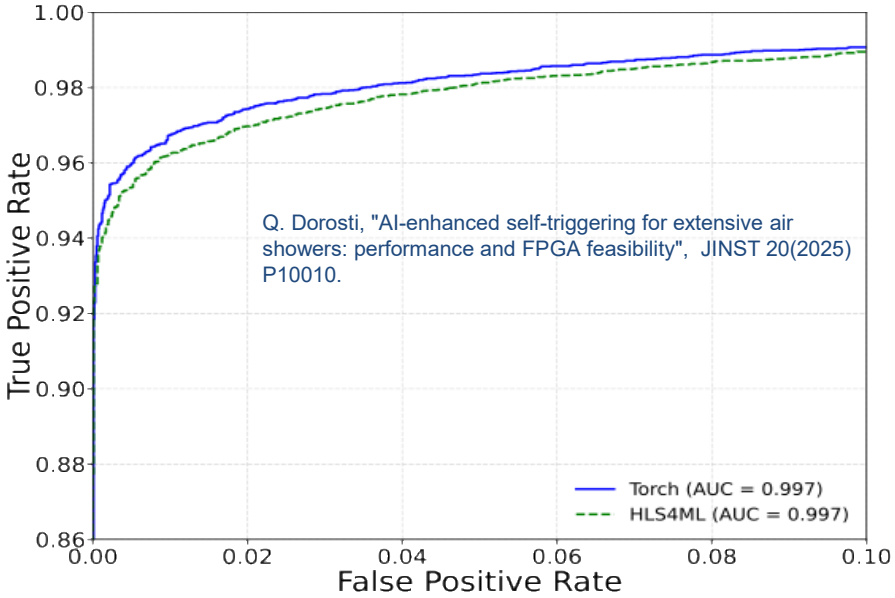
I. Bekman, et.al, „FPGA-Based Real-Time Waveform Classification“, https://arxiv.org/abs/2511.05479 (also presented at TWEPP 25)

- JINST paper + TWEPP contribution
- DFG proposal for AI-on-FPGA triggering system

Ongoing Activities
AI-Enhanced Self-Triggering for Radio Detection of EAS

Faint radio pulse (orange) embedded in noise (blue), correctly classified

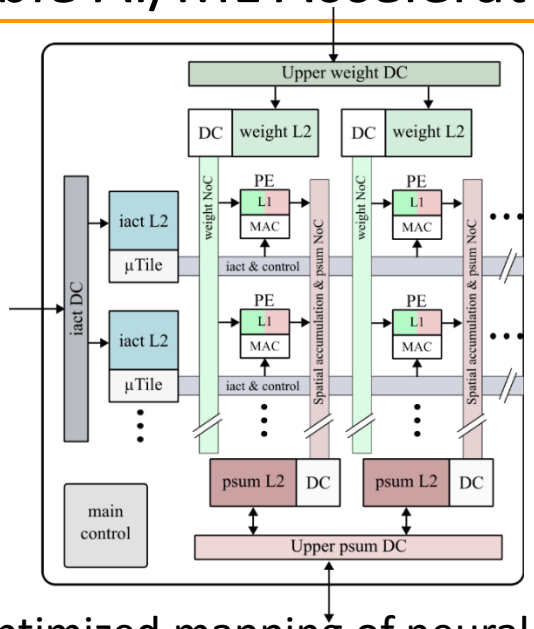


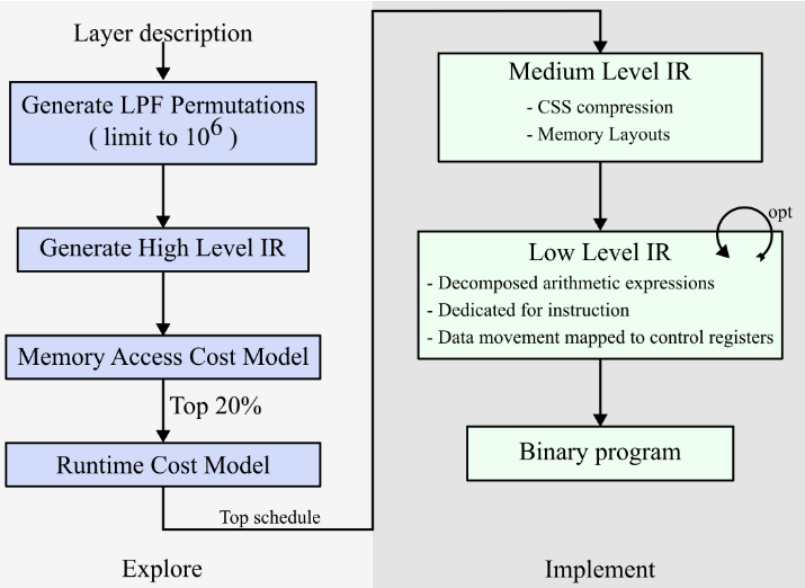


- Radio self-triggering fails in real noise conditions
- Deep-learning classifier robust to strong RFI
  >90% efficiency at <1% false-trigger rate
- FPGA synthesis feasible
  (2µs high-end FPGAs)
- Power consumption < 5 Watt

Ongoing Activities: Dataflow Optimized Flexible AI/ML Accelerator

- Process element matrix scalable in X and Y direction to define parallelism
- Scalable L1 /L2 memories sizes to influence locality of data processing and meet bandwidth requirements
- Programmability of the processing sequence during runtime e.g. spatial/temporal distribution
- Data coding that restricts flexibility is avoided e.g. bitmaps instead of RLC, CSS in the feature maps





- automatic optimized mapping of neural networks to custom hardware
- compiler translates configurations into intermediate representations
  - MLIR Framework (Multilevel Intermediate Representation)
- Evaluation using cascaded cost models e.g. for memory accesses, peak bandwidth, runtime, pre- / post-processing,

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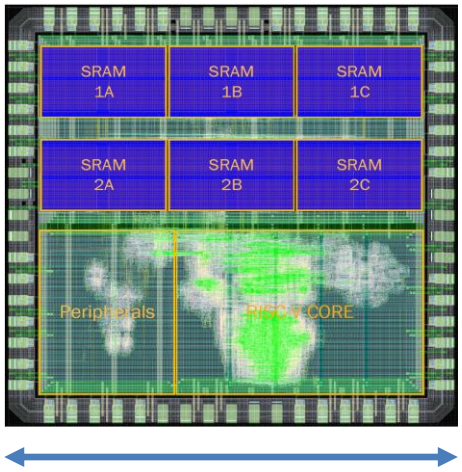
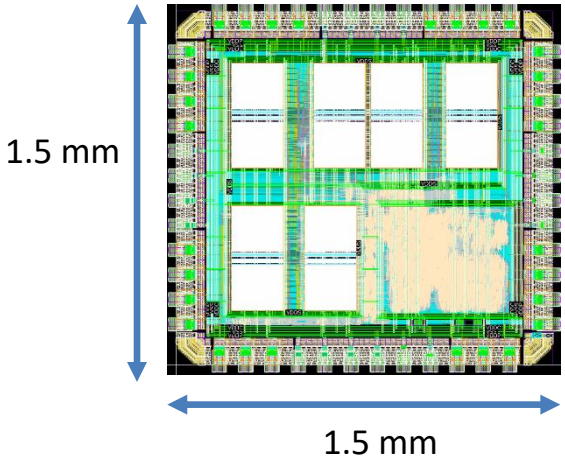
Ongoing Activities: Radiation Hard RISC-V Micrcontroller

STRV-1 (65nm)



STRV-2 (28nm)



- functional under lab conditions
- detailed characterization ongoing

	STRV-1	STRV-2
Frequency	50 MHz	100 MHz
Supply Voltage	1.2V	0.9V
Power with Scrubbing	20 mW	-
Power without Scrubbing	15 mW	-
TID hardness	1 Gigarad	-
SEE hardness	2.2 SEFI/h @ 10^9 p/cm²/s	-

Conclusion

- FPGAs are a cross-sectional technology that will be used extensively in IHL
- study of advanced algorithms and their efficient mapping to hardware
- Radiation-hardened (eFPGA) hardware is required.
- Meaningful detector physics applications must be identified and implemented.