Chip Design @ FTD

CmF Kick-off
14.11. 2025

Projects Overview

Hybrid Pixel

- ATLAS
  - RD53/ITKpix
- X-FEL
  - AGIPD
  - **CoRDIA**

Monolithic Sensors

DRD 3

- ATLAS R&D
  - LF Monopix 1 / 2
  - TJ Monopix 1 / 2
- Belle II upgrade (VTX)
  - **OBELIX**
- *Monolithic strips (DMASS)*
- Insight
  - **OBELIX**
- *Lohengrin*
  - *improved OBELIX design*
- ‘Fast 3D‘
  - **TIA for 3D pixel sensors**

DEPFET Pixel

- Belle II PXD
  - Digital FE chip (DHPT)
- EDET
  - Digital FE chip (DMC)
  - **ADC upgrade (DCD)**

Passive sensors

- ITKpix planar pixel
- DMAPS guard rings
- “thin hybrid” sensor wafer

All silicon modules

DRD 7

- **Wafer scale RDL (iVTX)**
- *Interposer (MPI-HLL)*

“28 nm” generic

DRD 7

- *eFPGA*
- *rad. hard MCU*
- **fast ADC**

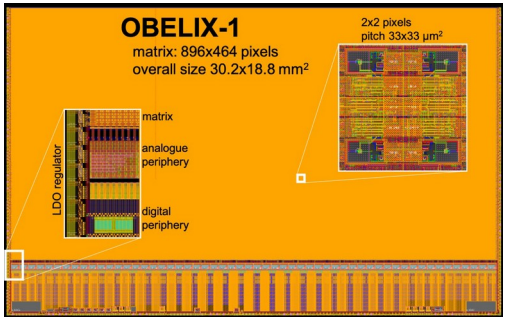
Future Directions

- Improved OBELIX chip (Lohengrin)
- 28 nm CMOS
  - fast ADC
  - eFPGA / rad. hard MCU (DRD7)
- Monolithic strip detector for g-2 (@ J-Parc)
- DMAPS for future colliders and LHC upgrades (DRD3: i.e. Octopus)
- Thin hybrids (semi-active sensor)
- Wafer scale integration (RDL, 2.5D integration)
- DCD / DMC upgrade (multi channel ADC / digital FE chip for DEPFET)

Resources

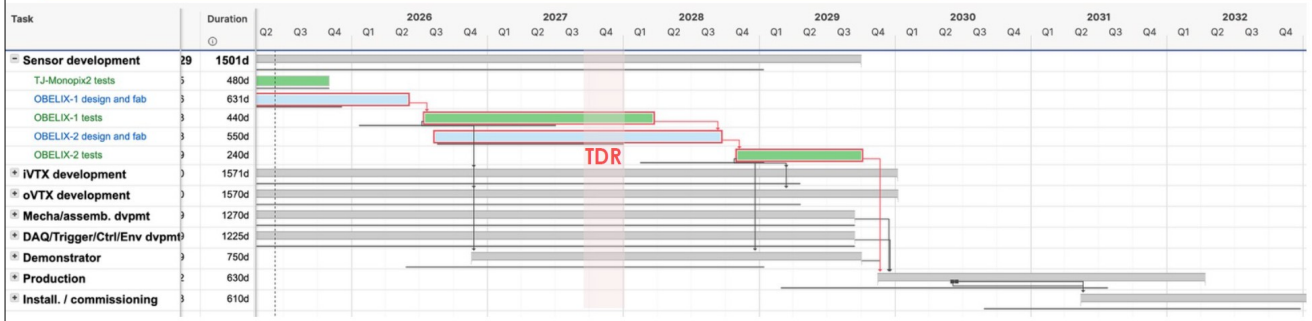
- Two leading chip designers (staff)
  - Alexander Walsemann (digital designer)
  - Tetsuichi Kishishita (analog designer)
- Postdocs
  - Vasiliki Gogolou (Marie Curie fellow, analog designer)
  - Sinou Zhang (TCAD, sensor design, monolithic strips)
- PhD
  - Kennedy Caisley (ADC design)
  - Andreas Ulm (RDL design & fabrication)

OBELIX Chip Development



	Belle-II depleted MAPS	TJ-Monopix2
Sensitive area	~30x17 mm²	17x17 mm²
Sensitive thickness	~30 µm	25-100 µm
Pitch	30 to 40 µm	33 µm
Signal digits	1 to few bits	7 bits ToT
Integration time	50 to 100 ns	25 ns
Hit rate (average)	120 MHz/cm²	> 100 MHz/cm²
Triggered read-out	30 kHz, lat. 10 µs	
Power	~200 mW/cm²	200 mW/cm²
TID fluence	~1 MGy ~5.10^{14} n_{eq}/cm²	1 MGy 3.10^{15} n_{eq}/cm²
Oper. Temp.	room+	- 20 °C

Schedule of the VTX project



- VTX project
  - Current critical path = sensor development
  - Key decision Q1/Q2 2027: do we need OBELIX-3?
    - Would delay project by ~1.5 years

- OBELIX-1 short term
  - 23-24 October 2025: Final design review
  - November 2025: adjustments / review feed-back
  - December 2025: submission process with Tower
    - ER, 12 wafers with 30 µm epi layer
  - July 2026: tests starts

Schedule is unlikely to be met