

color meets flavor

Intelligent Hardware Lab

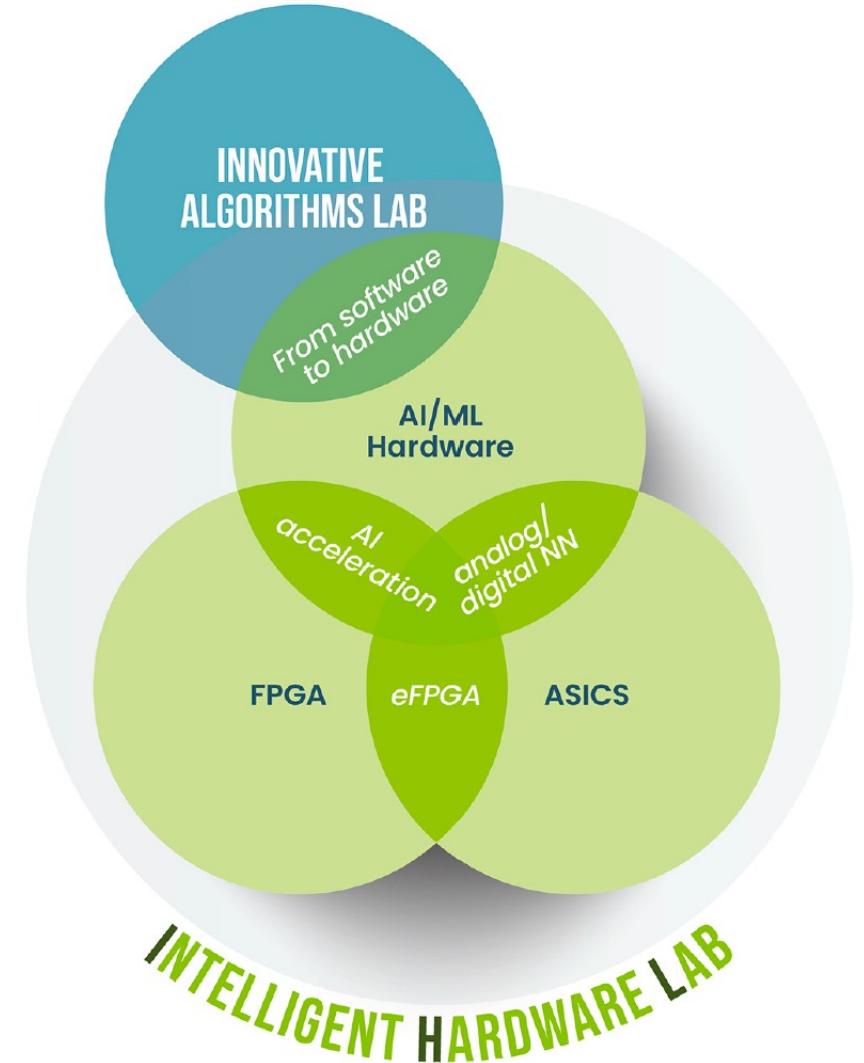
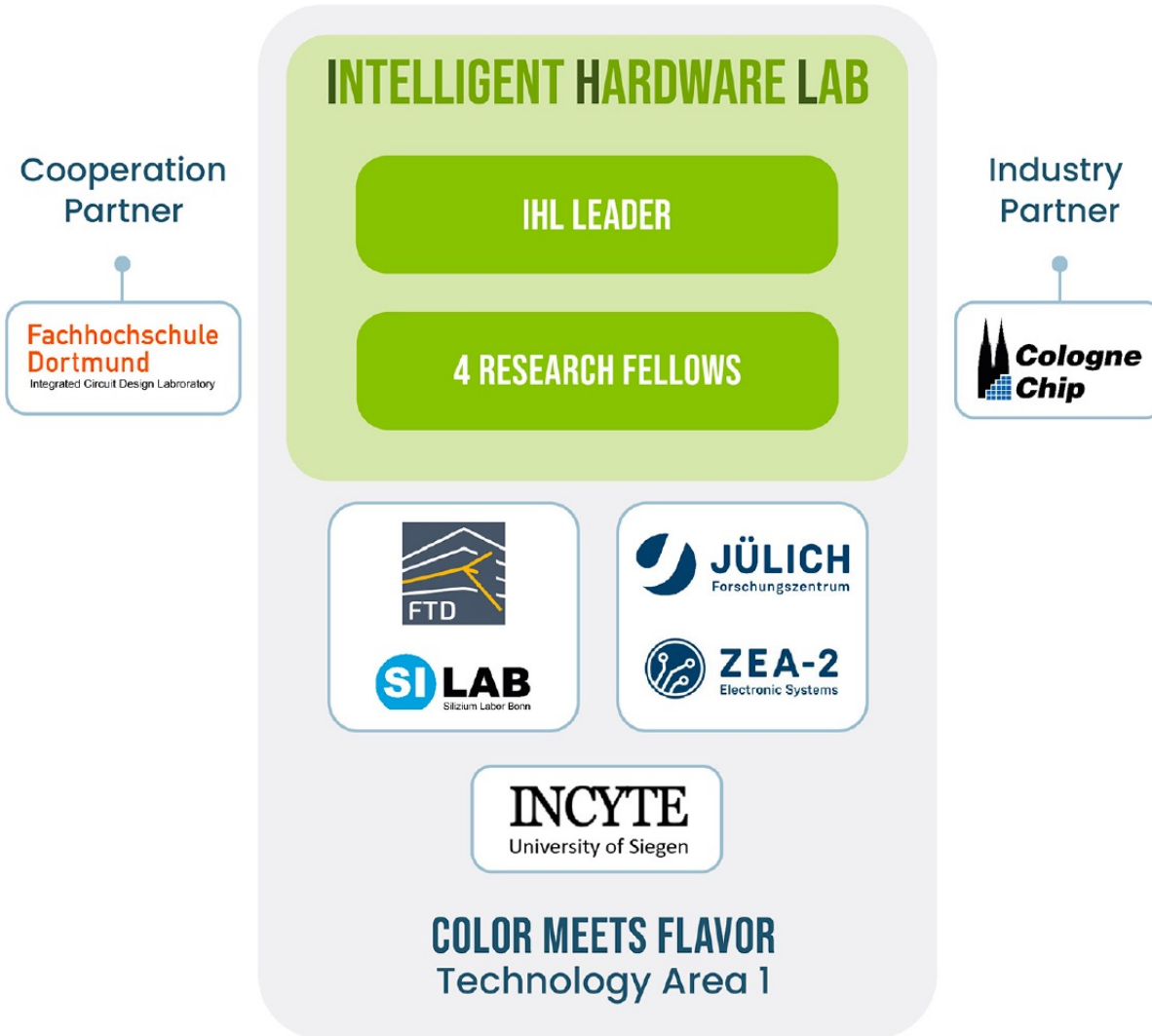
TA1 Kick-off meeting

Nov. 14, 2026

Jochen Dingfelder



Intelligent Hardware Lab (IHL)



+ FPGA & electronics expertise at all CmF sites

IHL activities & tasks

FPGA-related support

→ Talk by Michael Karagounis

- FPGA-based hardware and firmware developments for DAQ
- AI/ML-accelerated FPGA systems
- **Training** in FPGA programming

ASIC-related support

→ Talk by Hans Krüger

- ASIC design for new experiments
 - Support for (re-)use of existing pixel chips (monolithic or hybrid)
 - Provision of radiation-hardened IP (BGR, PLL, ADC, power management, eFPGAs, microcontroller cores, ...)
 - **Training** in microelectronics / chip design tools
- Use of open-source Electronic Design Automation (EDA) tools and Physical Design Kits (PDK)

Research topics (examples)

- Innovative AI/ML-based detector concepts
- ASIC implementation for AI/ML algorithms, computing in memory / neuromorphic computing
- eFPGA in front-end ASICs for programmability & reconfigurability
- On-chip intelligence (software-programmable on-chip microcontrollers)
- Code-driven design/simulation framework for analog blocks
- ...

IHL personnel



IHL Leader:

- To be elected from experts in CmF

4 Research Fellows:

- 1 already filled → Tetsuichi Kishishita (analog designer), tenured at U. Bonn (SILAB position)
- 3 to be advertised
 - 1 with tenure at U. Siegen
- Areas of expertise for the 3 fellows to be discussed

IHL resources

IHL operating budget: 120 kEUR / year

- Chip submissions
- Maintenance of FPGA and EDA resources
- Licenses

TA1 Ressources	2026	2027	2028	2029	2030	2031	2032
Staff Category	Number of Persons						
Professors ^a	0.5	1	1	1	1	1	1
Independent Junior Research Group Leaders	0	0	0	0	0	0	0
Postdoctoral Researchers	4.5	7	7	5	5	5	5
Doctoral Researchers	5	5	5	0	0	0	0
Other Staff	0	0	0	0	0	0	0

4 of these
are the IHL
fellows

^a Funding for Cluster Professors is provided by the universities.