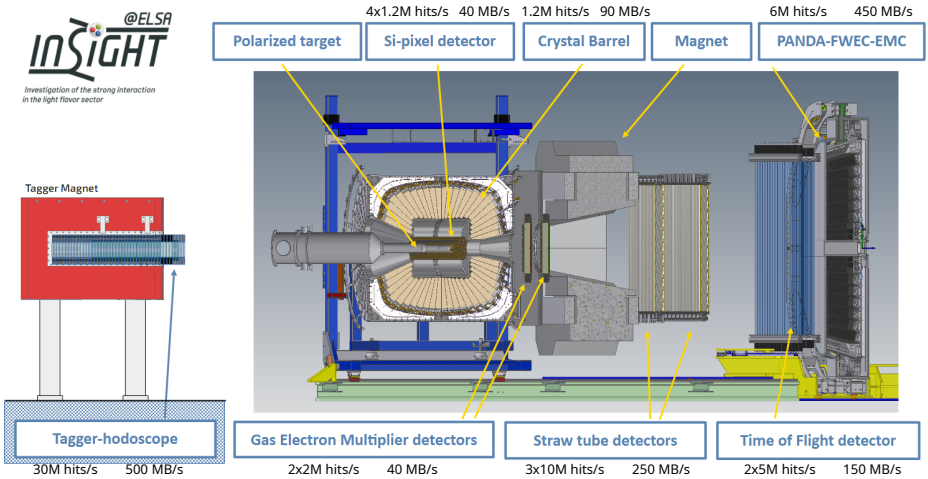
INSIGHT DAQ


@ELSA
INSIGHT
Investigation of the strong interaction in the light flavor sector
4x1.2M hits/s 40 MB/s
1.2M hits/s 90 MB/s
6M hits/s 450 MB/s
Polarized target
Si-pixel detector
Crystal Barrel
Magnet
PANDA-FWEC-EMC
Tagger Magnet
Tagger-hodoscope
30M hits/s 500 MB/s
Gas Electron Multiplier detectors
2x2M hits/s 40 MB/s
Straw tube detectors
3x10M hits/s 250 MB/s
Time of Flight detector
2x5M hits/s 150 MB/s

INSIGHT DAQ concept

Existing DAQ for CBELSA/TAPS:

- Triggered readout
  - Low-latency hardware trigger
  - Subdetectors must provide trigger signals
  - Deadtime ($\gtrsim 30\,\mu s$) after each event
- Max. event rate limited to ~ 10 kHz

$\rightsquigarrow$ Inadequate for INSIGHT

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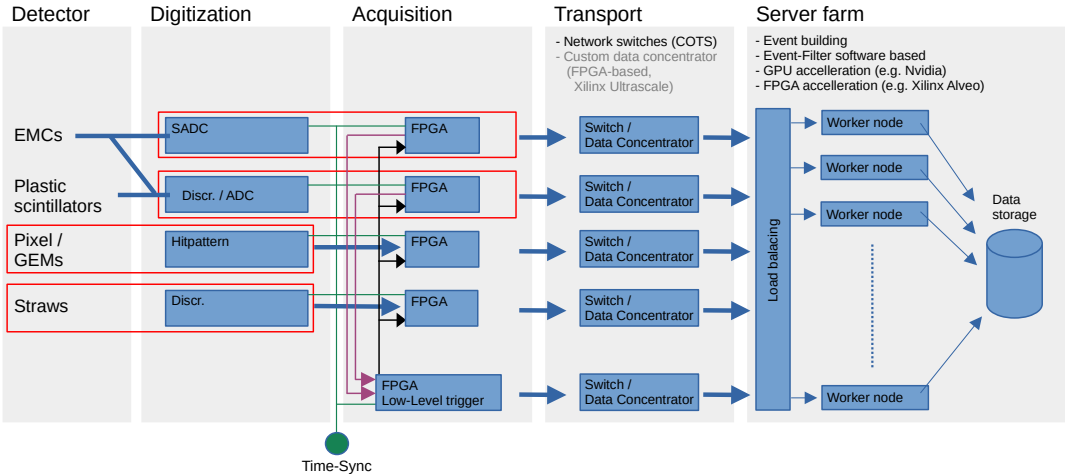
New DAQ for INSIGHT

- Triggerless, streaming DAQ
  - Free-running subdetectors (SDs)
  - Send *every* hit to back-end
  - Software trigger/ event filter on server farm
  - Time-synchronization
- Expected data rate: a few GB/s (total)
  - Custom electronics only on front-end
  - Standard hardware (Switches) and protocols (IP/UDP) for data transport

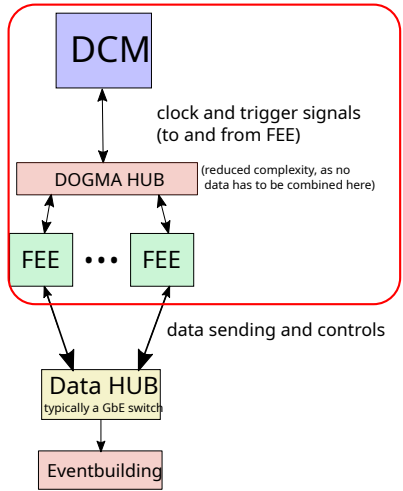
INSIGHT DAQ Pipeline



Synchronization – DOGMA

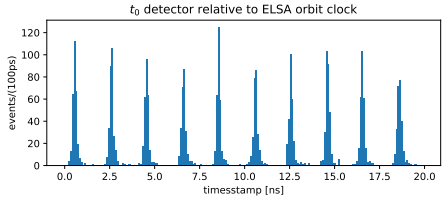
- DAQ Framework developed at GSI[Tra+24]
- Optical links for synchronization
- Bi-directional trigger signals embedded in 800 MHz clock
- Designed to work with cheap, commercially available FPGAs

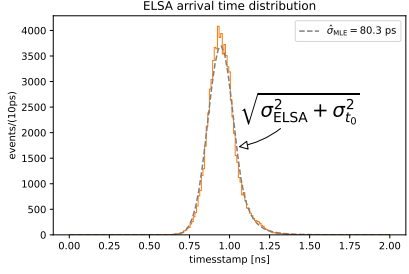
Only synchronization
⇝regular Ethernet for data



DOGMA in Bonn

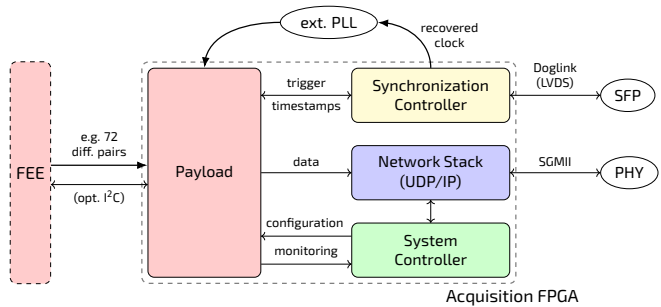
- Some practical experience
  ⇝ToF test beam
- Implemented endpoint module for SADC platform (Kintex7)
  - CB-SADC
  - FWEC
- Developed interface to ELSA-HF
  - Synchronization over ~ 300 m existing OM1/2 fiber
  - Beam synchronous measurements with ToF t_0-detector





DAQ design strategy

- Many parts of the pipeline still undefined (especially for new SDs)
- Use common hardware platforms where possible
- Don't duplicate common functionality
- Define clear interfaces between SD and central DAQ



To-Do's

DAQ group

- Continue to evaluate DOGMA
- Specify and develop common hardware components
- Develop common software components
  - Event-building
  - Software trigger
  - Reconstruction
- Evaluate solutions for Detector Control System

Subdetector (SD) groups

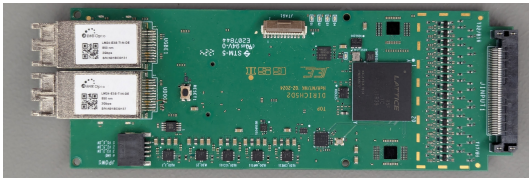
- Discuss requirements with DAQ group
- Implement SD-specific components
  - Front-End electronics
  - Firmware modules
  - Detector Control System / slow control

Backup

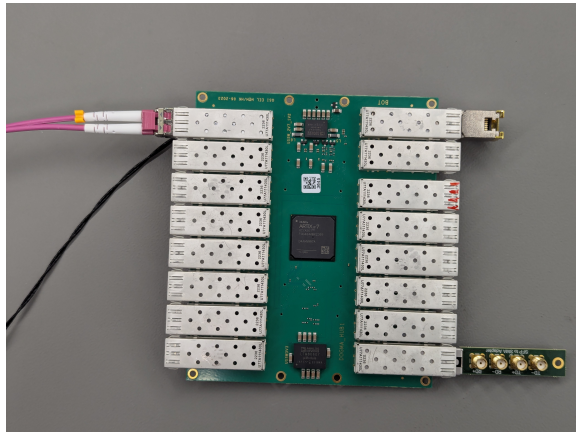
DAQ pipeline by sub detector

sub detector	digitization	acquisition	transport
Tagger (fibers)		jTDC	TCP
Tagger (bars)		jTDC (/ LVDS-DIRICH)	TCP / Dogma GBE
Pixel	OBELIX	LVDS-DC (to be specified)	UDP?
CB (Time)		jTDC	TCP
CB (Energy)	SADC	Kintex7 SADC Board	UDP
GEMs	VMM3a?	ifTDC / LVDS-DC (to be specified)	
Straws	PASTTREC	LVDS-DiRICH	DogmaGBE (UDP)
ToF	PADIWA-like?	LVDS-DIRICH	DogmaGBE (UDP)
FWEC	SADC	Kintex7 SADC Board	UDP

DOGMA-Hardware



DIRICH TDC

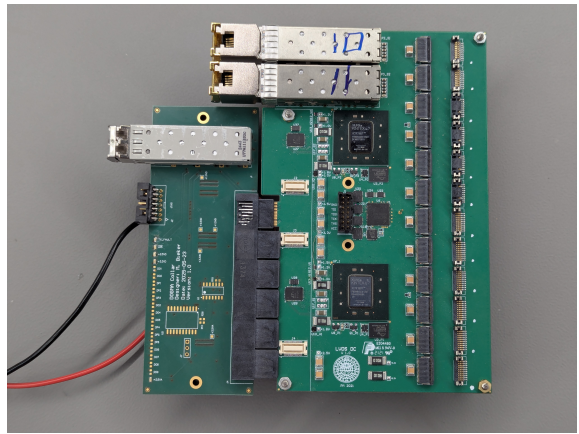


HUB / DCM

LVDS-DC (SADC Platform)

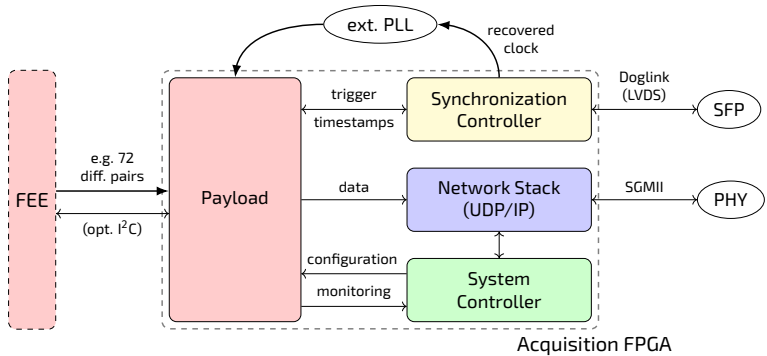
- 2 Kintex7 FPGAS[Xil21]
- Input: 2x 72 LVDS pairs
- Hardware PLL
- 2x 1GbE network via SFP
- DOGMA mezzanine
- Reference implementation: Tapped delayline TDC

- Use of SADC variant in INSIGHT:
  - PANDA FEC EMC
  - Crystal Barrel



Firmware Framework (SADC Platform)

- Network stack / event sender
- Doglink client
- Monitoring and configuration registers
- Customizable Payload
- Flavors for PANDA/CB SADC and LVDS-DC



Other hardware?

For INSIGHT DAQ:

- Communication via Ethernet (IP/UDP)
- Optical transceiver for synchronization

Potential problems

❌ GBT, Versatile Link, etc.

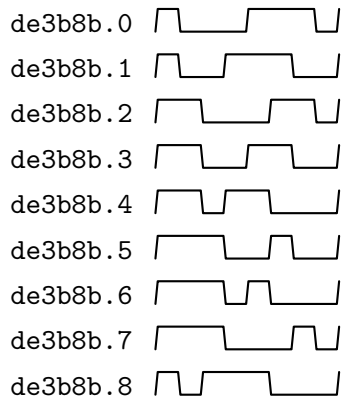
❌ Hard IP transceivers for synchronization

- Where/if possible: Re-use parts of firmware framework

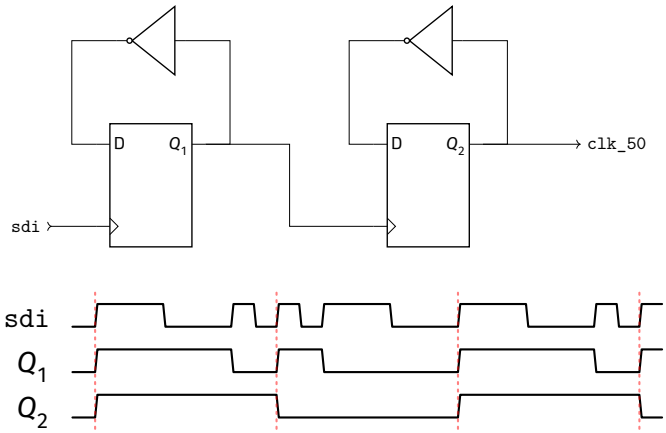
⚠️ Effort increases significantly with hardware differences

Dual-edge 3b8b Encoding

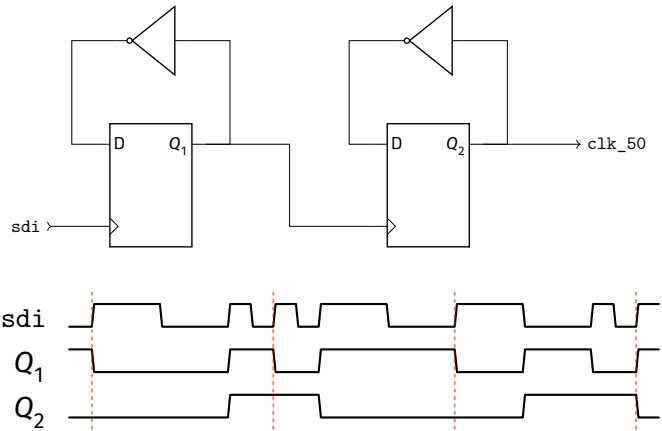
- 8 bit words
- 0-to-1 transition between words
- exactly one 0-to-1 transition within words
- DC-balanced



Clock Recovery



Clock Recovery (Wrong Edge)



Referenzen

[Tra+24] Michael Traxler et al. *The DOGMA DAQ System*. GSI Helmholtzzentrum für Schwerionenforschung GmbH. 2024. URL: https://dogma.gsi.de.

[Xil21] Xilinx, Inc. *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS182)*. 2021. URL: https://docs.amd.com/v/u/en-US/ds182_Kintex_7_Data_Sheet.