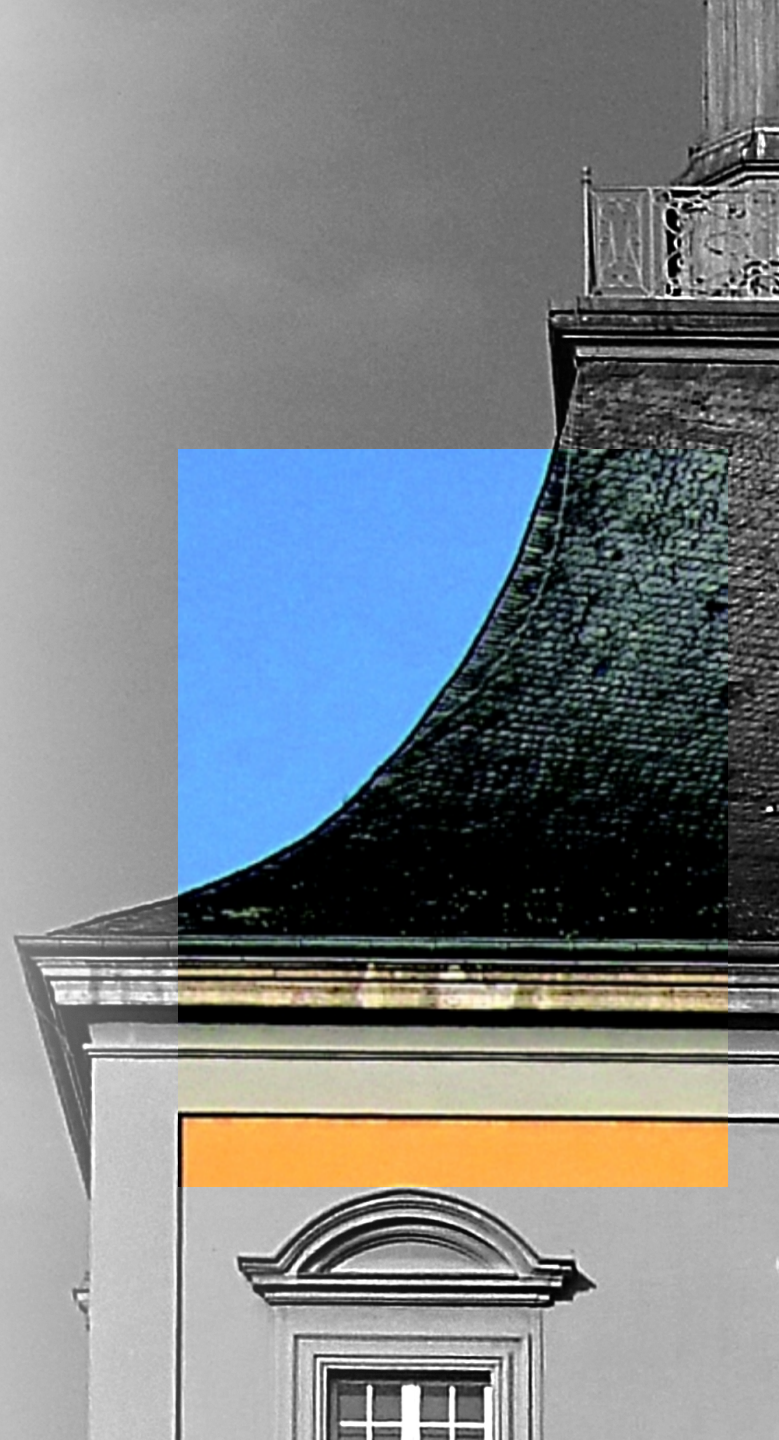


VTX MECHANICS WORKSHOP
LONDON 2025

ALL-SILICON LADDER ELECTRICAL AND MECHANICAL PROGRESS IN BONN

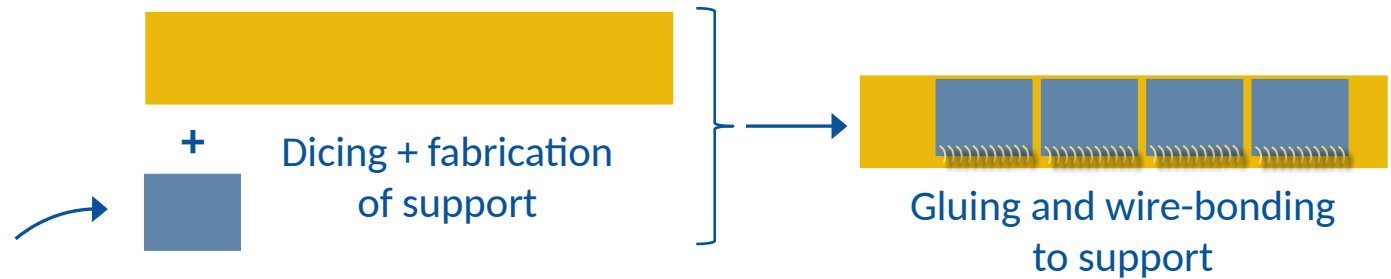
J. Dingfelder^B, H. Krüger^B, C. Marinas^V, A. Ulm^B, M. Vogt^B

Affiliations: U. Bonn (B), IFIC Valencia (V)

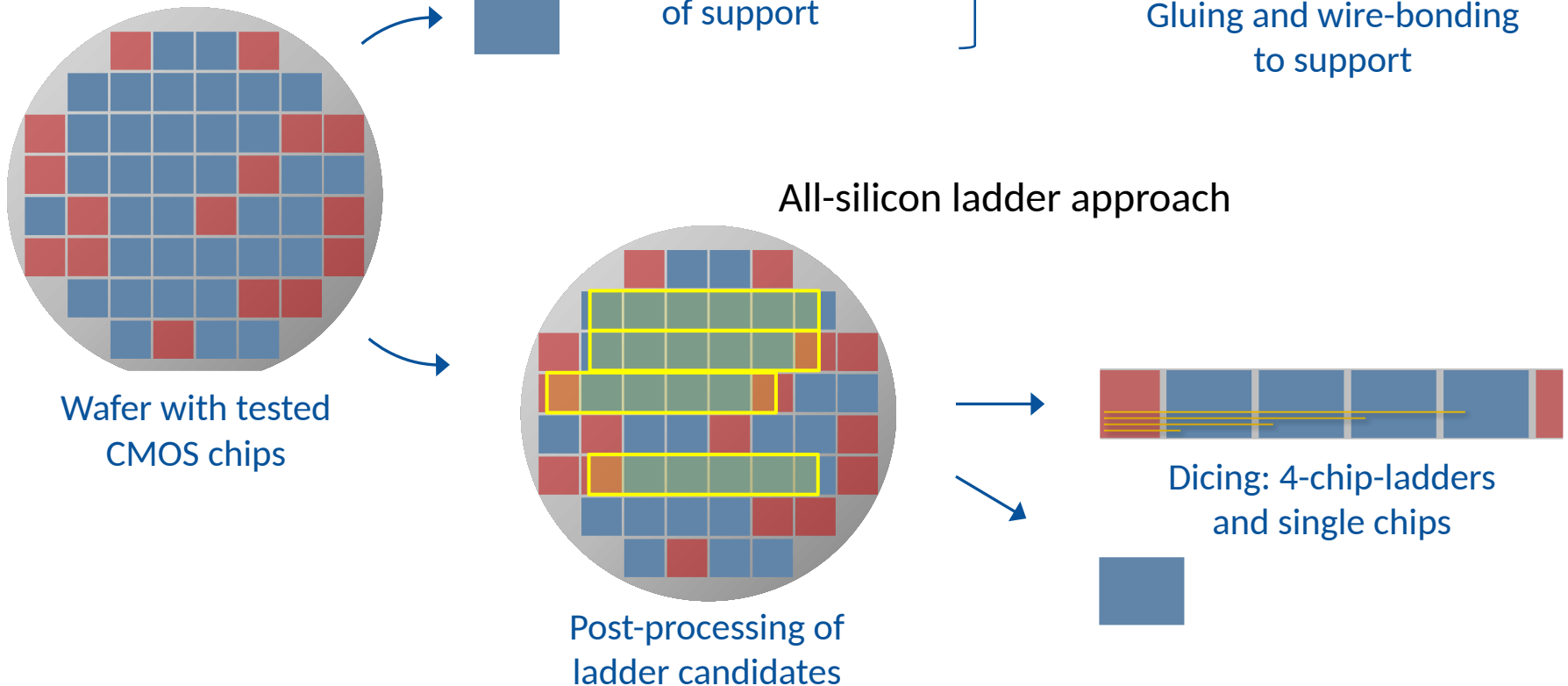


ALL-SILICON LADDER CONCEPT

Common module-building approach



All-silicon ladder approach



ALL-SILICON LADDER LAYOUT

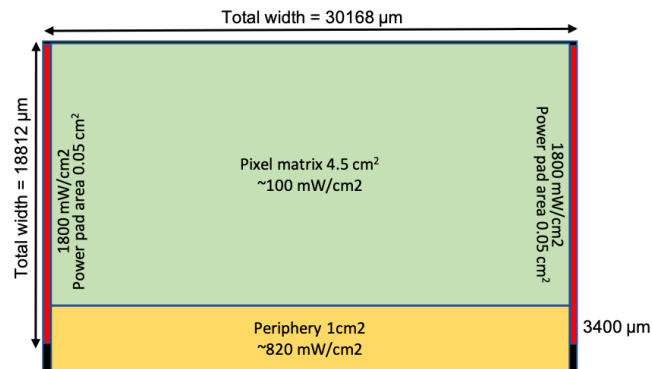
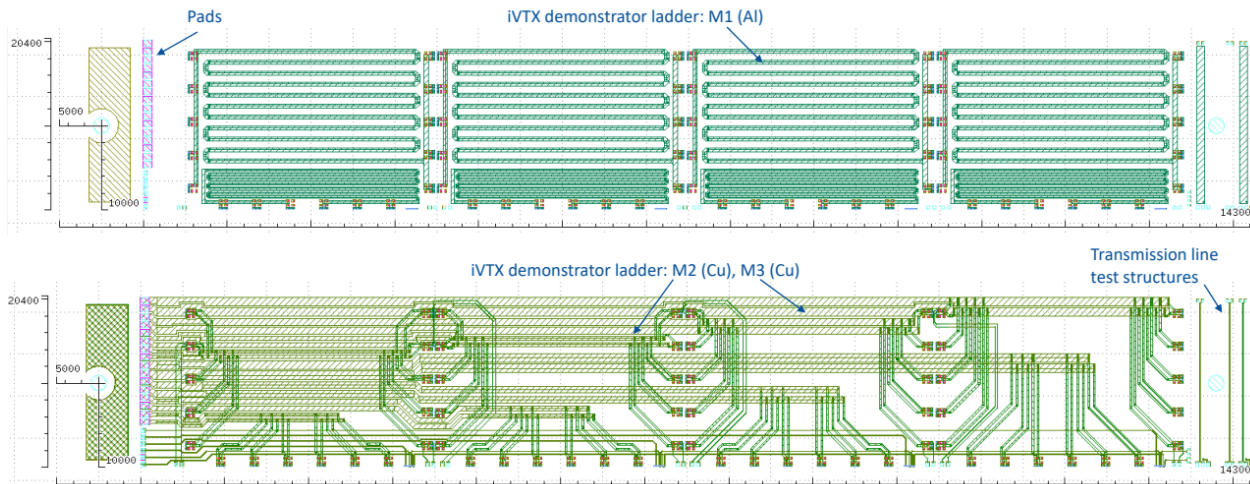
L1 might get a 3 chip ladder

First RDL demonstrator with resistive heaters instead of CMOS sensors

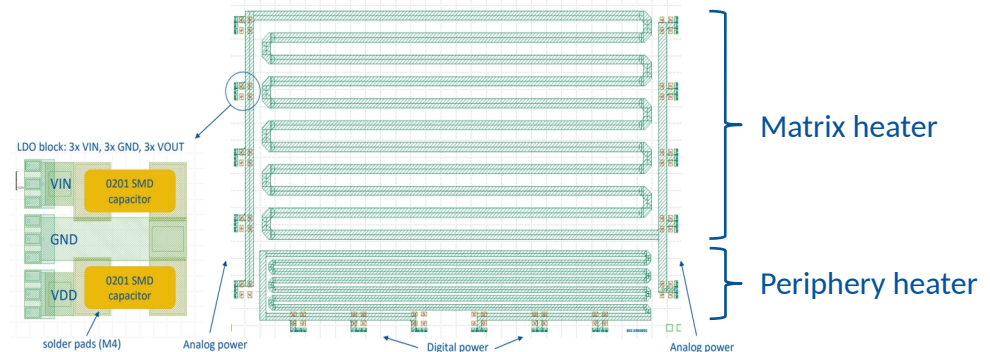
Metal system:

- Resistive heaters: 1.5 μm Al
- 2 RDL metal layers: 4 μm Cu
- Top metal finish: NiAu for wire-bonding, SMD soldering

Ladder dimension: 143 x 20.4 mm^2
Dummy heaters ($\sim 10 \Omega$): 30 x 20 mm^2



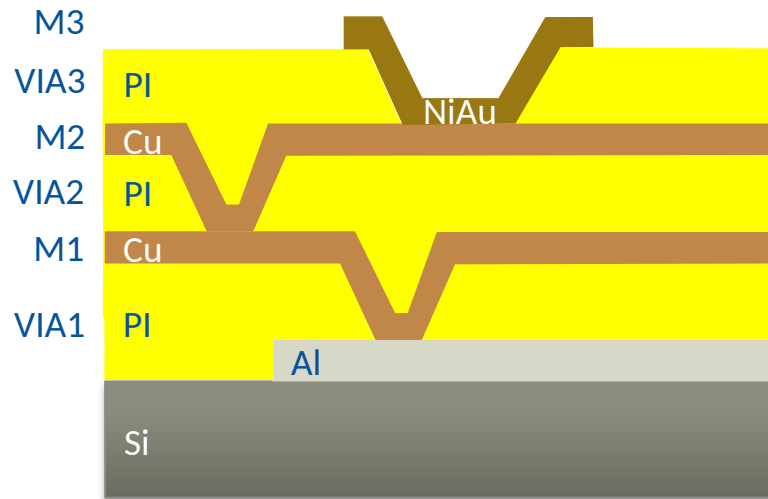
CMOS sensor example: Power domains, power pad locations



ALL-SILICON LADDER PROTOTYPE FABRICATION

Main fabrication steps:

- Alternating deposition of metal (3 μm Cu) and polymer (7 μm Polyimide)
- Photo lithography, wet chemical patterning

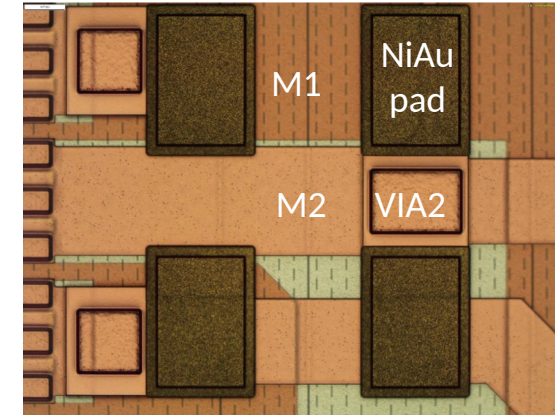
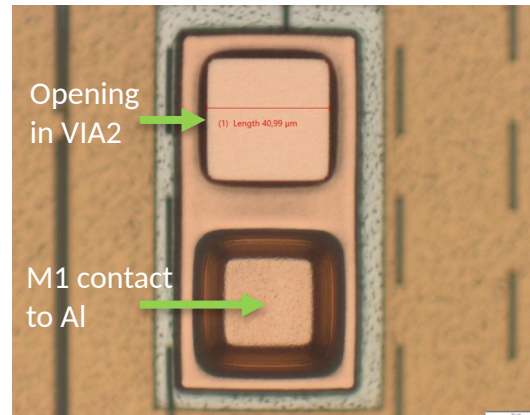
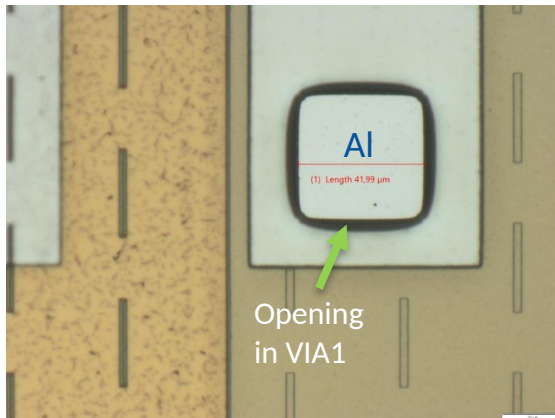
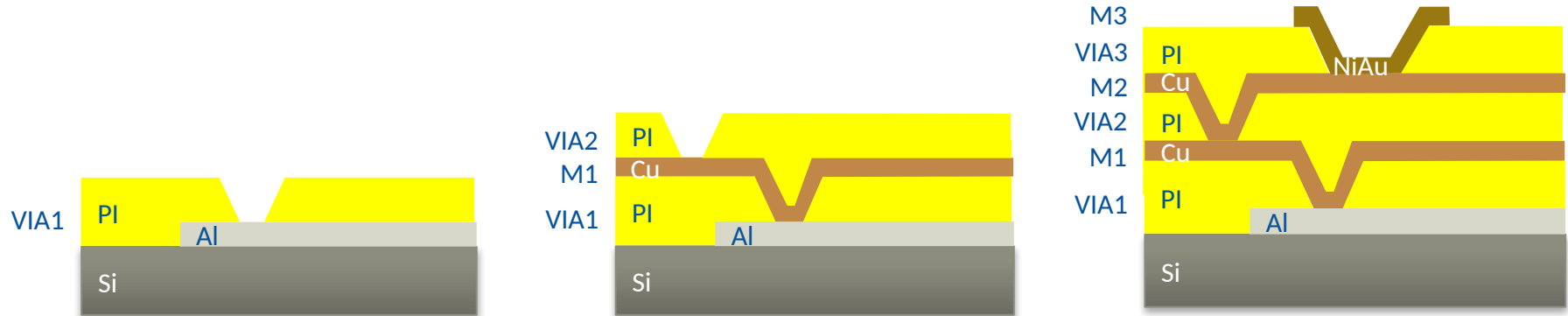


- First polymer layer “VIA1”
 - Openings above sensor bond pads
- First RDL metal “M1”
 - Contacts to sensor bond pads
- Second polymer layer “VIA2”
 - Openings to M1
- Second RDL metal “M2”
 - Contacts to M1
- Passivation layer “VIA3”
 - Openings to M2
- NiAu bond pads “M3”
 - Contacts to M2

ALL-SILICON LADDER FABRICATION

RDL process documentation of the first demonstrator produced by IZM Berlin

Characterization of layer topography, wafer flatness etc.

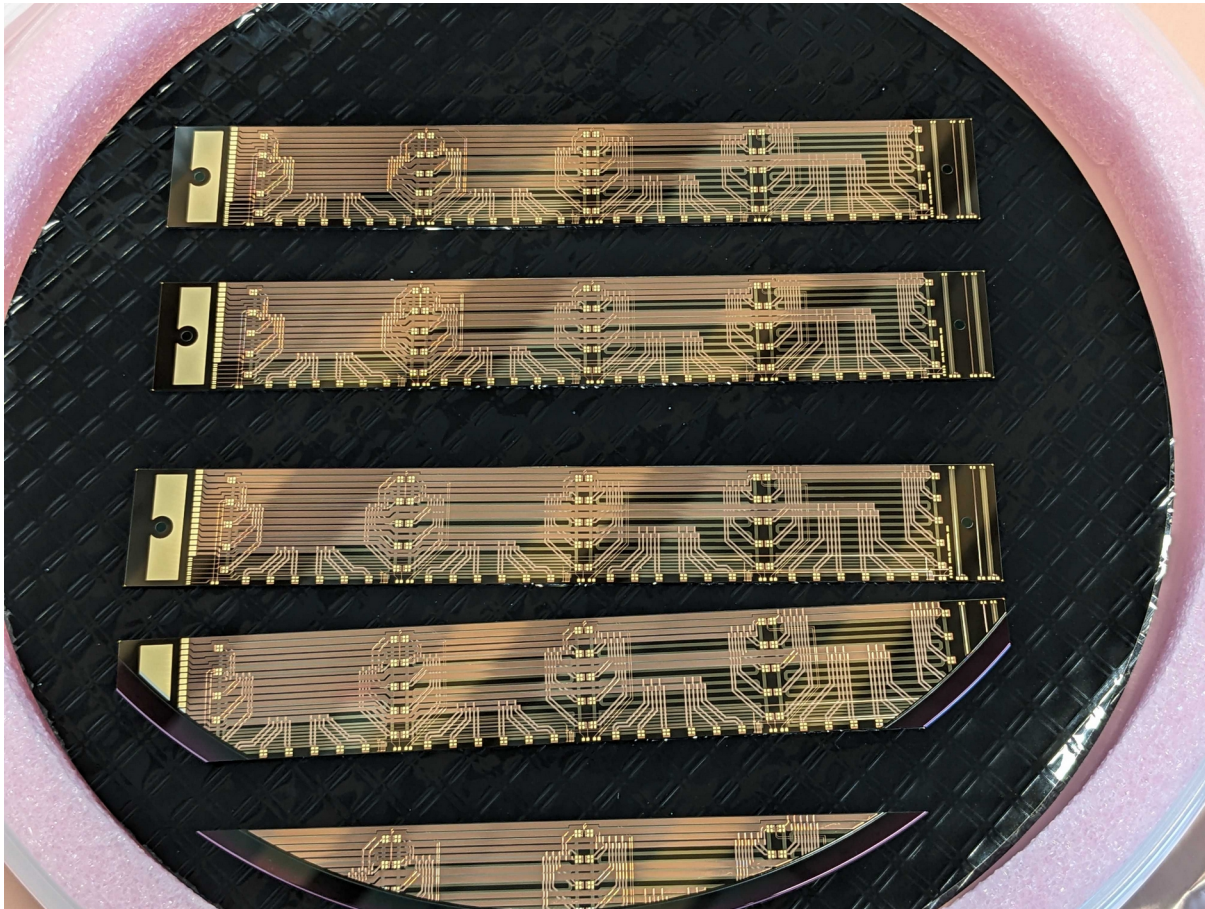


Pictures by IZM Berlin

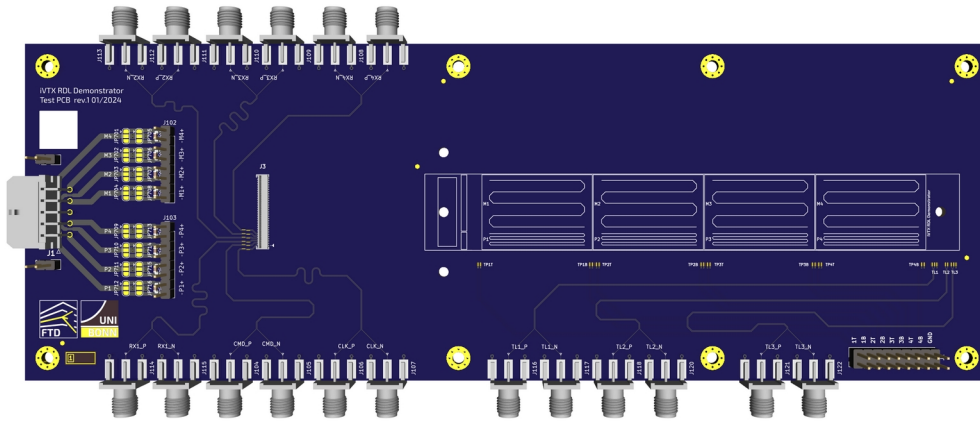
ALL-SILICON LADDER DEMONSTRATOR

First RDL demonstrators: 8 Wafers (725 μm , 400 μm , 300 μm)

Production finished smoothly

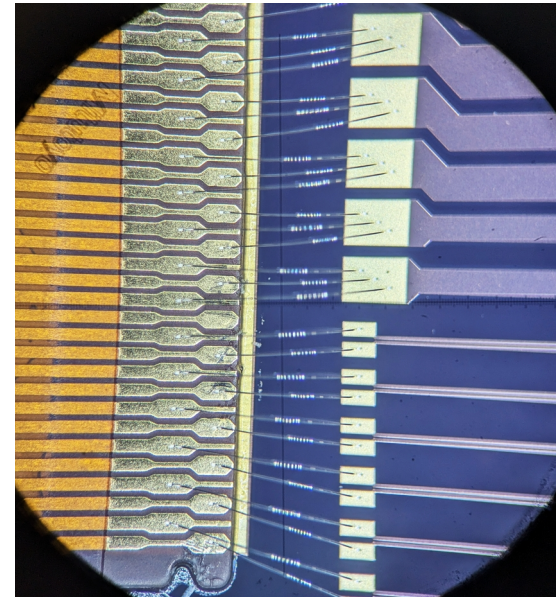
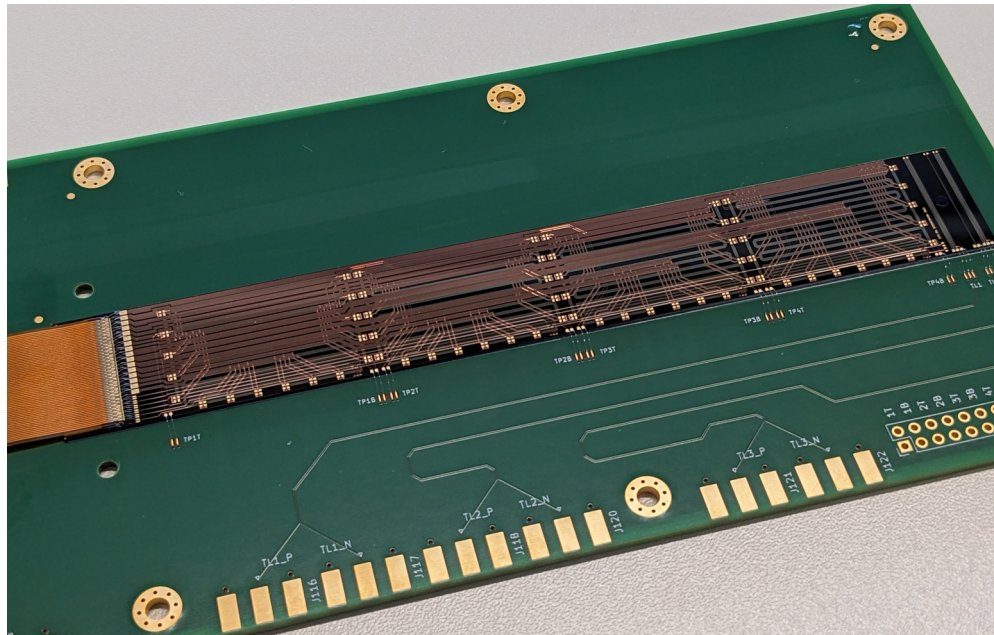


ALL-SILICON LADDER DEMONSTRATOR



PCBs for electrical tests

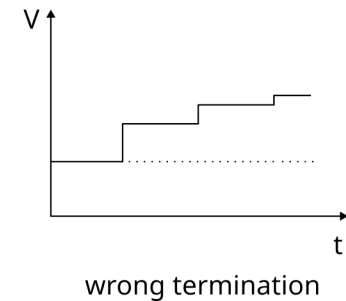
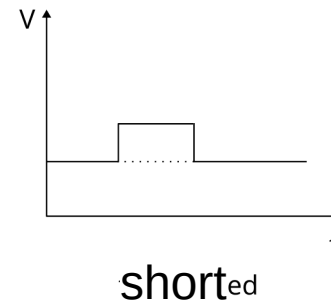
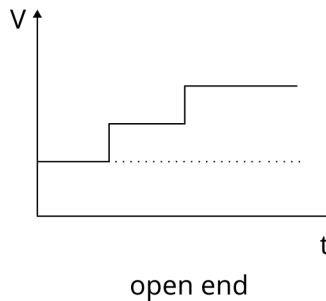
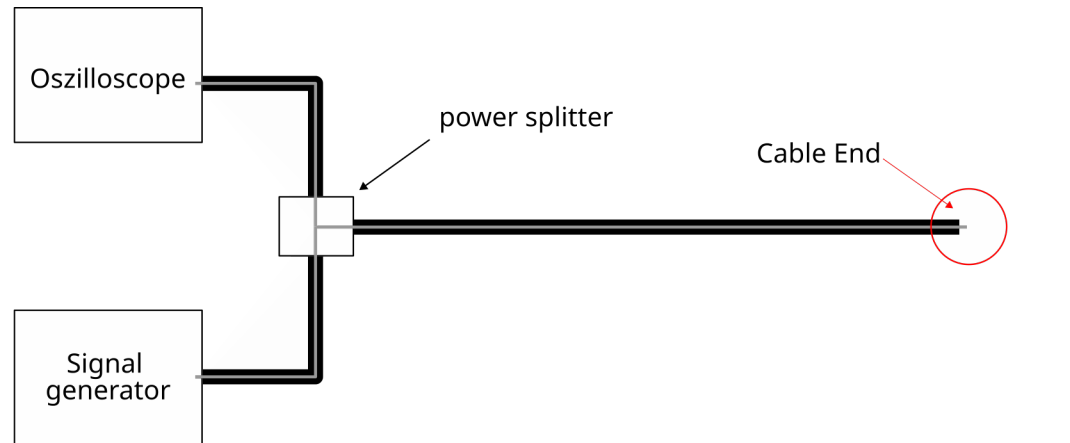
- Configurable power routing and test points for $I \cdot R$ drop measurements
- SMA connectors for differential lanes
- PCB mockups of the ladder for SMD soldering studies



- | Matrix | Resistance |
|--------|-----------------|
| M4 | 16.425 Ω |
| M3 | 16.08 Ω |
| M2 | 15.75 Ω |
| M1 | 15.083 Ω |

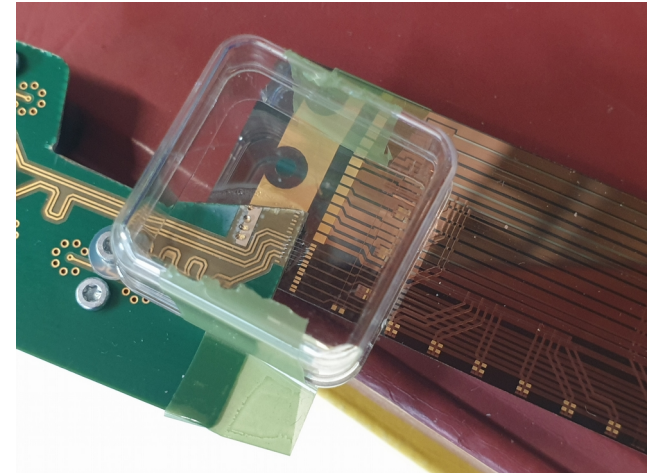
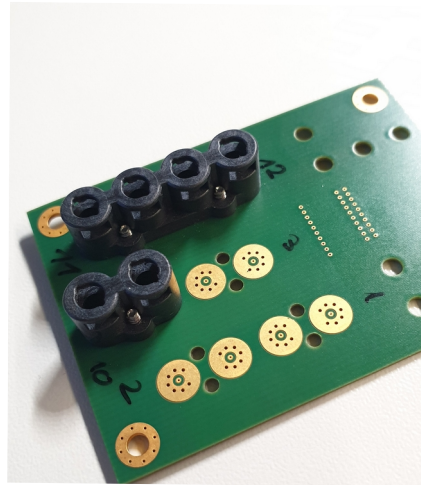
TIME DOMAIN REFLECTOMETRY

- Send electrical pulse and measure reflection
- Important is sharp edge at the beginning
- Method used to measure
 - Cable length
 - Defects
 - Shorts
 - Changes of impedance
 - Etc.



TDR MEASUREMENT SETUP

- Cut old test PCB with high frequency connector
- Wirebonded PCB to test traces



TDR RESULTS ON GOOD TEST TRACE

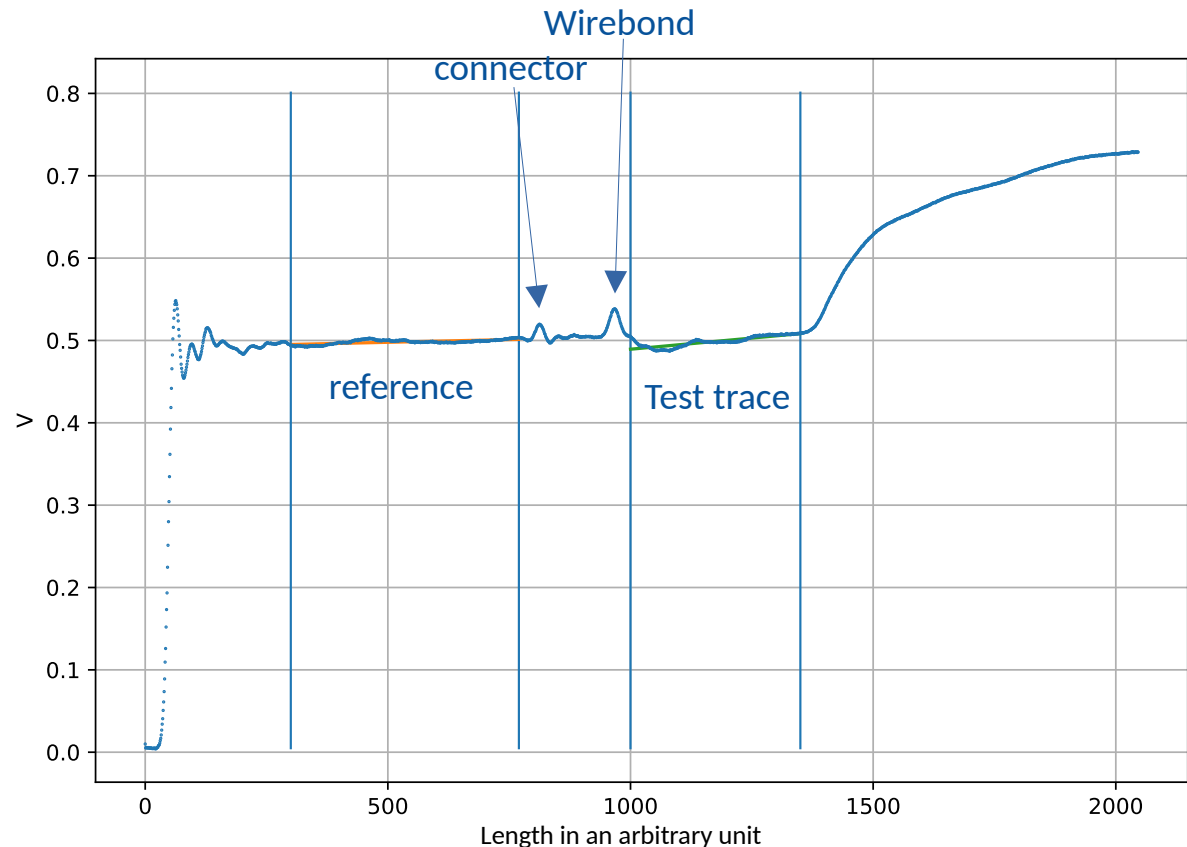
- Average over cable as reference (100 Ω , differential)
- Fit linear eq. to trace to calculate impedance of trace
- Results:
 - 96.4 Ω at beginning
 - 104.4 Ω at end
 - 100.2 Ω average

Reflection coefficient:

$$\rho_{\text{test}} = (V_{\text{test}} - V_{\text{in}}) / (V_{\text{in}} - V_0)$$

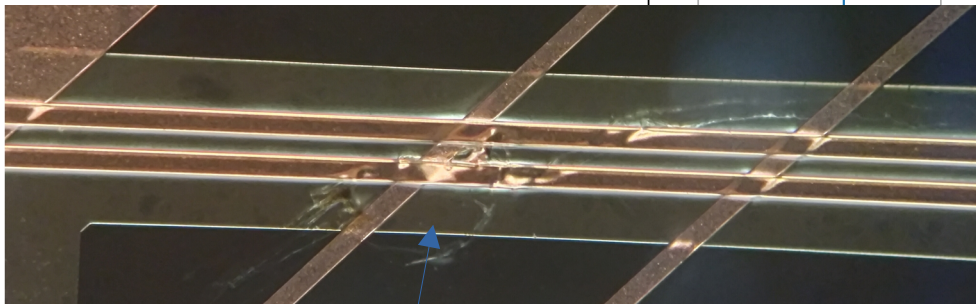
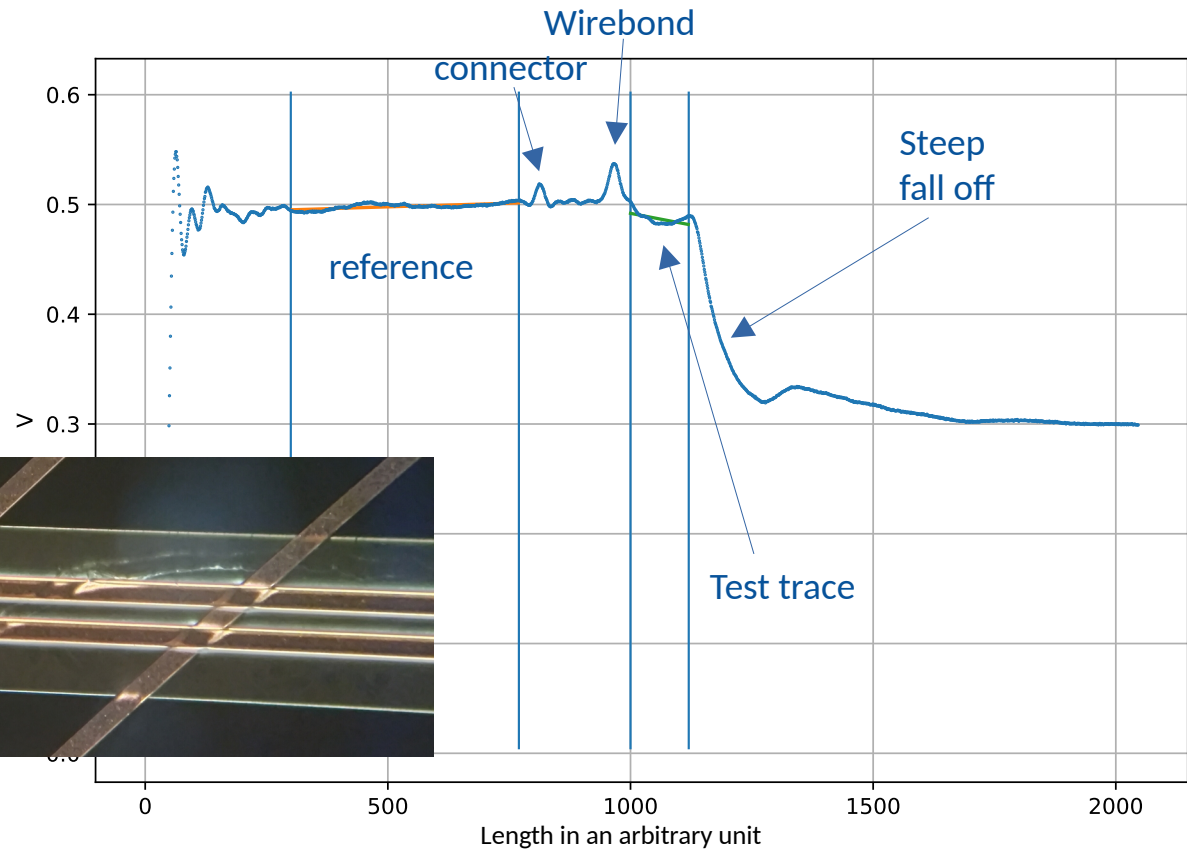
Test trace impedance:

$$Z_{\text{test}} = Z_0 * (1 + \rho) / (1 - \rho)$$



TDR RESULTS ON BAD TEST TRACE

- Test trace seems to short
- Impedance falls off at the end
→ Short circuit
- Problem shows under microscope
- Resistance between differential lines $10\ \Omega$

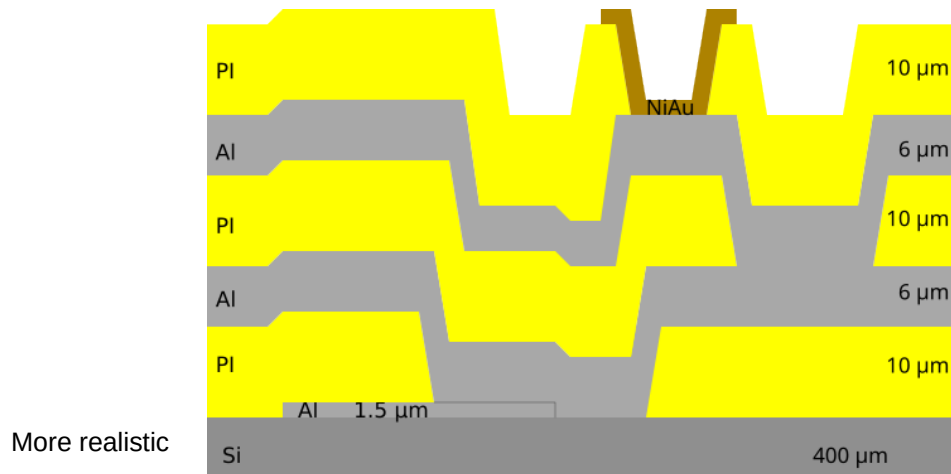
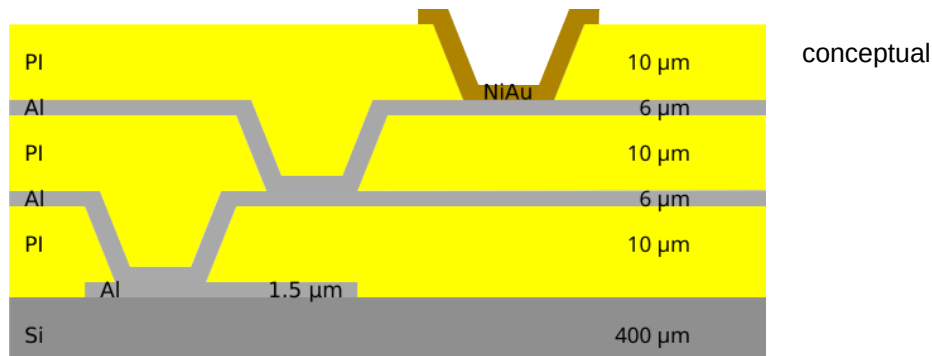


Damaged photo resist

ALL-SILICON LADDER SECOND PROTOTYPE FABRICATION IN FTD CLEANROOM

Main fabrication steps:

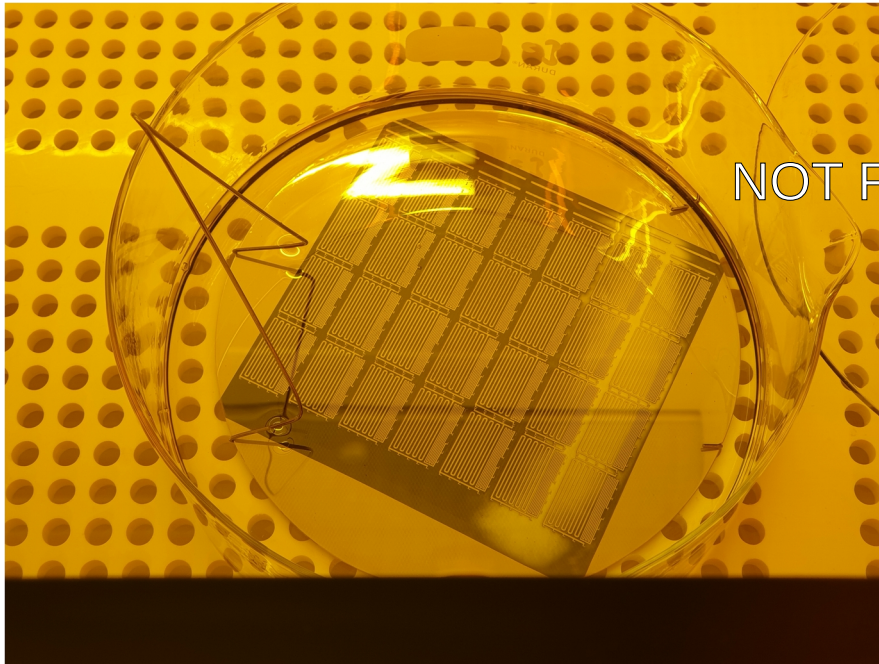
- Alternating deposition of metal (6 μm Al) and polymer (10 μm Polyimide)
- Photo lithography, wet chemical patterning



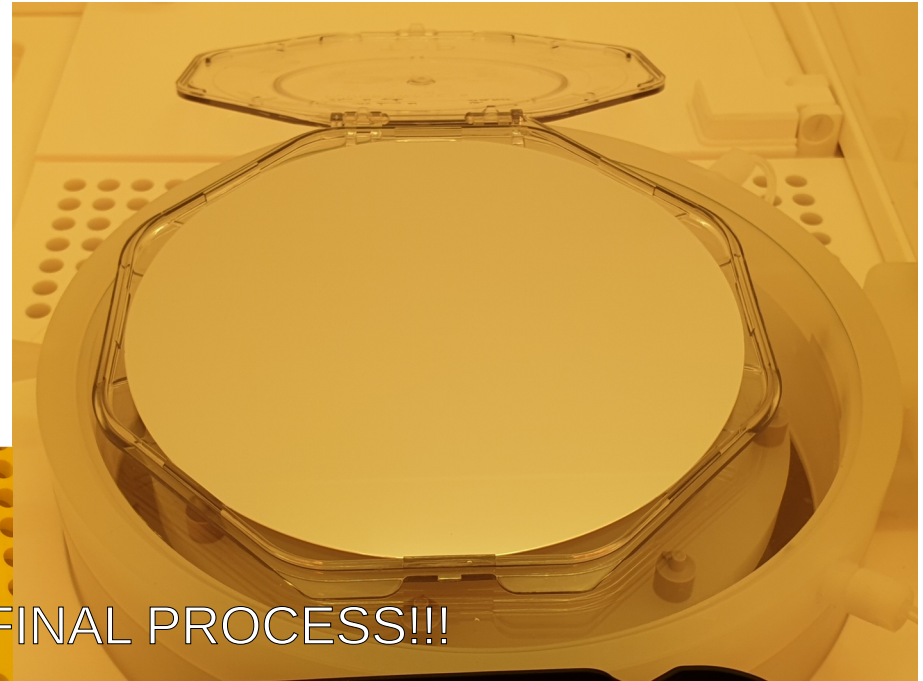
- First polymer layer “VIA1”
 - Openings above sensor bond pads
- First RDL metal “M1”
 - Contacts to sensor bond pads
- Second polymer layer “VIA2”
 - Openings to M1
- Second RDL metal “M2”
 - Contacts to M1
- Passivation layer “VIA3”
 - Openings to M2
- (NiAu bond pads “M3”)
 - Contacts to M2

ALL-SILICON LADDER SECOND PROTOTYPE FABRICATION IN FTD CLEANROOM

- 1) Deposit first metal layer
- 2) Deposit photo resist for etching



NOT FINAL PROCESS!!!



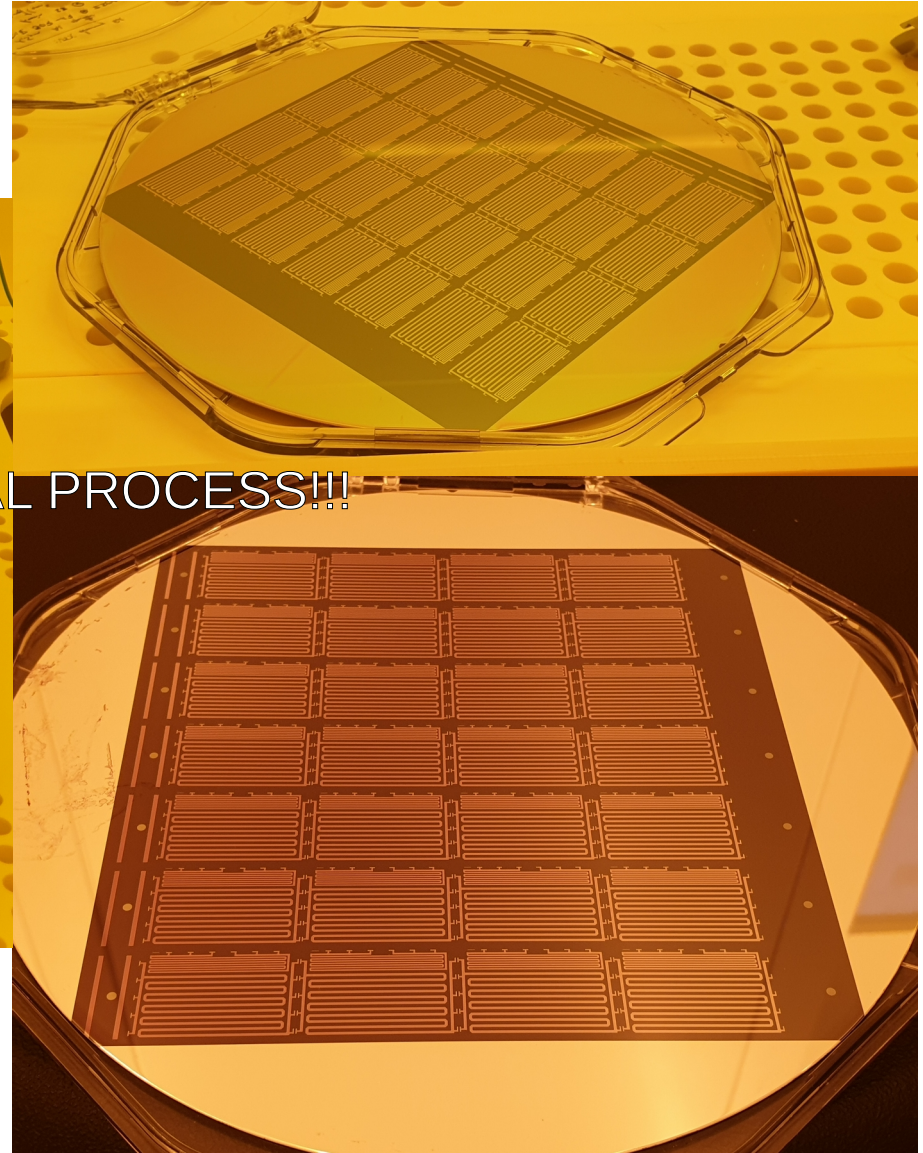
- 3) Wet etching of aluminum
- 4) Application of polyimide photo resist

ALL-SILICON LADDER SECOND PROTOTYPE FABRICATION IN FTD CLEANROOM

4) Application of polyimide photo resist



NOT FINAL PROCESS!!!



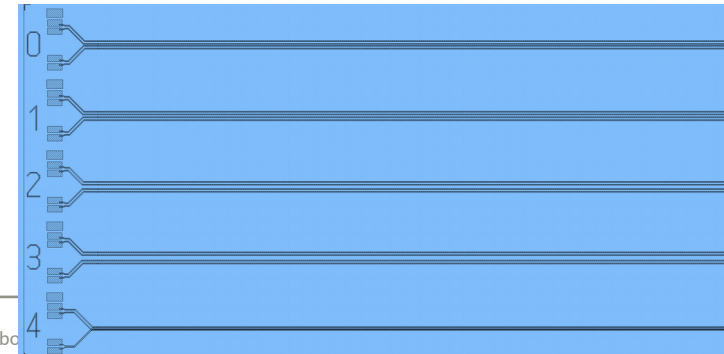
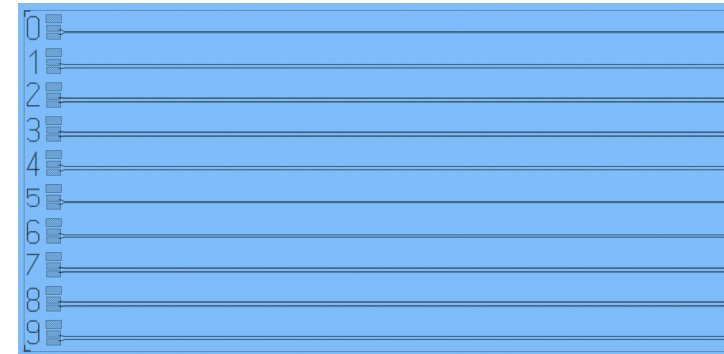
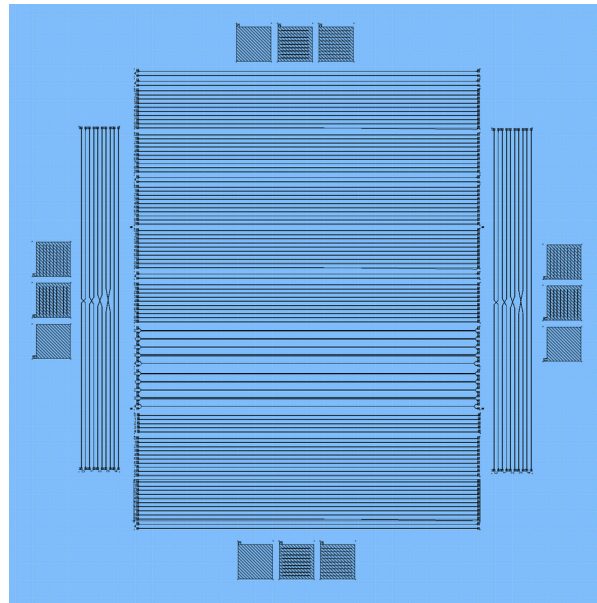
5) Baking of photo resist

6) repeat from 1)

ELECTRICAL TEST STRUCTURES

For better and more measurements we designed some test structures to test the properties of traces and our process:

- Different trace width and spacing
- Impedance matching
- Different polyimid thicknesses
- Crosstalk test structures
- Vias & Quality controll
- Capacities
- Bond pads
- Alignment

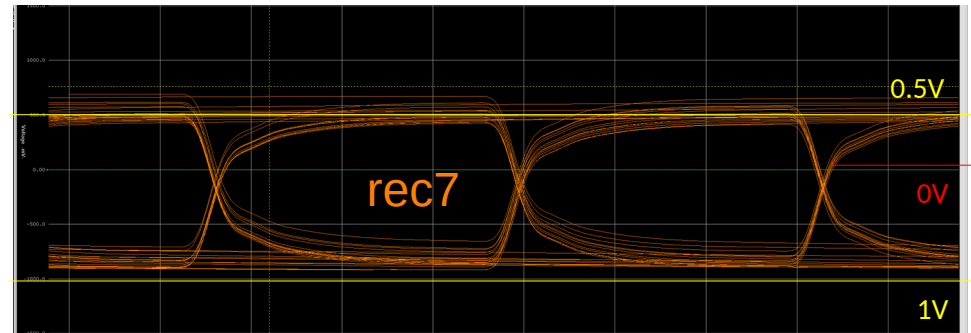
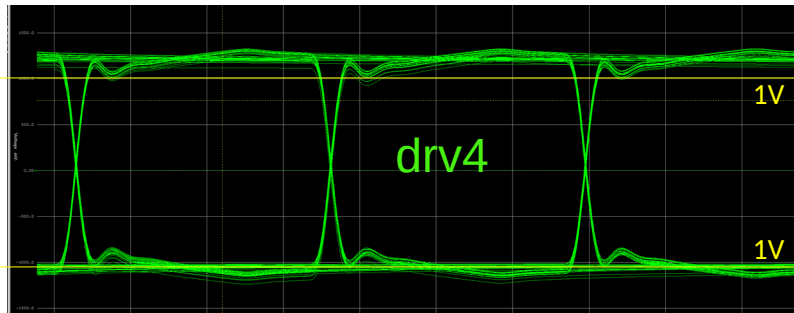
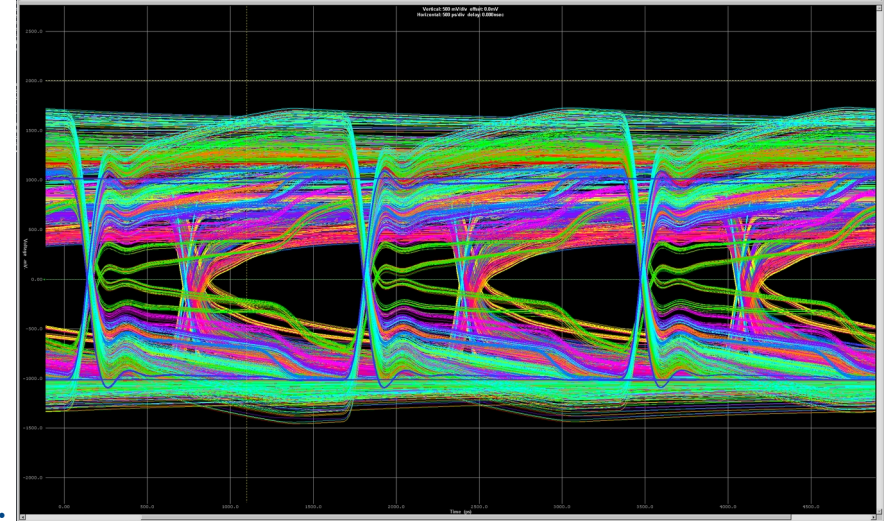


ELECTRICAL SIMULATIONS (PRELIMINARY)

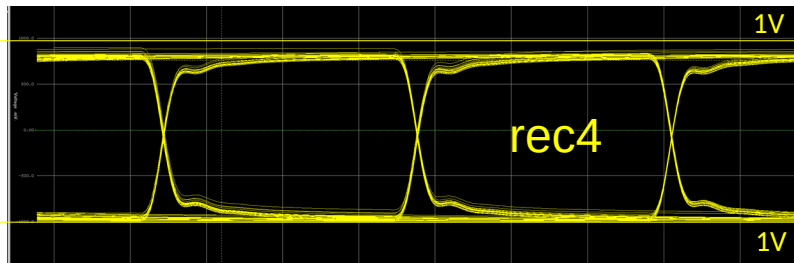
Trace design originates from simulation:

- Important features are:
 - Impedance matching
 - Rise time of signal edge
 - Signal loss over trace
- Simulation set to
 - 600 Mbps
 - 1V
 - differential

Some examples
(arbitrary names):



Rec7 shows a lot of amplitude loss over a 10 cm trace, even though the eye still looks ok



Rec4 shows a pretty nice example. A wide open eye with max and min voltage around 1V (input voltage).

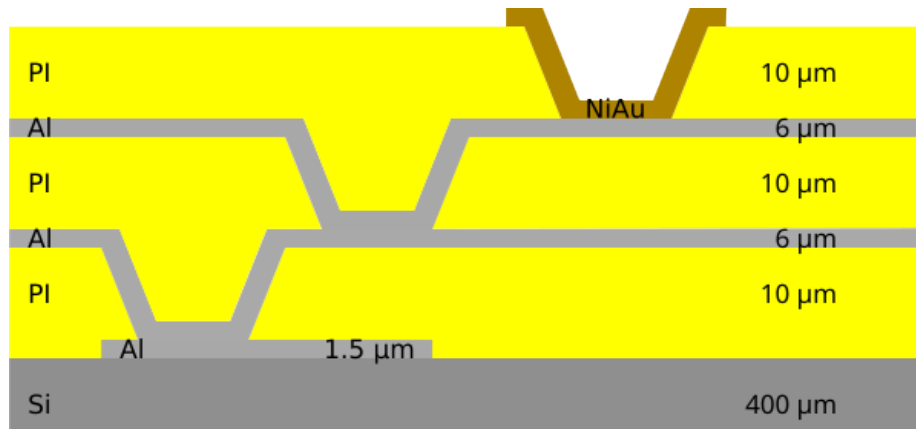
- Bonn is probably going to produce the latters for belle ii ivtx upgrade
 - Will get pad wafers (thinned and unthinned) in 2026
 - Will probably get real wafers in 2026 with obelix 1
 - “Final” top layer design will be sent soonish
-
- Need to refine processing of wafers and get reproducible results
 - Need to characterize process (ionbeam cutting to characterize photoresist and metal layer properties in crosssections?!)
 - Material constants of polyimide, AL layers, combinations
 - RDL design need to be revised with properties of our process in mind

MATERIAL BUDGET

The contributions to Material Budget:

- Main contribution Silicon:

400 μm	$0.427\% X_0$
300 μm	$0.32\% X_0$
100 μm	$0.107\% X_0$



Assuming homogeneous distribution over whole ladder. As structuring leads to places with no/less Al, the material budget on average will be lower.

- RDL Contributions:

Material	Thickness	X_0
Copper	3 μm	$0.021\% X_0$
Aluminum	6 μm	$0.0067\% X_0$
Polyimid	10 μm	$0.0035\% X_0$
NiAu	100 nm	$0\% X_0$

- RDL total:

Material	Thickness	X_0
Aluminum	2 x 6 μm	$0.0135\% X_0$
Polyimid	2 x 10 μm	$0.007\% X_0$
Total	32 μm	$0.0205\% X_0$

For Cu RDL: $0.0488\% X_0$ in total

MATERIAL BUDGET OF CAPACITORS

- Two options for capacitors on RDL:

Multi layer ceramic capacitor	Silicon trench capacitor
Advantages: - Cheap - Easy to get - Large capacities available	Advantages: - Material budget comparable to silicon - Different capacities available
Disadvantages: Material Budget very high (from calculation)	Disadvantages: - Expensive - Limited availability

Example:

- MLC made from BaTiO_3 , $W_0=233$ ($W_{\text{Ba}}=137\text{g}$, $W_{\text{Ti}}=48\text{g}$, $W_{\text{O}}=3.16\text{g}$)
- $X_0=W_0 / \sum(W_i/X_i)$ with $X_{\text{Ba}}=8.31\text{g/cm}^2$, $X_{\text{Ti}}=16.16\text{g/cm}^2$, $X_{\text{O}}=2.15\text{g/cm}^2$ *
- $\Rightarrow X_0(\text{BaTiO}_3) = 5.5766\text{g/cm}^2$ with $\rho=5.85\text{g/cm}^3 \Rightarrow X_0(\text{BaTiO}_3) = 0.953\text{cm}$

$$* X_0 = \frac{716.4}{Z(Z+1) \ln \frac{287}{\sqrt{Z}}} \text{ g.cm}^{-2}$$

- For 250um thick capacitors:

$X_0(\text{MLC}) = 2.623\%$	$X_0(\text{Si}) = 0.267\%$
-----------------------------	----------------------------

THERMAL MEASUREMENTS

Relevant for Göttingen. Should get a setup up and running at Göttingen for compare measurements with simulations.

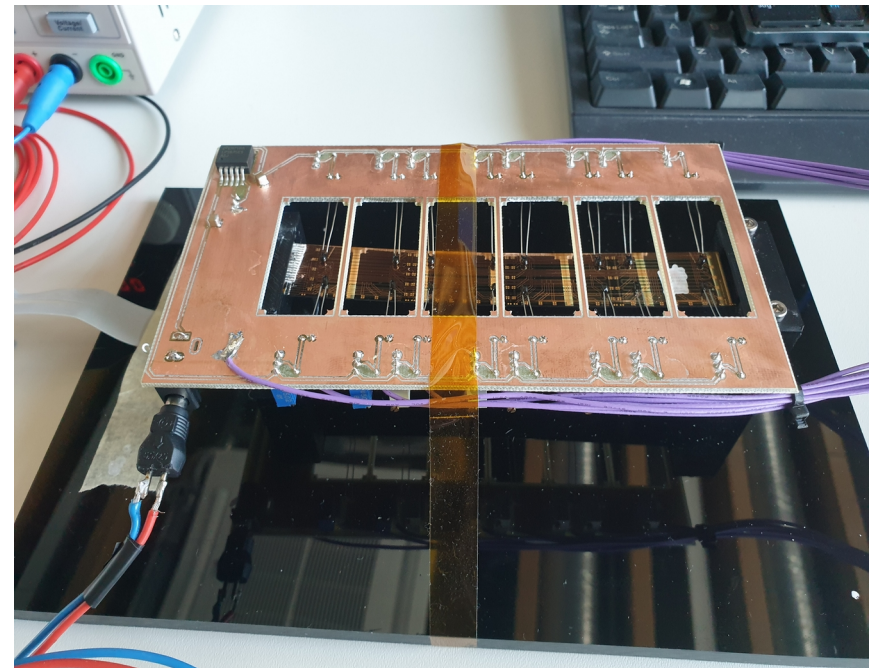
Two approaches:

Thermal Camera

- Deposit chalk on RDL to prevent reflections
- Might slightly insulate
- Nice spacial overview over module
- Not calibrated

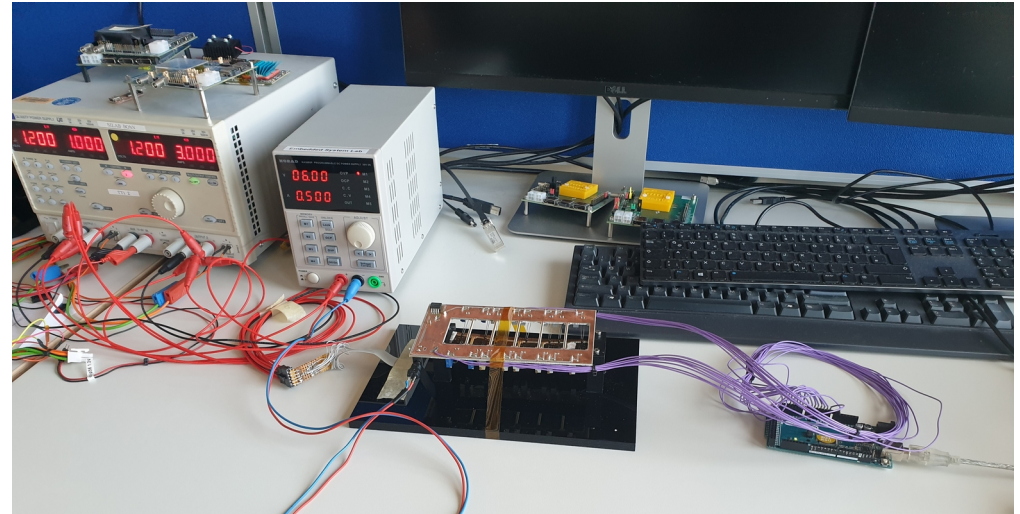
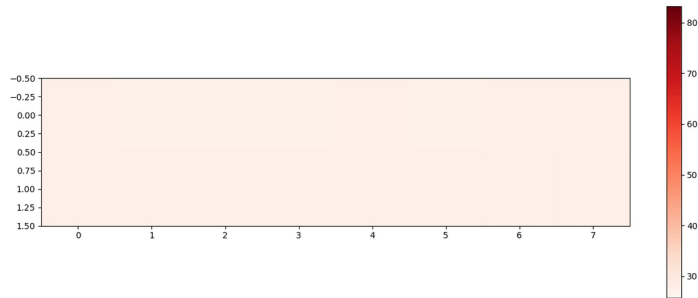
NTC Array

- No chalk
- Spacial resolution low
- NTC array calibrated in climate chamber

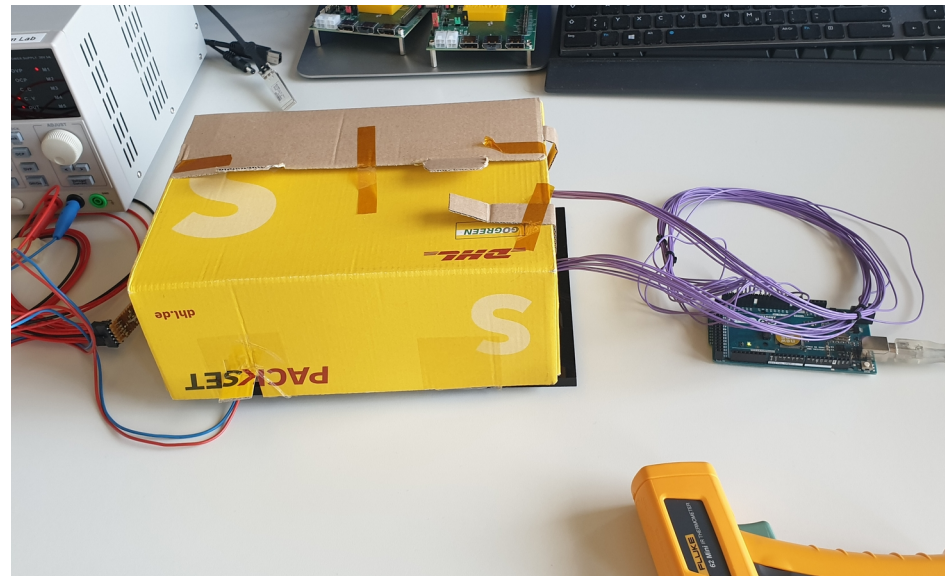
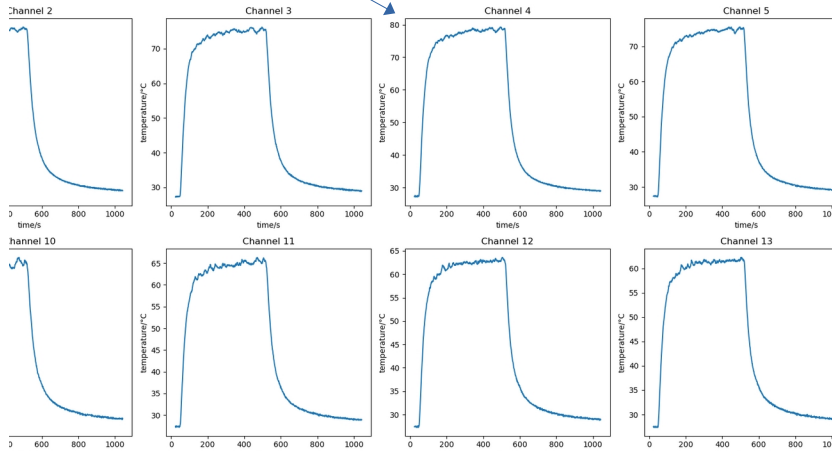


THERMAL MEASUREMENTS NTC ARRAY

Measurements with NTC array in Box to
reduce environmental effects

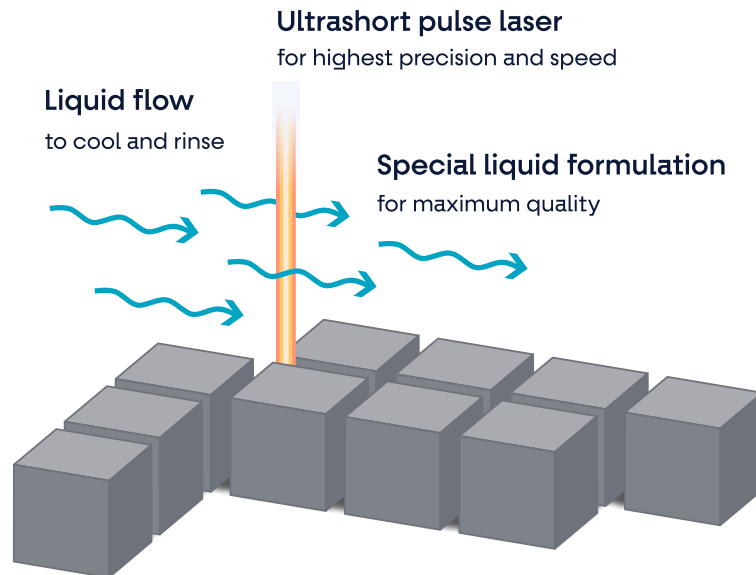


Max temperature ~80°C



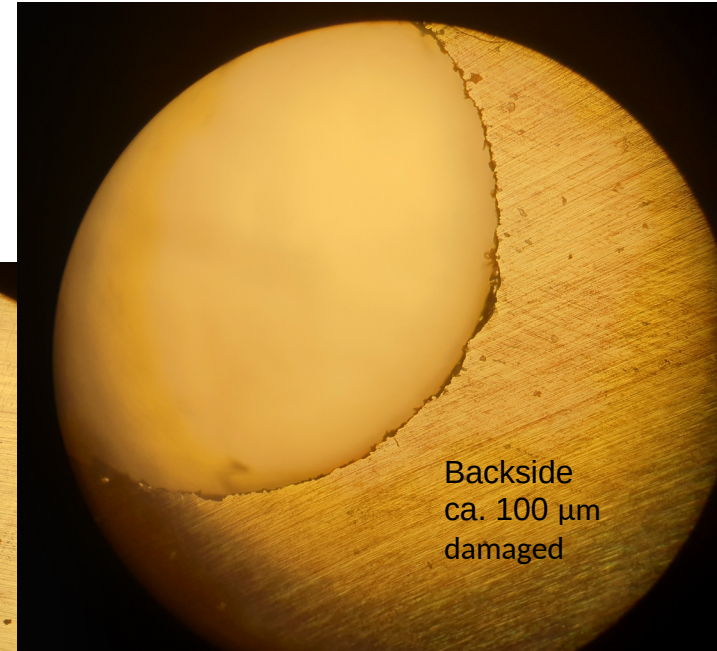
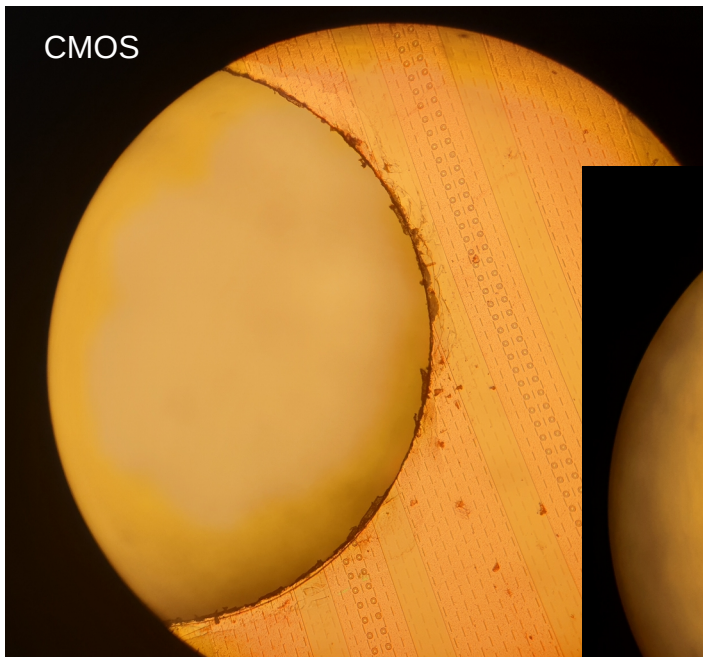
MOUNTING HOLES

- IZM: Etching is very difficult. Combination of etching and backside thinning?
- Lidrotec GmbH (Bochum) suggested by IZM
 - “2.5D” Laser cutting, arbitrary shapes, low thermal stress
- Mechanical drilling in Zentralwerkstatt Bonn
- Laser cutting in Valencia?

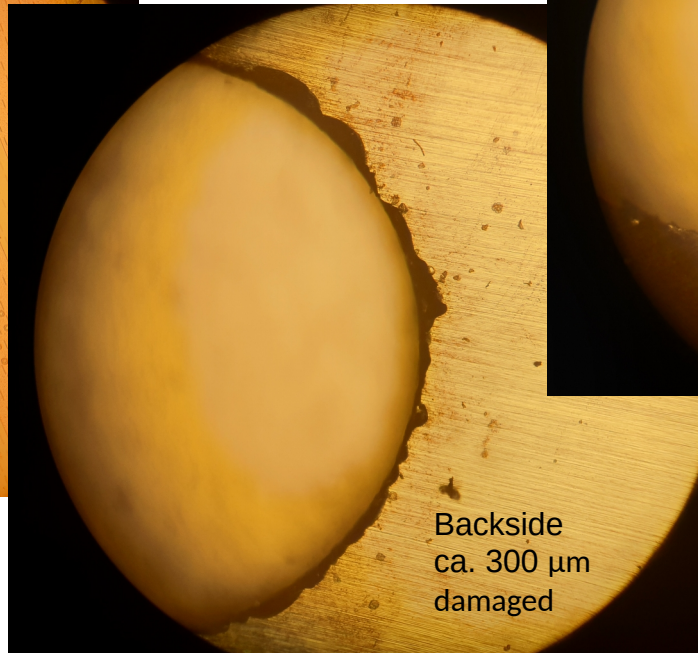


MOUNTING HOLES – BONN PROCESS

- Mechanical drilling with CNC machine in Bonn Zentralwerkstatt
- Diamond drill bit in spiral motion



- Some better, some worse
but it is getting reproducible

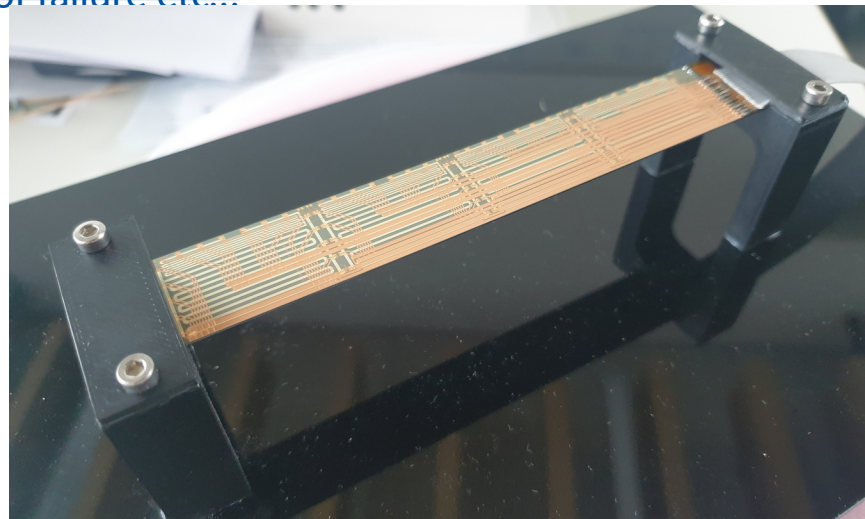


MOUNTING HOLES

- Samples were sent to Valencia but DHL failed to deliver.
- Trying again currently...

Decided to not go for holes!
Alternative mechanism tbd.

- ~~Discussion: Do we really need the holes?~~
 - ~~Was discussed previously in meeting but should discuss again~~
 - ~~Pros/Cons, structural integrity, chance of failure etc...~~
- Alternative:
 - Clamp on top of Module like this maybe:



FURTHER STEPS

Still a lot of Stuff in the making

- Test PCBs for future TDR tests
 - Test PCBs for characterization of test structures
 - Test structure production
 - Test structure simulation
 - Testing new photoresist Durimide (1.5 μm Polyimide)
 - Getting NiAu for top metalization
 - Testing capacity structures
-
- How involve Siegen? Keep very general or go for vtx specific?
 - How keep on with Göttingen? Keep going with gernerall air cooling? Want to go towards full detector simulation? Involve other cooling systems? CO₂/water/parafine cooling?
 - We need a flex and it was decided that Bonn (maybe Siegen) should investigate this further. Need to talk to IpGBT group for connection to PCB.

SUMMARY

- In Progress of testing All-Silicon Module concept
 - RDL will likely work for iVTX!!!
- Electrical test structure production ongoing
 - First simulations used to create optimal trace parameter, more to follow!
 - Electrical characterization will follow soon

- Material budget very low

Idea to reduce it even more with silicon trench capacitors

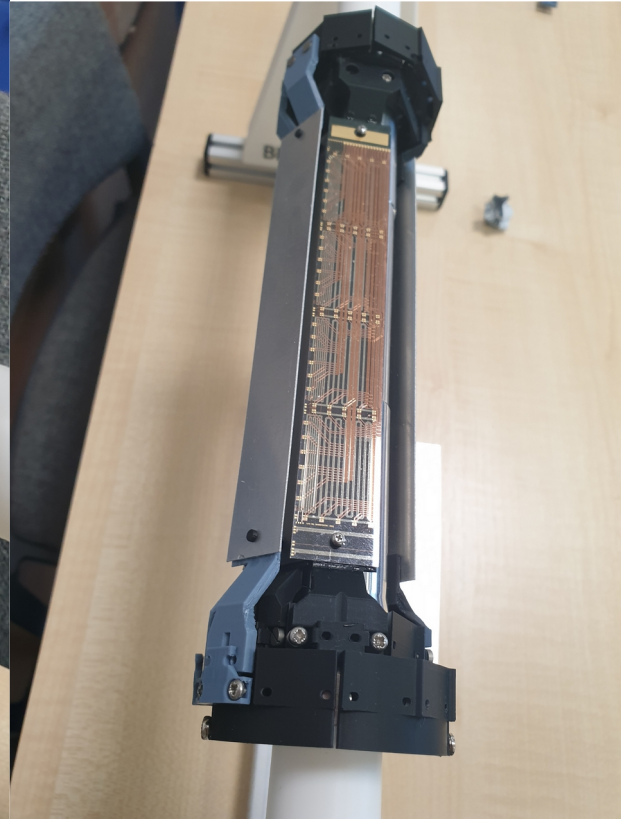
- ~~Hole drilling investigations ongoing~~

- ~~Promising mechanical drilling in Bonn~~
- ~~Laser cutting under investigation~~
- ~~Discussion if holes are needed~~

No holes!

- Detailed thermal studies to be done
 - Our measurements show about 80°C

→ Paris, Valencia, Göttingen
We should consider building real models with thermal ladders.





CAPACITY STUDIES

- Idea: instead of soldering capacities on top of LDOs, make RDL one large capacity
- Using $C = \epsilon A/d$ we can estimate the capacitance of RDL layers

10 μm Polyimide, 6 μm Al 1.5 cm $\times$ 12 cm • 2 layers: 1.59 nF, 0.017% X_0, 22 μm • 3 layers: 3.19 nF, 0.027% X_0, 38 μm • 10 layers: 14.3 nF, 0.099% X_0, 150 μm	2 μm Polyimide, 0.5 μm Al 1.5 cm $\times$ 12 cm • 2 layers: 30.6 nF, 0.0018% X_0, 3 μm • 3 layers: 61.4 nF, 0.0031% X_0, 5.5 μm • 10 layers: 276.1 nF, 0.0119% X_0, 23 μm • 21 layers: 613.6 nF, 0.0258% X_0, 50.5 μm
	1.5 μm Polyimide 0.5 μm Al 1.5 cm $\times$ 12 cm • 2 layers: 35 nF • 10 layers: 315 nF • 21 layers: 701 nF